Backside Copper Metallization of GaAs MESFETs Using TaN as the Diffusion Barrier

Chang-You Chen, Edward Yi Chang, *Member, IEEE*, Li Chang, and Szu-Hung Chen

***Abstract*—Backside copper metallization of GaAs MESFETs using TaN as the diffusion barrier was studied. A thin TaN layer of 40 nm was sputtered on the GaAs substrate before copper film metallization. As judged from the data of X-ray diffraction (XRD), Auger electron spectroscopy (AES), and cross-sectional transmission electron microscopy (TEM), the Cu/TaN films with GaAs were very stable without interfacial interaction up to 550 °C annealing. The copper metallized MESFETs were thermally stressed at 300 °C. The devices showed very little change in the device characteristics ($<3\%$) after thermal stress, and the changes of the electrical parameters and RF characteristics of the devices after thermal stress were of the same order as those devices without Cu metallization. These results show that TaN is a good diffusion barrier for Cu in GaAs devices and the Cu/TaN films can be used for the backside copper metallization of GaAs MESFETs.**

***Index Terms*—Copper, GaAs MESFET, metallization, TaN.**

I. Introduction

COPPER metallization has become a hot topic in silicon IC technology ever since IBM announced its success in silicon VLSI processes [1]–[3]. Now, copper metallization is widely used in 0.18-μm VLSI technology. The advantages of copper metallization for Si VLSI include lower resistivity and higher electromigration resistance. Even though the use of copper as a metallization metal has become very popular in the Si industry, the use of copper as a metallization metal for GaAs FETs has not been reported yet. Traditionally, GaAs FETs and MMICs use Au as the metal for transmission lines and ground plane metallization. The gold used in transmission lines and ground planes are usually plated to more than 2 μm. The use of copper as the metallization metal for transmission lines and ground plane metallization has the following advantages over gold: lower resistivity, higher thermal conductivity, lower cost, and better mechanical properties if plated thicker. Low thermal conductivity and fragile substrates have always been problems in GaAs devices, especially in GaAs power FETs which are required to dissipate a lot of heat. To provide a good thermal sink, the wafer of the power GaAs FETs is usually thinned to 2–5 mils thick, which makes the substrate very fragile. Therefore, the use of a thicker copper layer for backside metallization of GaAs FETs and MMICs to provide better mechanical strength and heat sink capabilities is a very attractive concept.

Copper diffuses very fast into Si when it is in contact with the substrate without any diffusion barrier [4]–[6]. Just like in the silicon case, copper also diffuses very fast into GaAs when deposited on the substrate without any diffusion barrier [7]. Since copper is a deep acceptor for GaAs, this causes degradation of electrical properties in GaAs devices. TaN is currently an effective diffusion barrier for Cu metallization in Si technology, and it also has good adhesion to GsAs. Therefore, using TaN as diffusion barrier should ensure the success of Cu metallization of GaAs. In this paper, the thermal stability of a Cu/TaN/GaAs film structure is investigated. Also, the electrical performances of the Cu/TaN metallized GaAs MESFETs are reported for the first time.

II. Device Fabrication and Metallization

A blanket film structure of Cu/TaN/GaAs was evaluated first. After that, MESFETs with TaN and Cu as backside metallized layers were fabricated for evaluation of electrical performance. The GaAs substrate was cleaned with boiling acetone and isopropyl alcohol for 5 min each and dipped in HF:H_2O_2:H_2O (1:2:20) for 20 s and HCl:H_2O (1:4) for 1 min before it was loaded into the vacuum system. A TaN film of 40 nm thickness was sputtered onto the 3-in (100) GaAs substrate, then 100-nm Cu and 10-nm TaN films were subsequently sputtered on top of the TaN film without breaking vacuum in a multitarget magnetron sputtering system. The top layer of TaN served as a protective layer to prevent oxidation and penetration of oxygen into the films during higher temperature annealing. Both TaN films were deposited by reactive sputtering of Ta in the N_2/Ar mixture with 20% N_2 and 80% Ar. The base pressure was 2.6×10^{-5} Pa before sputtering, and the total sputtering gas pressure was 0.8 Pa during deposition of the films. The samples were annealed for 30 min at temperatures ranging from 400 °C to 600 °C in an argon ambient for materials analysis. X-ray diffraction (XRD), Auger electron spectroscopy (AES), and cross-sectional transmission electron microscopy (TEM) were used for phase identification and study of the interfacial reactions. Both 150 μm and 1 mm gate width MESFETs used in this study were typical epitaxial-material based MESFETs. The process steps included mesa isolation, Au/Ge/Ni ohmic metallization, recessed gate with Au/Pt/Ti metals, plasma enhanced chemical vapor deposition (PECVD) silicon nitride passivation and gold plated air bridges. The GaAs wafers were mechanically thinned to only 75 μm before the backside copper metallization, consisting of 40 nm TaN and 10 μm Cu. The structure of the MESFETs with copper backside metallization is shown in Fig. 1, the superlattice in the structure is the superlattice buffer.

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C. Y. Chen, E. Y. Chang, and S. H. Chen are with the Department of Materials Science and Engineering and the Microelectronics and Information Systems Research Center, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: edc@cc.nctu.edu.tw).

L. Chang is with the Department of Materials Science and Engineering, National Chiao-Tung University, Hsinchu, 300 Taiwan, R.O.C.

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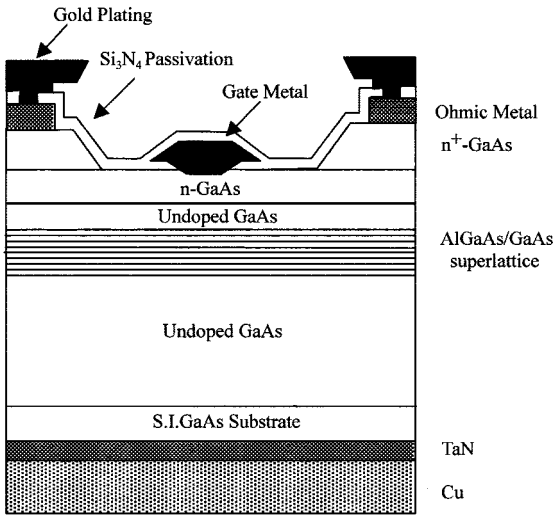

Fig. 1. Structure of the GaAs power MESFET with backside Cu metallization.

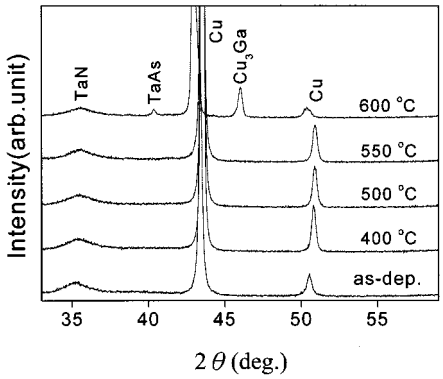

Fig. 2. XRD pattern of the TaN/Cu/TaN/GaAs samples after annealing at various temperatures.

The MESFETs with copper backside metallization were annealed at 300 °C for 2 h under vacuum for thermal stress. The electrical parameters were compared to the devices without copper backside metallization (bare chip without backside metal). Devices with and without copper backside metallization were put through the same thermal stress cycle.

III. Thermal Stability of Multilayers

Fig. 2 shows the XRD results of the samples as-deposited and after annealed from 400 °C to 600 °C. From the XRD data, it is clear that the peaks of TaN and Cu remain unchanged until 550 °C, indicating that the Cu/TaN/GaAs structure is still quite stable at 550 °C. After 600 °C annealing, the intensity of Cu decreased, and new phases of TaAs and Cu_3Ga were identified, suggesting that reactions between the substrate and the metallization layers have taken place at 600 °C. Additional evidence has been obtained from AES depth profiles. Fig. 3 shows the AES depth profiles of the metallized samples as-deposited and after annealing. As can be seen from this figure, the distribution of the elements of the deposited films did not change after 550 °C annealing, however after 600 °C annealing, the results show that copper has diffused into the GaAs substrate. Fig. 4 shows the cross-sectional TEM micrograph of

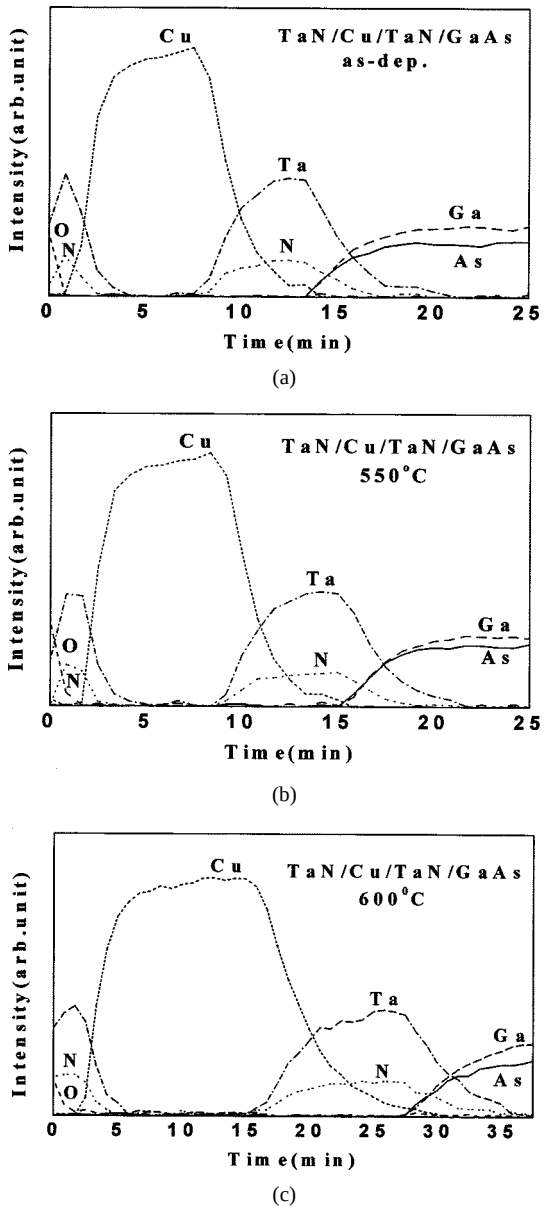

Fig. 3. AES depth profiles of the TaN/Cu/TaN/GaAs samples (a) as deposited; (b) after 550 °C annealing; and (c) after 600 °C annealing.

the TaN/Cu/TaN/GaAs structure. After annealing at 550 °C, grain growth of the Cu occurred, and the interfaces between Cu, TaN, and GaAs were still quite sharp, we found no intermixing of Cu and TaN barrier layers with the GaAs substrate. From the XRD, AES, and TEM data shown above, there is no interfacial reaction between Cu/TaN/GaAs up to 550 °C.

IV. Device Electrical Characterizations

The results from the materials study in the blanket GaAs wafer mentioned above suggest that diffusion of copper into GaAs can be severely retarded to an extremely small level below 550 °C with TaN as the diffusion barrier. To study the electrical performance of the device after copper metallization and the thermal stability of the metallized devices after thermal stress, MESFETs with and without copper metallization were annealed at 300 °C for 2 h and tested for the electrical performance. The electrical

Fig. 4. Cross-sectional TEM micrograph of the TaN/Cu/TaN/GaAs sample after 550 °C annealing.

TABLE I
AVERAGE ELECTRICAL PARAMETER CHANGES OF THE 150-μm DEVICE (a) WITH Cu METALLIZATION. (b) WITHOUT Cu METALLIZATION. (TESTING CONDITIONS: $I_{\rm dss}$ IS MEASURED AT $V_{\rm ds} = 2$ V; G_m IS MEASURED AT $V_{\rm gs} = 0$ V, $V_{\rm ds} = 2$ V; V_p IS MEASURED WHEN $I_{\rm ds} = 150$ μA)

(a) 150 μm Device with Cu Metallization

Change in magnitude		Change in Percent (%)	
ΔIdss (mA)	0.51	$\frac{\Delta \text{Idss}}{\text{Idss}}$	1.60
ΔGm (Vgs=0V) (mS/mm)	0.75	$\frac{\Delta \text{Gm}}{\text{Gm}}$	0.73
ΔVp (V)	0.04	$\frac{\Delta \text{Vp}}{\text{Vp}}$	1.35

(b) 150 μm Device without Cu Metallization

Change in magnitude		Change in Percent (%)	
ΔIdss (mA)	0.91	$\frac{\Delta \text{Idss}}{\text{Idss}}$	3.93
ΔGm (Vgs=0V) (mS/mm)	3.07	$\frac{\Delta \text{Gm}}{\text{Gm}}$	3.03
ΔVp (V)	0.08	$\frac{\Delta \text{Vp}}{\text{Vp}}$	3.00

parameter changes of the 150-μm devices before and after annealing are listed in Table I. As can be seen from Table I(a), for the Cu metallized device, the drain to source saturation current $(I_{\rm dss})$ change is around 1.60%, the transconductance (G_m) change is around 0.73%, and the pinchoff voltage (V_p) change is around 1.35% after thermal stress. The changes in the parameters are of the same order as the devices without copper metallization as compared with the data shown in Table I(b).

There was no appreciable piezoelectrical related pinchoff voltage shift for the devices after copper metallization, which means that there is little stress effect for the copper film. Fig. 5 exhibits the changes in the $I-V$ curves before and after annealing for the devices with and without copper metallization. The pinchoff voltage difference of these two devices shown is due to the nonuniformity of the wet chemical etch in the gate recess process. As can be seen from this figure, for devices with or without copper metallization, the source resistance of both devices increases after annealing. The increase of source resistance after annealing is due to the aging effect of the ohmic metals and not related to the copper metallization. Fig. 6 shows the copper metallized device G_m and

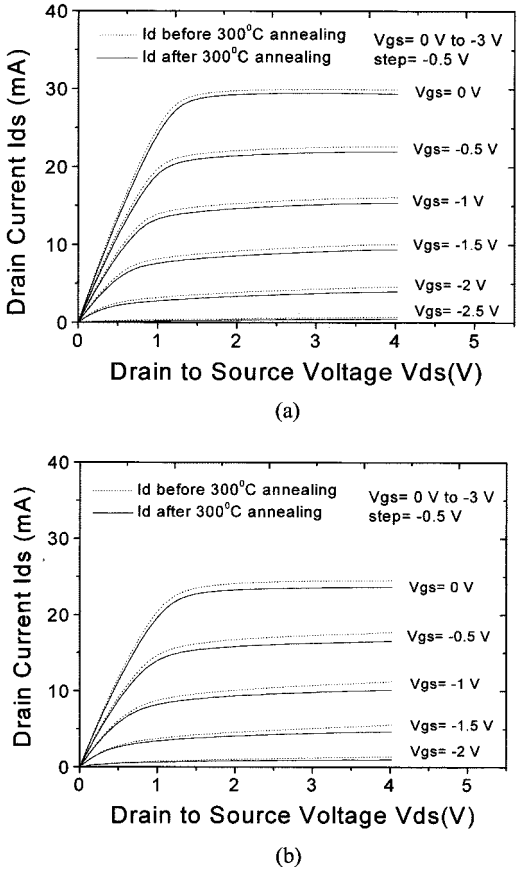

Fig. 5. Changes in the $I-V$ curves for the 150-μm device (a) for device with Cu metallization and (b) for device without Cu metallization.

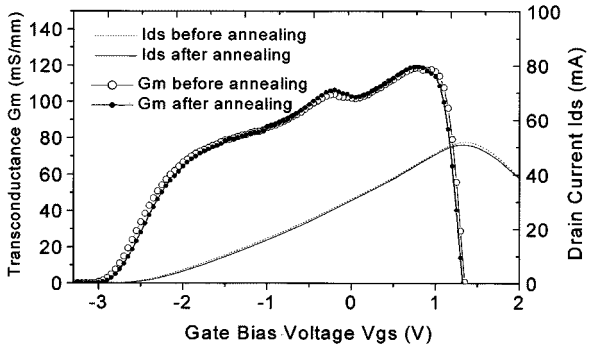

Fig. 6. Changes in the transconductance (G_m) and drain current $(I_{\rm ds})$ versus gate bias voltage $(V_{\rm gs})$ curves for the 150-μm device with Cu metallization.

drain to source current $(I_{\rm ds})$ versus gate bias voltage $(V_{\rm gs})$ curves before and after 300 °C/2 h annealing. The changes of G_m and $I_{\rm ds}$ are very small for the copper metallized device, which implies that there is no copper diffusion into the GaAs substrate, consistent with the material analysis results. The RF characteristics of the devices with and without Cu metallization were also listed. As shown in Table II(a), for 1 μm $\times$ 1 mm device, the changes of $f_{\rm max}$ (maximum oscillation frequency), $G_{\rm max}$ (maximum power gain), and U_G (unilateral power gain) after 300 °C/2 h annealing are 0.34 GHz, 0.38 dB, and 0.69 dB, respectively, for devices with Cu metallization. For devices without Cu metallization, the changes are of the same order as shown in Table II(b). The deterioration of the properties after annealing is mainly caused by the thermal effect on the properties of the intrinsic device itself. Therefore, it

TABLE II
AVERAGE RF PARAMETER CHANGES FOR THE 1 μm × 1 mm DEVICE (a) WITH Cu METALLIZATION (b) WITHOUT Cu METALLIZATION. (TESTING CONDITIONS: $V_{ds} = 7$ V; $I_{ds} = 100$ mA)

(a) 1 μm x 1mm Device with Cu Metallization

Device parameter	Before annealing	After annealing	Change in magnitude	
*f*max (GHz)	10.37	10.03	△*f*max (GHz)	0.34
Gmax (dB) at 0.9GHz	17.24	16.86	△Gmax (dB) at 0.9GHz	0.38
U_G (dB) at 0.9GHz	19.00	18.31	△U_G (dB) at 0.9GHz	0.69

(b) 1 μm x 1mm Device without Cu Metallization

Device parameter	Before annealing	After annealing	Change in magnitude	
*f*max (GHz)	9.6	10	△*f*max (GHz)	-0.4
Gmax (dB) at 0.9GHz	17.36	17.26	△Gmax (dB) at 0.9GHz	0.1
U_G (dB) at 0.9GHz	19.86	19.30	△U_G (dB) at 0.9GHz	0.56

clearly shows that copper backside metallization has a negligible effect on the GaAs device performance. The measured value of sheet resistance for the 40-nm TaN barrier and 10-μm thick Cu film on GaAs MESFETs is 1.9 m$\Omega/\square$, and the corresponding values of electrical conductivity and thermal conductivity are estimated to be 5.18×10^5 $(\Omega\cdot\text{cm})^{-1}$ and 3.47 W/cm °K, respectively, at room temperature. It is noted that bulk copper has a electrical conductivity of 5.88×10^5 $(\Omega\cdot\text{cm})^{-1}$ and a thermal conductivity of 4.01 W/cm °K, whereas gold has a electrical conductivity of 4.55×10^5 $(\Omega\cdot\text{cm})^{-1}$ and a thermal conductivity of 3.17 W/cm °K [8].

V. CONCLUSION

Backside copper metallization with TaN as the diffusion barrier layer was successfully applied to GaAs MESFETs. The Cu/TaN metallization layers on GaAs substrate were very stable up to 550 °C. After 600 °C annealing, however, the interfacial mixing of TaN and Cu with the GaAs substrate occurred, resulting in the formation of TaAs and Cu_3Ga phases. MESFETs metallized using these Cu/TaN layers showed small changes in the electrical parameters after 2 h annealing at 300 °C. The changes of electrical parameters and RF characteristics of the devices including I_{dss}, G_m, V_p, $f_{\max}$, $G_{\max}$, and U_G were within 3%. The magnitude of the changes in the device parameters is of the same order as those devices without copper metallization. The results show that Cu/TaN layers are quite stable and can be of practical use for backside GaAs MESFETs and MMICs metallization.

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Chang-You Chen was born in Taiwan, R.O.C. He received the B.S. degree in materials science and engineering in 1977 from National Tsing Hua University, Hsinchu, Taiwan, and the M.S. degree in materials science and engineering in 1995 from National Chiao-Tung University, Hsinchu, where he is currently pursuing the Ph.D. degree in materials science and engineering.

He is currently with the Department of Materials Science and Engineering, National Hu Wei Institute of Technology, Yun-Lin, Taiwan. His research interest is copper metallization of GaAs devices.

Edward Yi Chang (M'84) received the B.S. degree in materials science and engineering from National Tsing Hua University, Taiwan, R.O.C., and the Ph.D. degree in materials science and engineering from the University of Minneapolis, MN, in 1977 and 1985, respectively.

From 1985 to 1988, he was with Unisys Corporation GaAs Component Group, Eagan, MN, and from 1988 to 1992, he was with Comsat Labs Microelectronic Group. He worked on the GaAs MMIC programs in both groups. In 1992, he joined National Chiao-Tung University, Hsinchu, Taiwan. In 1994, he helped set up the first GaAs MMIC production line in Taiwan, and became president of Hexawave Inc., Hsinchu, in 1995. He returned to the teaching position in National Chiao-Tung University in 1999 and is currently an Associate Professor in the Department of Materials Science. His research interests include new device and process technologies for GaAs MMICs for wireless communication.

Dr. Chang is a member of the IEEE Electron Devices Society.

Li Chang received the B.S. and M.S. degrees in materials science and engineering, from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1977 and 1981, respectively, and the D.Phil. degree in materials from the University of Oxford, Oxford, U.K., in 1986.

He is currently with the Department of Materials Science and Engineering, National Chiao-Tung University, Hsinchu. His interest is in the area of thin-film processing and microstructural characterization.

Szu-Hung Chen was born in Taiwan, R.O.C. He received the B.S. degree in materials science and engineering in 1997 from Tsing Hua University, Hsinchu, Taiwan. He is currently pursuing the Ph.D. degree in materials science and engineering at Chiao-Tung University, Hsinchu. His research interests are new materials and process technology for GaAs microwave devices.