Characterization and Modeling of Edge Direct Tunneling (EDT) Leakage in Ultrathin Gate Oxide MOSFETs

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***Abstract*—This paper examines the edge direct tunneling (EDT) of electron from n$^+$ polysilicon to underlying n-type drain extension in off-state n-channel MOSFET's having ultrathin gate oxide thicknesses (1.4–2.4 nm). It is found that for thinner oxide thicknesses, electron EDT is more pronounced over the conventional gate-induced-drain-leakage (GIDL), bulk band-to-band tunneling (BTBT), and gate-to-substrate tunneling, and as a result, the induced gate and drain leakage is better measured per unit gate width. A physical model is for the first time derived for the oxide field $E_{\rm OX}$ at the gate edge by accounting for electron subband in the quantized accumulation polysilicon surface. This model relates $E_{\rm OX}$ to the gate-to-drain voltage, oxide thickness, and doping concentration of drain extension. Once $E_{\rm OX}$ is known, an existing DT model readily reproduces EDT I–V consistently and the tunneling path size extracted falls adequately within the gate-to-drain overlap region. The ultimate oxide thickness limit due to EDT is projected as well.**

***Index Terms*—Author: Please e-mail keywords@ieee.org for more info..**

I. INTRODUCTION

THE off-state drain leakage is one of the big issues for aggressively shrunk MOSFET's. The well recognized mechanisms are the gate-induced-drain-leakage (GIDL) [1], [2], the bulk band-to-band tunneling (BTBT) [3], and the drain-induced-barrier-lowering (DIBL) enhanced subthreshold conduction. In the case of reverse substrate bias for suppression of DIBL or subthreshold leakage, the bulk BTBT dominates [4]. On the other hand, the gate leakage due to direct tunneling (DT) [5] was measured per unit oxide area and a certain criterion of 1 A/cm^2 set the ultimate limit of scalable oxide thicknesses [6], [7]. Recently, Yang *et al.* [8] have originally explored a dominant off-state leakage component via edge direct tunneling (EDT) of electron from n$^+$ polysilicon to underlying n-type drain extension. Also carried out in [8] is the I-V modeling obtained by following the procedure in [9], [10]. However, some parameters of great relevance were not clarified yet, such as the tunneling path area and the dopant concentration of drain extension. In particular, the oxide field is an essential input parameter to the DT I-V model in [9],

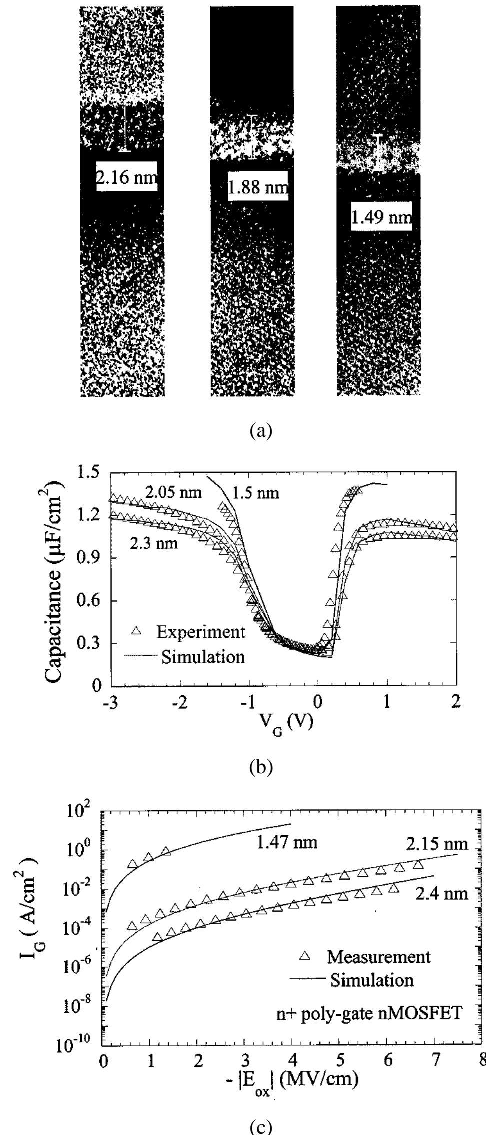

Fig. 1. (a) HRTEM images of three nMOSFET gate stacks. $T_{\rm OX}$ values extracted from the canvases correspond to 2.16, 1.88, and 1.49 nm, respectively. (b) The oxide thickness extraction using C-V method was based on van Dort's model [13] and successive researchers [14], [15]. Best fitting produces $T_{\rm OX}$ of 2.3, 2.05, and 1.5 nm, respectively. (c) I–V fitting to find $T_{\rm OX}$. $T_{\rm OX}$ values extracted by electron DT model [9], including quantization effect in accumulation layer under $V_G < V_{\rm FB}$ are 2.40, 2.15, and 1.47 nm, respectively.

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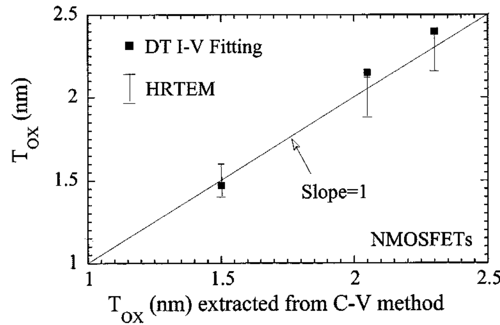

Fig. 2. Comparing $T_{\rm OX}$ extracted from several techniques.

[10], and is usually gained by means of the so-called C-V integration technique [11]. However, unlike the whole area counterpart, it is impossible to assess such oxide field at the gate edge for the situation that the overlap capacitance is too small to detect using present C-V equipment.

In this paper, we report that as scaled gate oxide thickness approaches the DT regime, the EDT of electron from n^+ polysilicon to underlying n-type drain not only dominates the gate leakage, but also can prevail over the conventional GIDL, in agreement with [8]. This phenomenon is more pronounced for thinner oxide thicknesses, and EDT can even compete over the bulk BTBT in the case of reverse substrate bias not mentioned in [8]. It is clarified that the gate leakage in stand-by mode indeed originates from the edge part rather than the whole gate oxide, and thus should be measured per unit gate width rather than per unit oxide area as in [6], [7]. Also presented is a physical model for the first time derived for the oxide field $E_{\rm OX}$ at the gate edge by accounting for electron subband in the quantized accumulation polysilicon surface. This model is valuable in enabling consistently the reproduction of EDT I–V, the extraction of EDT path size and dopant concentration of drain extension, and even the projection of ultimate oxide thickness.

II. Experiment and Characterization

The n^+ poly-gate nMOSFET's were fabricated by a 0.18-um process technology [12]. The gate oxides were grown in dilute wet oxygen ambient to three different thicknesses. The gate dimension was drawn to $100 \times 100\ \mu\text{m}^2$. Accurate determination of ultrathin oxide thickness $T_{\rm OX}$ is strongly demanded. Three techniques in terms of high resolution TEM (HRTEM), polysilicon depletion and quantum mechanics (QM) corrected C–V [13]–[15], and DT I–V [9] were adopted as shown in Fig. 1, through which consistent results were achieved as compared in Fig. 2. Fig. 1(a) just shows highly-localized HRTEM cross section while the variation across the wafer is depicted in Fig. 2 in terms of a bar. Our C–V data in Fig. 1(b) was measured in parallel mode with 1-MHz AC frequency. QM corrected C–V fitting based on van Dort's model for surface quantization [13], [14] was carried out to extract physical $T_{\rm OX}$. In particular, the singular point problem encountered around the flat-band voltage $V_{\rm FB}$ was eliminated by adopting a modified version [15]. In Fig. 1(b), C–V fitting for $T_{\rm OX} = 1.47$ nm is limited to nondistorted range, $-1.4\ \text{V} < V_G < 0.6\ \text{V}$, where the tunneling current effect or others can be neglected. C–V fitting

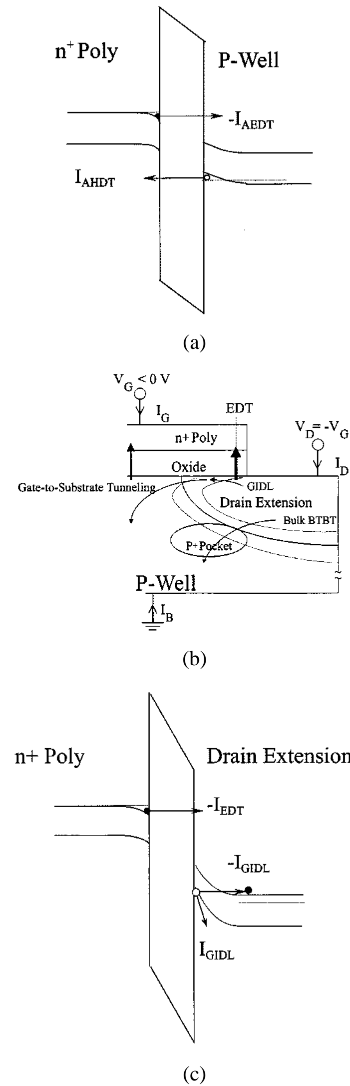

Fig. 3. (a) Band diagram located at channel region far from drain extension. Accumulation hole DT ($I_{\rm AHDT}$) and accumulation electron DT current ($I_{\rm AEDT}$) both contribute to gate-to-substrate tunneling current. (b) Schematic cross section near gate/drain overlap region under $V_G < 0$ V and $V_D = -V_G$. Different tunneling paths are shown. (c) Band diagram located at gate/drain overlap region, showing EDT and GIDL under off-state condition.

in Fig. 1(b) also produced the n^+ polysilicon dopant concentration $N_{\rm poly} = 6 \times 10^{19}\ \text{cm}^{-3}$ and the effective channel dopant concentration $N_{\rm well} = 5 \times 10^{17}\ \text{cm}^{-3}$, all being found to be consistent with the SIMS doping profile. In Fig. 1(c), the devices were biased in poly accumulation (negative gate voltage, $V_G < V_{\rm FB}$) with source, drain, and p-well tied to ground, and the oxide field strength $E_{\rm OX}$ was obtained in advance by means of the C–V integration technique [11]. With the effective mass $m_{\rm oxe} = 0.61\ m_o$ for Franz-type dispersion relationship in the oxide, the conduction electron DT I–V fitting in Fig. 1(c) extracted $T_{\rm OX} = 1.47, 2.15$, and 2.40 nm from three samples. Note that as all data go closer to the straight line with the unity slope in Fig. 2, more confidence for DT I–V extracted $T_{\rm OX}$, as well as its subsequent applications in consistently calculating the EDT current of electron from n^+ polysilicon to underlying n-type drain, can all be ensured.

Fig. 3 illustrates the tunneling leakage paths and related band diagrams. With source open and under $V_G = -V_D$, the

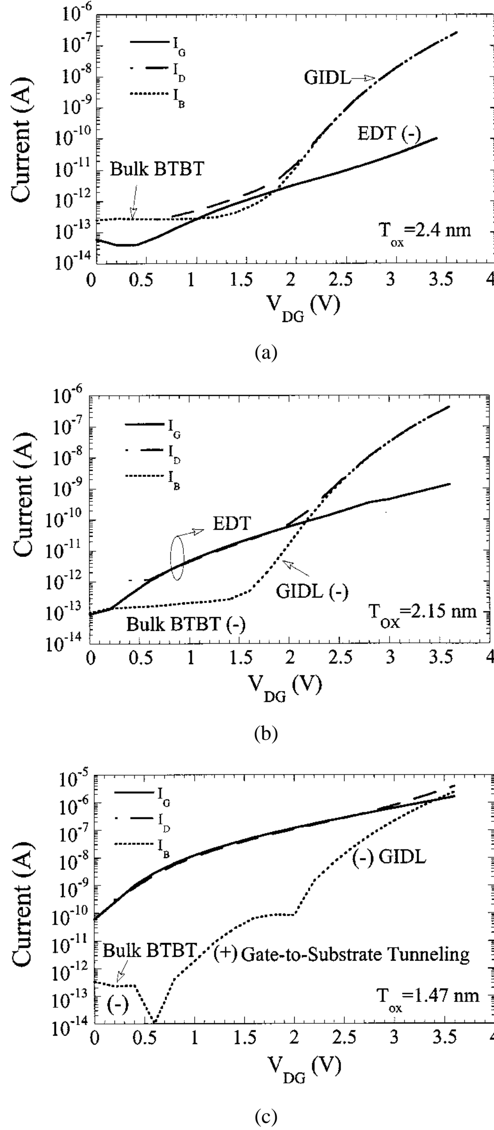

Fig. 4. Displaying the measured terminal currents versus $V_{\rm DG}$ for three different $T_{\rm OX}$ (a), (b), and (c) under $V_G = -V_D$ and source open. The aspect ratio $W/L = 10\,\mu$m/0.5 μm. (a) EDT dominates the drain leakage in $1\ \mathrm{V} < V_{\rm DG} < 1.8$ V. (b) The edge tunneling mechanism dominates I_D for $0\ \mathrm{V} < V_{\rm DG} < 2.2$ V, and GIDL constitutes drain leakage for $V_{\rm DG} > 2.2$ V. (c) The edge tunneling mechanism prevails over the drain leakage current. Note that gate-to-substrate tunneling is an important leakage source for I_B in $0.5\ \mathrm{V} < V_{\rm DG} < 2$ V.

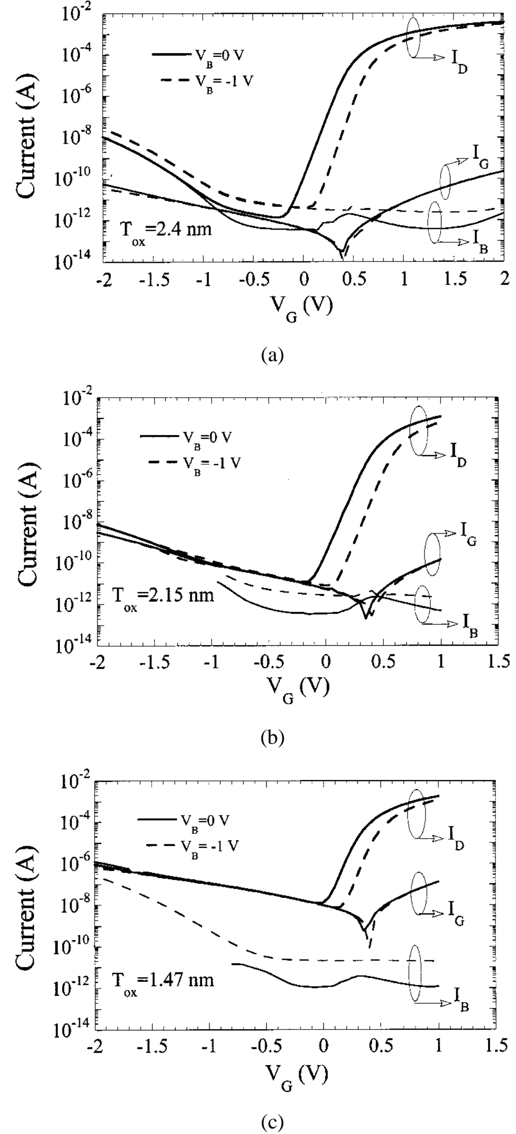

Fig. 5. Measured terminal current versus gate voltage. The aspect ratio $W/L = 10\,\mu$m/ $0.5\,\mu$m. With source grounded and $V_D = 1$ V, (a)–(c) shows the measured terminal currents versus both polarities of V_G for substrate bias $V_B = 0$ and -1 V. (b) and (c) exhibits that off-state drain current does not come from GIDL or bulk BTBT but EDT due to the evidence, $I_G \sim I_D$.

measured drain current I_D, gate current I_G, and bulk current I_B are plotted in Fig. 4 versus $V_{\rm DG}$ for three different oxide thicknesses. Fig. 4 reveals that the drain current primarily comprises the GIDL, the bulk BTBT, and the gate current, implying the EDT as the origin of the latter component. It can be observed that the EDT dominates the gate leakage, and there exists a certain range where the EDT prevails over the conventional GIDL and bulk BTBT. This phenomenon is more pronounced for thinner oxide thicknesses. In Fig. 4(c) for 1.47 nm thick oxide, the polarity of the bulk current is reversed due to gate-to-substrate tunneling.

With source grounded and $V_D = 1$ V, the measured terminal currents versus both polarities of V_G are plotted in Fig. 5 for substrate bias $V_B = 0$ and -1 V. Obviously, for $T_{\rm ox} = 2.40$ nm the bulk BTBT at $V_B = -1$ V dominates the drain leakage in $-0.5\ \mathrm{V} < V_G < 0$ V, while such role is replaced by EDT for thinner oxides. In Fig. 5(b) and (c), $I_D \simeq I_G$ for $V_G < 0$ V, which seems to be unchanged with and without substrate bias, supporting the EDT mechanism responsible. This implies that EDT is only dependent on the vertical electrical field but not the lateral electrical field; that is, the edge tunneling can be assumed as one-dimensional approximation. Besides, we found experimentally that the EDT leakage is indeed proportional to the gate width, regardless of the aspect ratio (W/L). This means that the gate leakage in stand-by mode (i.e., only source and gate tied to ground) should be adequately measured per unit gate width.

III. EDT Model

An analytic electron DT model [9] was again employed in this study. One essential physical parameter, namely, oxide field

$E_{\rm OX}$ at the gate edge, has to be estimated under each value of $V_{\rm GD}$. In our work, the mentioned C–V integration technique failed to extract $E_{\rm OX}$ because EDT occurs only within the area of gate/drain overlap region and it is difficult to measure such small capacitance in the overlap part. First of all, oxide field at the gate edge can be obtained by solving the following equation:

$$V_{\rm DG} - V_{\rm FB}(\cong 0) = V_{\rm poly} + T_{\rm OX}E_{\rm OX} + V_{\rm DE} \tag{1}$$

where $V_{\rm poly}$ is the potential drop in the polysilicon and $V_{\rm DE}$ is that in the drain extension region. The charge Q available for the tunnel process is modeled as field induced, i.e.,

$$Q = \epsilon_{\rm OX}E_{\rm OX}. \tag{2}$$

Due to the lowest quantized energy, the accumulated electrons mainly fill in the first subband. Thus, relating this sheet charge density to the number of occupied subband states constructs the charge conservation relationship

$$q(E_{\rm FN} - E_1)\frac{\eta m_{S_i,\parallel}}{\pi\hbar^2} = \epsilon_{\rm OX}E_{\rm OX} \tag{3}$$

where $E_{\rm FN}$ is the quasi-Fermi level in the n^+-polysilicon and η is the degeneracy factor. Using triangle-like electrostatic potential approximation to the polysilicon surface, the quantized energy of the first subband, can be calculated directly with Sommerfeld-Wilson's quantization rule

$$E_1 = \left(\frac{\hbar^2}{2m_{S_i,\perp}}\right)^{1/3}\left(\frac{9\pi q\epsilon_{\rm OX}}{8\epsilon_{S_i}}E_{\rm OX}\right)^{2/3}. \tag{4}$$

Applying the first subband approximation to the accumulated n^+ poly gate and the deep depletion approximation to the underlying drain extension region as shown in Fig. 6, we get

$$V_{\rm poly} \simeq E_{\rm FN}/q = \epsilon_{\rm OX}E_{\rm OX}\frac{\pi\hbar^2}{q^2\eta m_{S_i,\parallel}} + E_1/q \tag{5}$$

$$V_{\rm DE} = \frac{\epsilon_{\rm OX}^2 E_{\rm OX}^2}{2q\epsilon_{S_i}N_{\rm DE}} \tag{6}$$

where $N_{\rm DE}$ is the dopant concentration of drain extension. Here, $m_{S_i,\perp} = 0.32,\ m_o$, $m_{S_i,\parallel} = 0.25\ m_o$, and $\eta = 4$ were used to approximate the band-structure for $\langle 110\rangle$ oriented n^+-polysilicon grains [9]. As a result, (1) can further be rearranged as

$$V_{\rm DG} = a_1E_{\rm OX} + a_2E_{\rm OX}^2 + a_3E_{\rm OX}^{2/3} \tag{7}$$

where

$$a_1 = T_{\rm OX} + \frac{\pi\hbar}{q^2\eta m_{S_i,\parallel}}\epsilon_{\rm OX}$$
$$a_2 = \frac{\epsilon_{\rm OX}^2}{2q\epsilon_{S_i}N_{\rm DE}}$$
$$a_3 = \left(\frac{\hbar^2}{2m_{S_i,\perp}}\right)^{1/3}\left(\frac{9\pi q\epsilon_{\rm OX}}{8\epsilon_{S_i}}\right)^{2/3}.$$

Thus, it is easy to get $E_{\rm ox}$ by solving (7) numerically. With the effective edge-tunneling area $A_o(=L_{\rm TN} \times W)$, the EDT I–V model reads [9]

$$I_{\rm EDT} = A_oQfT = L_{\rm TN}WQfT \tag{8}$$

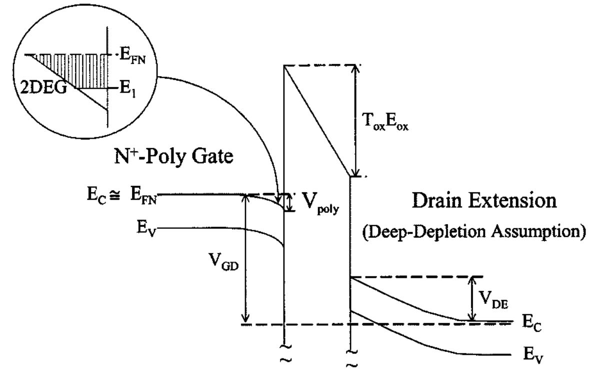

Fig. 6. Band diagram drawn along gate/SiO_2/drain extension. The accumulation potential bending, $V_{\rm POLY}$, with two-dimensional electron gas (2-DEG) concept and the silicon surface potential bending, $V_{\rm DE}$, with the deep depletion approximation are adopted in the procedure of $E_{\rm OX}$ extraction.

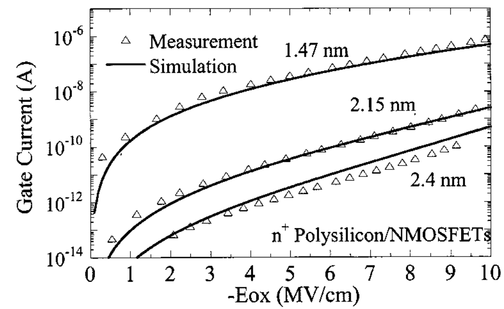

Fig. 7. Comparison of the EDT calculation and experiment. The extracted effective EDT range is 6.25 nm wide from the gate edge, equal for three different oxide thickness. $W = 10\ \mu$m.

where

- Q sheet charge of the accumulation layer;
- f electron impact frequency on the n^+-poly/SiO_2 interface;
- T is the modified transmission probability considering interface reflection factor [9].

Once $E_{\rm OX}$ was quantified, an excellent reproduction for different oxide thicknesses was achieved with $N_{\rm DE} = 3 \times 10^{19}$ 1/cm^3 and effective mass $m_{\rm oxe} = 0.61\ m_o$ resulting from Franz-type dispersion relation in tunnel oxide, as depicted in Fig. 7. The tunneling path extracted was 6.25 nm wide $(=L_{\rm TN})$ from the gate edge (due to $N_{\rm DE}$ extracted). This is quite reasonable since the drain extension beneath the gate is less than 0.01 μm. Therefore, the consistent modeling work validates the EDT as the origin of the leakage of concern.

It is recognized that the drain extension may be considered a nonscalable factor [16], implying a constant $L_{\rm TN}$ of 6.25 nm in the scaling direction. With this in mind, the conventional criterion of 1 A/cm^2 can be transferred to 0.625 μA/cm. Using the roadmap parameters [17], the electron EDT current is calculated versus scaling generation oxide thickness as shown in Fig. 8. In this figure, the new criterion due to electron EDT sets the ultimate oxide thickness of around 1.4 nm.

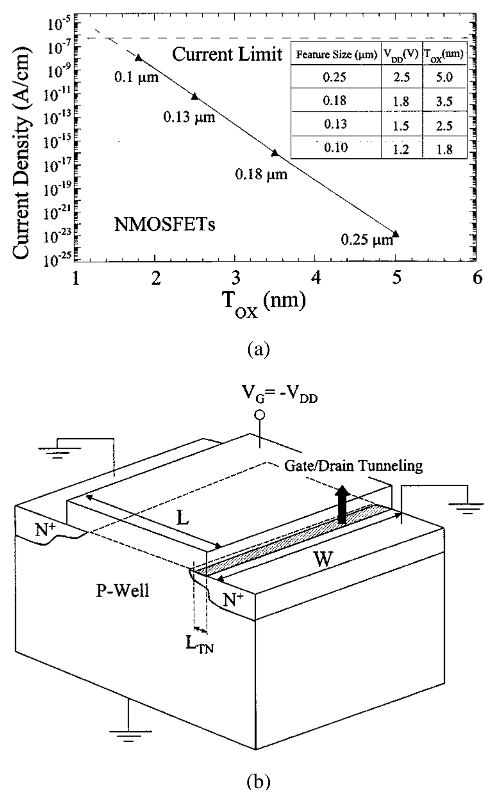

Fig. 8. (a) The calculated electron DT current per gate width versus scaling generation oxide thickness in NMOSFET's. The inset shows the scaling parameters from [17]. (b) Exhibiting the EDT path in the structure of NMOSFET. $L_{\mathrm{TN}} = 6.25$ nm.

IV. Conclusion

The EDT of electrons from n^+ polysilicon to underlying n-type drain extension has shown its tremendous impact on the drain leakage and gate leakage. This effect is more pronounced for thinner oxide thicknesses. It is clarified that the gate leakage in practical stand-by mode should be measured per unit gate width, particularly for MOSFETs with oxide thickness less than 2.40 nm. Eventually, a physical model cited in the literature does reproduce consistently experimental EDT I–V characteristics and its tunneling area extracted indeed falls within the gate-to-drain overlap region. The ultimate oxide thickness due to electron EDT has also been projected based on the model.

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M. S. Liang photograph and bio not available at the time of publication.