

Leakage Mechanism in Cu Damascene Structure with Methylsilane-Doped Low- K CVD Oxide as Intermetal Dielectric

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Abstract—This letter investigates the leakage mechanism in the Cu damascene structure with methylsilane-doped low- k CVD organosilicate glass (OSG) as the intermetal dielectric (IMD). The leakage between Cu lines was found to be dominated by the Frenkel–Poole (F-P) emission in OSG for the structure using a 50-nm SiC etching stop layer (ESL). In the structure using a 50-nm SiN ESL, the leakage component through SiN also made a considerable contribution to the total leakage in addition to the bulk leakage from trapped electrons in OSG. An appropriate ESL of sufficient thickness is essential to reduce the leakage through the ESL if an ESL is used in the Cu damascene integration scheme.

Index Terms—Copper, CVD oxides, damascene structures, Frenkel–Poole (F-P) emission, low- k dielectrics, methylsilane, organosilicate glass (OSG).

I. INTRODUCTION

C-DOPED SiO₂-based low- k CVD OSGs are receiving extensive attention for potential BEOL applications because of their superior physical rigidity, mechanical strength, and process extendibility, which together reduce the risks and costs of integration. Previous studies on the methylsilane-doped OSGs have been concentrated on their electrical reliability with respect to integration with Cu using planar MIS capacitors [1]. In practical applications, however, considerable attention will be focused on the electrical reliability of the patterned wafers, such as leakage current mechanisms and potential leakage paths in OSG and its surrounding dielectrics. In this letter, we investigate the leakage mechanism in the Cu damascene structure using OSG as the intermetal dielectric (IMD) and the impact of ESL integrity on the leakage.

II. EXPERIMENTAL

The leakage between Cu lines (I_L) was measured on a 0.23/0.23- μm (line width/space) comb/serpentine structure. A single level Cu damascene process with methylsilane-doped low- k CVD OSG as the IMD was employed to fabricate the test structures. A 750-nm LPCVD BPSG layer was first deposited

on p-Si to serve as the interlevel dielectric (ILD). Either a PECVD SiN ($k = 7 - 9$) or a PECVD SiC ($k = 4 - 6$) ESL (50 nm) was then deposited on the BPSG layer, followed by the deposition of 250-nm PECVD OSG ($k = 2.9$) using (CH₃)SiH₃/N₂O gases at 17 °C. Another split of samples with a very thin SiN ESL (10 nm) were also prepared. The SiN ESL was deposited at 400 °C with SiH₄/NH₃/N₂ flow ratio of 3/1/67 and a total gas pressure of 1–5 Torr at an RF power of 280–330 W. The deposition condition was not optimized, mainly due to low RF power, so that the leakage component contributed by the SiN layer can be studied. After patterning of 0.23- μm trenches in the OSG/ESL/BPSG dielectric stack, the damascene Cu feature was constructed by electroplating Cu on a 30-nm TaN barrier, and was passivated with a 100-nm PECVD SiN layer after CMP. The completed damascene structure was annealed at 400 and 500 °C for 10 h in an N₂ ambient before the ramped voltage test. I_L was measured as a function of ramped voltage (V_L) at room temperature to 250 °C with a continuous N₂ purge throughout testing.

III. RESULTS AND DISCUSSION

Fig. 1(a) and (b) show the I_L - V_L characteristics at various temperatures for the structures with a SiN and a SiC ESL (50 nm), respectively, after annealing at 400 °C. To look into the leakage mechanism of these currents, the I_L - V_L curves were transformed into the I_L - E_L (electric field) relation like the $\text{Ln}(I_L)$ - $(E_L)^{1/2}$ plots shown in Fig. 1(c) and (d). Notably, $\text{Ln}(I_L)$ is linearly correlated with $(E_L)^{1/2}$, corresponding to either Frenkel–Poole (F-P) or Schottky mechanism [2]. To differentiate F-P from Schottky, the temperature (T) dependence of I_L plotted as $\text{Ln}(I_L/T^2)$ - $(1/T)$ relation curves at a number of ramped voltages are illustrated in Fig. 1(e) and (f). The experimental data points are best fit with a second order polynomial rather than a straight line that negates the Schottky nature of I_L under consideration. I_L can be expressed by (1) if it is dominated by the F-P emission, and the effective dielectric constant ϵ can be determined by the slope of the straight line section of the $\text{Ln}(I_L)$ - $(E_L)^{1/2}$ plot, as shown in (2) [3], [4]

$$I_L \propto I_{LO} \exp(\beta E_L^{1/2} / K_B T), \quad \text{where } \beta = (q^3 / \pi \epsilon)^{1/2} \quad (1)$$

$$\text{Slope} = \beta / K_B T (\text{cm/V})^{1/2} \quad (2)$$

I_{LO} : low-field leakage current q : electronic charge

K_B : Boltzmann constant.

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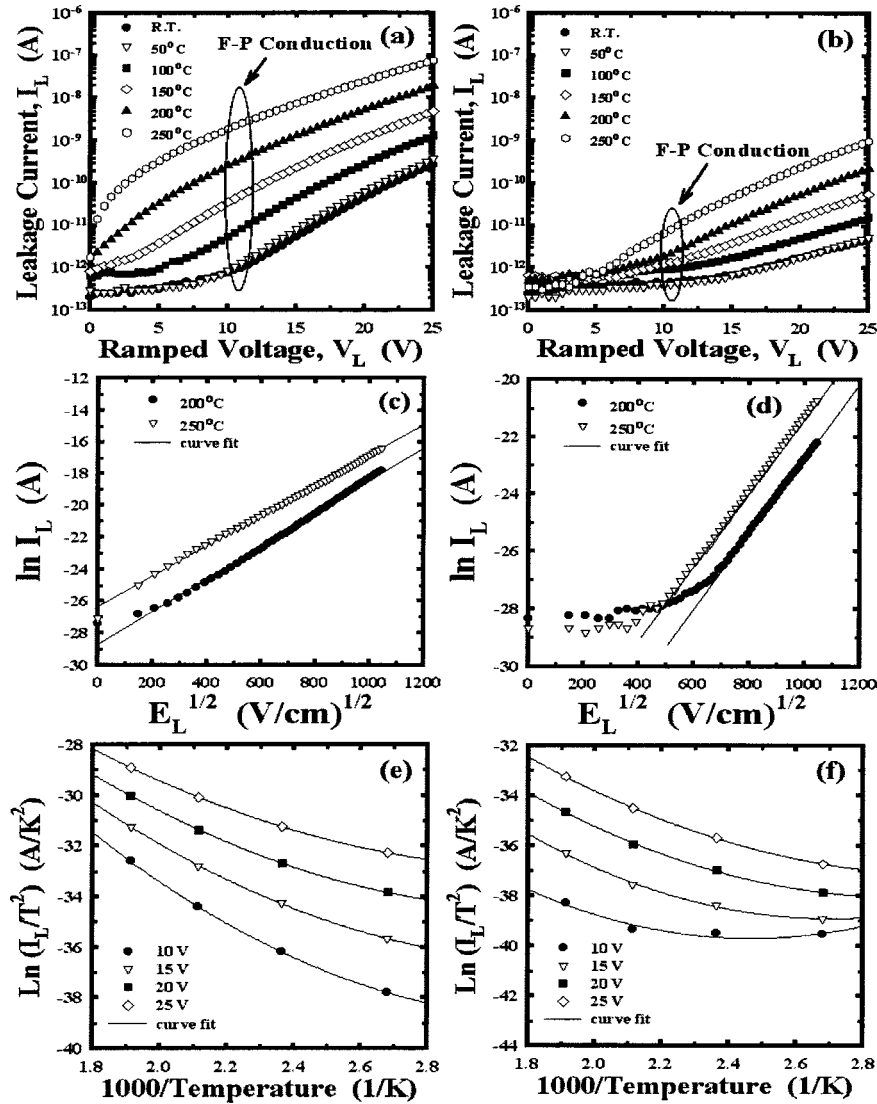


Fig. 1. I_L - V_L characteristics at various temperatures for the Cu damascene structures with (a) SiN and (b) SiC ESL after annealing at 400 °C for 10 h in N_2 ; I_L - E_L (electric field) characteristics for the structures with (c) SiN and (d) SiC ESL; temperature (T) dependence of I_L for the structures with (e) SiN and (f) SiC ESL.

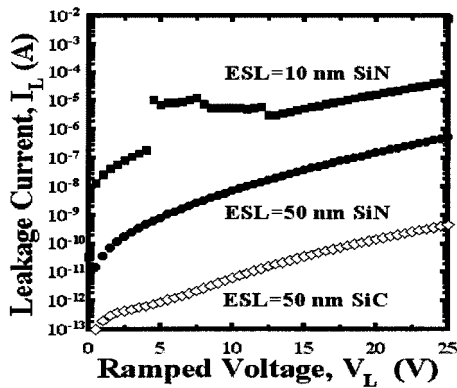


Fig. 2. I_L - V_L characteristics at 250 °C for various structures after annealing at 500 °C for 10 h in N_2 .

The values of the slope and the extracted dielectric constant are summarized in Table I. The effective ϵ values (2.81 and 2.88) extracted from the structure with a SiC ESL (50 nm) are very close to

that of OSG. This indicates that the F-P emission was mainly induced by field-enhanced thermal excitation of trapped electrons in OSG [2], and the increase in I_L with temperature was due to the enhancement in thermal excitation of the trapped electrons. These trap states may result from the presence of chemical impurities (such as OH and H_2O groups) or dangling bonds of Si, O, and CH_3 molecules generated during the deposition of OSG at a low deposition temperature of 17 °C in this study. However, the leakage characteristics in OSG can be improved by depositing OSG at a higher temperature and/or applying an NH_3 -plasma post-treatment to annihilate the trap states, and thus suppressing the F-P conduction. On the other hand, the finding that the effective ϵ values (3.29 and 3.12) extracted from the structure with a SiN ESL (50 nm) are larger than OSG's k value of 2.9 implies that in addition to the bulk leakage from trapped electrons in OSG, the leakage component through SiN also made a considerable contribution to the total I_L . Furthermore, test structures with a SiN ESL exhibited a larger I_L than those with SiC at a given temperature. Since the structural geometries of these two test structures

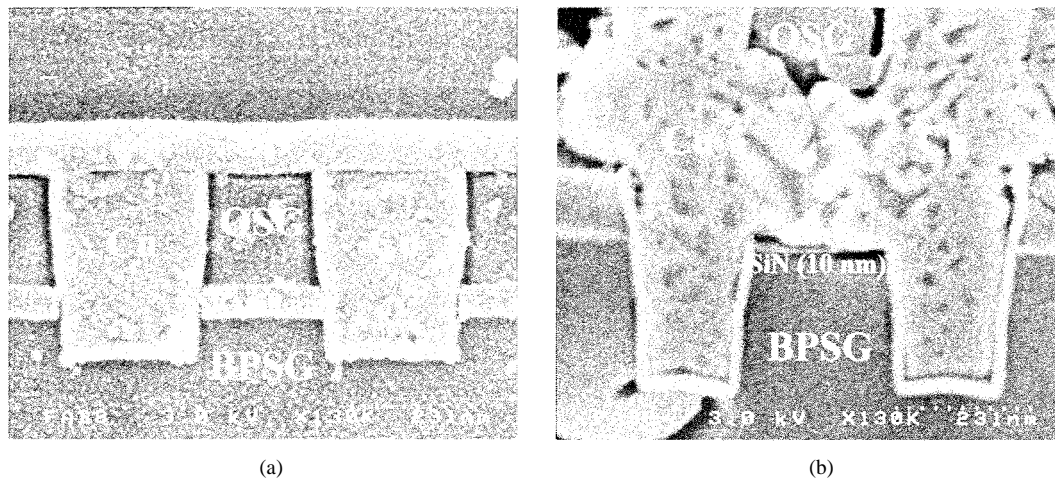


Fig. 3. Cross-sectional SEM micrographs of 500 °C annealed test structures with (a) 50-nm SiC and (b) 10-nm SiN ESL after ramped voltage measurements (with maximum voltage of 25 V) at 250 °C.

TABLE I
VALUES OF THE SLOPE $\beta/K_B T$ AND THE EXTRACTED DIELECTRIC CONSTANT ϵ AT 200 AND 250 °C

Temperature (°C)	200		250		
	ESL	$\beta/K_B T$ (cm/V) ^{1/2}	ϵ	$\beta/K_B T$ (cm/V) ^{1/2}	ϵ
SiN (50 nm)		1.03×10^{-2}	3.29	9.52×10^{-3}	3.12
SiC (50 nm)		1.11×10^{-2}	2.81	9.91×10^{-3}	2.88

are essentially identical, the contribution from the bulk leakage of trapped electrons in OSG should be equal. The larger I_L in the structure with a SiN ESL is presumably due to the leakage component through SiN. From the measured tensile stress of the SiN layer used herein, it is believed that some sort of defects, such as cracks or dangling bonds, may be induced in SiN during the thermal cycle and/or electrical testing. Fig. 2 shows the I_L-V_L curves measured at 250 °C on various structures after annealing at 500 °C. The I_L-V_L characteristics for the structures with a SiN and a SiC ESL (50 nm) resemble those of the corresponding structures annealed at 400 °C, indicating the superior thermal stability of these damascene Cu structures under the present thermal conditions, as revealed from the SEM micrograph of Fig. 3(a). However, severe degradation of I_L was found for the structure with a very thin SiN ESL (10 nm). It was reported that the defect density in the SiN layer increases with the decreasing layer thickness [5]. Thus, using a 10-nm SiN ESL greatly exacerbated the leakage component through SiN. Such a large leakage crowded at the localized TaN barrier and the OSG/SiN interface, causing the TaN breakdown and subsequent massive Cu penetration in OSG [Fig. 3(b)].

IV. CONCLUSION

The F-P emission was found to dominate the leakage behavior between Cu lines in the Cu damascene structure with

OSG as the IMD using a SiC ESL. In the structure using a SiN ESL, the leakage component through SiN also made a considerable contribution to the total leakage in addition to the bulk leakage from field-enhanced thermal excitation of trapped electrons in OSG. It is imperative to use an appropriate ESL of sufficient thickness if an ESL is used in the Cu damascene integration scheme.

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REFERENCES

- [1] Z. C. Wu, Z. W. Shiung, C. C. Chiang, W. H. Wu, M. C. Chen, S. M. Jeng, W. Chang, P. F. Chou, S. M. Jang, C. H. Yu, and M. S. Liang, "Comparative study of physical and electrical characteristics of F- and C-doped low-k CVD oxides," in *2000 Adv. Metallization Conf. Proc.*, Oct. 2000.
- [2] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981, pp. 402–407.
- [3] P. T. Liu, T. C. Chang, Y. L. Yang, Y. F. Cheng, and S. M. Sze, "Effects of NH₃-plasma nitridation on the electrical characterizations of low-*k* hydrogen silsesquioxane with copper interconnects," *IEEE Trans. Electron Devices*, vol. 47, pp. 1733–1739, Sept. 2000.
- [4] J. S. Park, D. K. Sohn, J. U. Bae, C. H. Han, and J. W. Park, "The effect of Co incorporation on electrical characteristics of n⁺/p shallow junction formed by dopant implantation into CoSi₂ and anneal," *IEEE Trans. Electron Devices*, vol. 47, pp. 994–998, May 2000.
- [5] C. G. Shirley and S. C. Maston, "Electrical measurements of moisture penetration through passivation," in *IEEE Proc. IRPS*, 1990, pp. 72–80.