

On the Architecture and Performance of a Hybrid Image Rejection Receiver

Chun-Chyuan Chen and Chia-Chi Huang

Abstract—This paper describes a hybrid image rejection receiver. The hybrid image rejection receiver contains a modified Hartley image rejection mixer and a digital image rejection processor. The modified Hartley image rejection mixer performs similarly to an original Hartley image rejection receiver but provides two digital outputs. In one output it enhances the desired signal, and in the other output it enhances the image signal. The digital image rejection processor first measures the mismatching effect in the analog devices and then suppresses the image signal by compensating for the mismatching effect. We also propose a simplified implementation method for the hybrid image rejection receiver to reduce its computation complexity. Computer simulation was used to evaluate the performance of this simplified implementation method to include the quantization effect introduced by the A/D converters. Simulation results show that the proposed hybrid image rejection receiver achieves much better performance than the original Hartley image rejection receiver. This architecture greatly relaxes the matching requirements of the analog devices and has a low complexity for an IC implementation.

Index Terms—Digital mismatch compensation, gain mismatch, hybrid image rejection receiver, low-IF, phase mismatch.

I. INTRODUCTION

THE CONTINUING evolution in both cellular mobile telephone services and personal communication services (PCS) demands small-size handsets at low cost [1], [2]. A monolithic RF module with a highly integrated transceiver architecture is required for fulfilling this purpose. Various transmitters designed with compact size and good performance have been proposed for different modulation schemes [3]–[5]. However, on the receiver side, it is still a major challenge to search for well-designed and highly integrated solutions [6].

Conventionally, three types of receiver architectures have been used: the heterodyne receiver architecture, the direct-conversion receiver architecture, and the low intermediate frequency (IF) receiver architecture. A heterodyne receiver architecture requires two or more local oscillators (LOs) and external filters, including a very high Q factor channel selection filter at a high frequency band. These filters are usually implemented with discrete components. Because a heterodyne receiver has good performance in its image rejection capability and channel selectivity, it has been used in most applications for a long time [7]. Nevertheless, this architecture is not suitable for a single-chip integrated circuit design.

A direct-conversion receiver architecture requires fewer discrete components and achieves a higher integration level

than other traditional receiver architectures [8]–[10]. Nevertheless, this architecture comes with several drawbacks [11]. For instance, DC-offset due to self-mixing and flicker noise near DC frequency in the devices substantially corrupt the baseband signal. Moreover, the mismatches between the in-phase and quadrature phase channels also distort the baseband signal constellation, thereby degrade the SNR performance. These I/Q mismatches can be reduced through a careful circuit design and fabrication procedure [12]. Nevertheless, both DC-offset and flicker noise problems are still difficult to deal with and require further efforts to overcome [13].

A low-IF receiver architecture can be implemented in a highly integrated way and is not sensitive to parasitic effects such as DC-offset voltages and self-mixing products. However, this architecture suffers severely from the image problem [14]. An image signal comes from an adjacent channel and cannot be totally removed by RF bandpass filtering. In 1928, Hartley introduced an image rejection receiver which has a similar structure as a single sideband (SSB) modulator [15]. The primary difficulty with Hartley's architecture is the serious degradation in its image rejection capability due to both gain and phase mismatches. For example, if the architecture needs to provide a 60 dB of image suppression, its phase mismatch between the in-phase and the quadrature phase channels must be maintained below 0.1° , even with no gain mismatch. This matching requirement is very difficult to meet in a typical IC design.

Many methods have been proposed to improve the matching issues in the low IF receiver architecture. Modifying the phase-shift circuit was proposed in [16]. Careful tuning and trimming in the analog circuits was introduced in [17]. A double quadrature downconverter makes the analog circuits more robust with respect to phase mismatch [18], [19]. Digital approaches for the correction of I/Q channel mismatch were presented in [20] and [21]. In [22], a complex least-mean-square algorithm and a modified adaptive noise cancellation model were used to compensate for the mismatching effect, which needed high computation power.

Conventional image rejection receiver architectures are implemented by analog circuit techniques. In this paper, we propose a hybrid analog and digital image rejection receiver architecture. Unlike conventional pure analog realizations, this architecture uses both analog and digital signal processing techniques to suppress the image signal. This architecture adopts a modified Hartley image rejection mixer and a digital image rejection processor. The modified Hartley image rejection mixer has performance similar to the original Hartley image rejection receiver but provides two digital outputs. In one output it enhances the desired signal, and in the other output it enhances the image signal.

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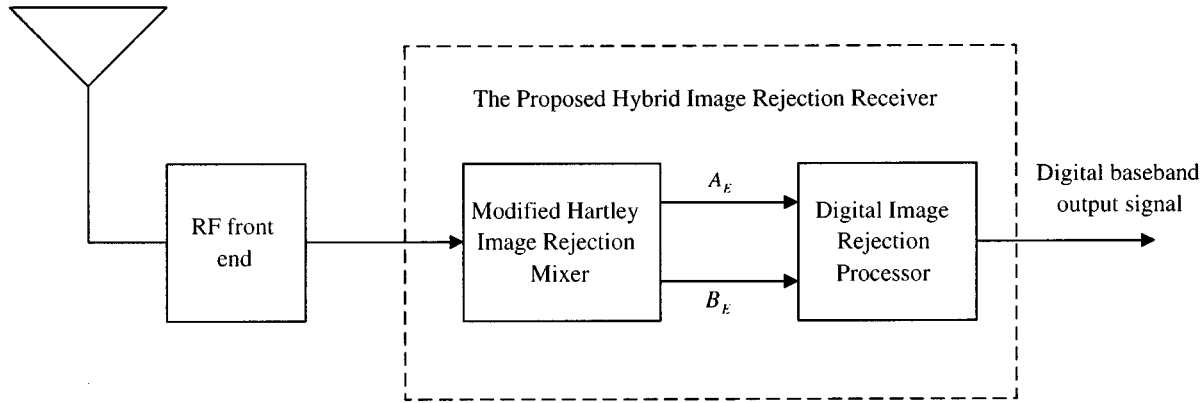


Fig. 1. A hybrid image rejection receiver system.

In the digital image rejection processor, this hybrid receiver first measures the I/Q mismatching effects in the analog devices and then suppresses the image signal digitally by compensating for the mismatching effects. The proposed architecture greatly relaxes the matching requirements for analog circuits and achieves a very high degree of image suppression capability.

In Section II, we describe the proposed hybrid image rejection receiver and derive its image rejection ratio (IRR) with mismatches in analog devices as parameters. In Section III, we describe a simplified implementation method for the proposed hybrid image rejection receiver architecture. Both the performance and the numerical accuracy of this architecture were evaluated by computer simulations and the simulation results are presented in Section IV. Finally, a conclusion is given in Section V.

II. A HYBRID IMAGE REJECTION RECEIVER ARCHITECTURE

In this section, we describe a hybrid image rejection receiver architecture. Its simplified block diagram is shown in Fig. 1. In this architecture, a radio frequency (RF) signal is received by an antenna and passed through an RF front end to generate a bandpass signal. The bandpass signal is then sent to a hybrid image rejection receiver to suppress the image signal.

The hybrid image rejection receiver can be divided into two parts. One part is a modified Hartley image rejection mixer, and the other part is a digital image rejection processor. The modified Hartley image rejection mixer generates two digital output signals A_E and B_E , where the signal A_E emphasizes on the desired signal and the signal B_E emphasizes on the image signal. The digital image rejection processor utilizes both the signal A_E and the signal B_E to achieve a much higher degree of image suppression.

In the following three subsections, we first describe the modified Hartley image rejection mixer. Then we introduce a single-stage image rejection processor. Next, we describe a multistage image rejection processor.

A. The Modified Hartley Image Rejection Mixer

The block diagram of the modified Hartley image rejection mixer is shown in Fig. 2. This mixer is a hybrid analog and digital circuit which is essentially an extended Hartley image rejection receiver. An RF input signal $\nu_{in}(t)$ is mixed with the two local

quadrature oscillator signals and down converted to a low IF band. After IF bandpass filtering, the lower arm signal is subject to a -90° phase shift with respect to the upper arm signal. The two bandpass A/D converters are used to generate two baseband digital signals through an IF sampling technique [23]. The digital output signal A_E is obtained by adding signals coming from both arms, and the digital output signal B_E is obtained by subtracting the lower arm signal from the upper arm signal.

Ideally, the output signal A_E will be the desired signal and the output signal B_E will be the image signal. Due to the mismatches in the analog devices, however, the signal A_E preserves the desired signal more than the image signal, and the signal B_E preserves the image signal more than the desired signal. To further understand the signal contents in A_E and B_E , we formulate them individually as follows.

Assume that an RF input signal $\nu_{in}(t)$ is represented by

$$\nu_{in}(t) = \Re\{S(t)e^{j\omega_s t}\} + \Re\{I(t)e^{j\omega_i t}\} \quad (1)$$

where $\Re\{\cdot\}$ is the real part notation. On the right side of the equation, the first term is the desired signal and the second term is the image signal. $S(t)$ and $I(t)$ are their equivalent baseband representations, and ω_s and ω_i are their carrier frequencies. In general, both $S(t)$ and $I(t)$ are complex and can be represented by

$$S(t) = x_s(t) + jy_s(t) \quad (2)$$

$$I(t) = x_i(t) + jy_i(t) \quad (3)$$

where $x_s(t)$ and $y_s(t)$ are the real and imaginary components of $S(t)$, and $x_i(t)$ and $y_i(t)$ are the real and imaginary components of $I(t)$. Without loss of generality, the mixing operation is assumed to be of a low-side injection type. This implies $\omega_s - \omega_{Lo} = \omega_{Lo} - \omega_i = \omega_{IF}$, where ω_{Lo} is the local oscillator frequency and ω_{IF} is a low IF frequency.

Multiplying the signal $\nu_{in}(t)$ by the local oscillator in-phase signal and neglecting the high frequency components, we obtain the signal v_A as

$$\begin{aligned} v_A &= \frac{1}{2}x_s(t)\cos\omega_{IF}t - \frac{1}{2}y_s(t)\sin\omega_{IF}t + \frac{1}{2}x_i(t) \\ &\quad \cdot \cos\omega_{IF}t + \frac{1}{2}y_i(t)\sin\omega_{IF}t \\ &= \Re\left\{\left[\left(\frac{1}{2}x_s(t) + \frac{1}{2}x_i(t)\right) + j \cdot \left(\frac{1}{2}y_s(t) - \frac{1}{2}y_i(t)\right)\right] \cdot e^{j\omega_{IF}t}\right\}. \end{aligned} \quad (4)$$

Assume the gain mismatch and phase mismatch between the lower arm and the upper arm are represented by m and θ , respectively. We multiply the signal $\nu_{in}(t)$ by $m \cdot \cos(\omega_{Lo}t - 90^\circ - \theta)$

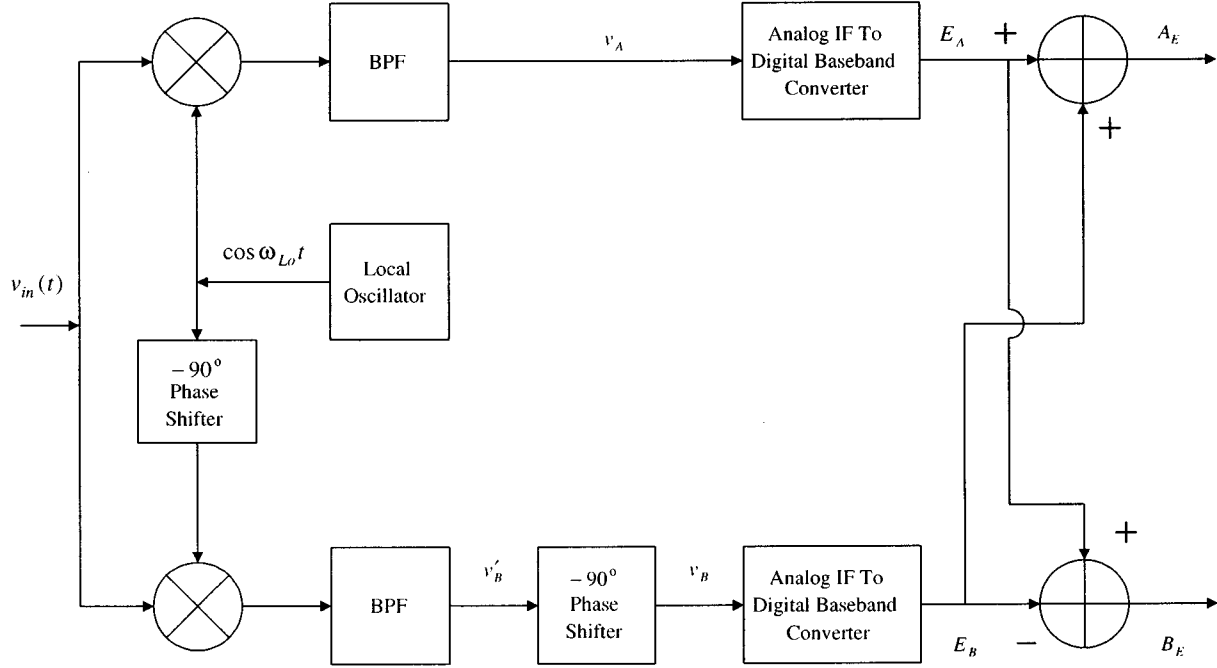


Fig. 2. The modified Hartley image rejection mixer.

and neglect the high frequency components to obtain the signal v'_B as

$$v'_B = \frac{1}{2}mx_s(t)\cos(\omega_{IF}t + 90^\circ + \theta) - \frac{1}{2}my_s(t) \cdot \sin(\omega_{IF}t + 90^\circ + \theta) + \frac{1}{2}mx_i(t)\cos(\omega_{IF}t - 90^\circ - \theta) + \frac{1}{2}my_i(t)\sin(\omega_{IF}t - 90^\circ - \theta). \quad (5)$$

After applying an additional -90° phase shift, we obtain the signal v_B as

$$v_B = \frac{1}{2}mx_s(t)\cos(\omega_{IF}t + \theta) - \frac{1}{2}my_s(t)\sin(\omega_{IF}t + \theta) - \frac{1}{2}mx_i(t)\cos(\omega_{IF}t - \theta) - \frac{1}{2}my_i(t)\sin(\omega_{IF}t - \theta) = \frac{1}{2} \cdot \Re\{[(mx_s(t)\cos\theta - my_s(t)\sin\theta) + j \cdot (mx_s(t)\sin\theta + my_s(t)\cos\theta) + (-mx_i(t)\cos\theta + my_i(t)\sin\theta) + j \cdot (mx_i(t)\sin\theta + my_i(t)\cos\theta)]e^{j\omega_{IF}t}\}. \quad (6)$$

From (4) and (6), we observe the discrete-time equivalent baseband signals E_A and E_B in both arms are

$$E_A = \frac{1}{2} \cdot [(x_s(n) + x_i(n)) + j \cdot (y_s(n) - y_i(n))] \quad (7)$$

$$E_B = \frac{1}{2} \cdot [(mx_s(n)\cos\theta - my_s(n)\sin\theta) + (-mx_i(n)\cos\theta + my_i(n)\sin\theta)] + \frac{1}{2}j \cdot [(mx_s(n)\sin\theta + my_s(n)\cos\theta) + (mx_i(n)\sin\theta + my_i(n)\cos\theta)] \quad (8)$$

where n is the discrete-time index. Finally, the output signals A_E and B_E can be calculated as

$$\begin{aligned} A_E &= E_A + E_B \\ &= \frac{1}{2} \cdot [(x_s(n) + mx_s(n)\cos\theta - my_s(n)\sin\theta) + x_i(n) - mx_i(n)\cos\theta + my_i(n)\sin\theta] \\ &\quad + j \cdot [(y_s(n) + my_s(n)\cos\theta + mx_s(n)\sin\theta) - y_i(n) + my_i(n)\cos\theta + mx_i(n)\sin\theta] \\ &= h_1S(n) + h_2I^*(n) \end{aligned} \quad (9)$$

$$B_E = E_A - E_B$$

$$\begin{aligned} &= \frac{1}{2} \cdot [(x_s(n) - mx_s(n)\cos\theta + my_s(n)\sin\theta) + x_i(n) - mx_i(n)\cos\theta - my_i(n)\sin\theta] \\ &\quad + j \cdot [(y_s(n) - my_s(n)\cos\theta - mx_s(n)\sin\theta) - y_i(n) - my_i(n)\cos\theta - mx_i(n)\sin\theta] \\ &= h_2^*S(n) + h_1^*I^*(n) \end{aligned} \quad (10)$$

where

$$\begin{aligned} h_1 &= (\frac{1}{2} + \frac{1}{2}m\cos\theta) + j \cdot \frac{1}{2}m\sin\theta \\ h_2 &= (\frac{1}{2} - \frac{1}{2}m\cos\theta) + j \cdot \frac{1}{2}m\sin\theta. \end{aligned}$$

We observe from (9) that the gain for the desired signal is h_1 and the gain for the image signal is h_2 . On the other hand, we observe from (10) that the gain for the desired signal is h_2^* and the gain for the image signal is h_1^* . In general, $|h_1| > |h_2|$ as m approaches 1 and θ approaches 0. Thus, the output signal A_E emphasizes the desired signal, and the output signal B_E emphasizes the image signal.

To examine the performance of this mixer, we define the image rejection ratio (IRR) as the ratio between the output “desired signal to image signal power ratio” and the input “desired signal to image signal power ratio.” From (9), we can calculate the IRR for the signal A_E as

$$\begin{aligned} \text{IRR}_{A_E} &= \frac{(|h_1|^2 \cdot E[|S(n)|^2]) / (|h_2|^2 \cdot E[|I(n)|^2])}{E[|S(n)|^2] / E[|I(n)|^2]} \\ &= \frac{|h_1|^2}{|h_2|^2} \\ &= \frac{m^2 + 2 \cdot m\cos\theta + 1}{m^2 - 2 \cdot m\cos\theta + 1}. \end{aligned} \quad (11)$$

Note that IRR_{A_E} has the same performance as that of an original Hartley image rejection receiver [14].

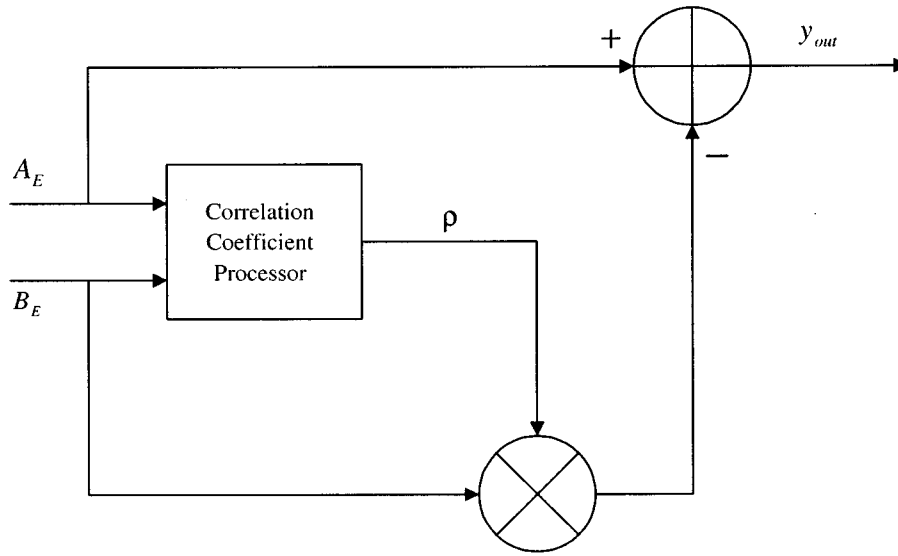


Fig. 3. The single-stage image rejection processor.

B. The Single-Stage Image Rejection Processor

To enhance the IRR performance of the modified Hartley image rejection mixer, the mismatching effects in the analog devices must be compensated digitally. In the digital image rejection processor, we compensate for the mismatches by eliminating the image signal component in the output signal A_E of the modified Hartley image rejection mixer.

The block diagram of a single-stage image rejection processor is shown in Fig. 3. This processor contains a correlation coefficient processor, a multiplier, and a subtractor. First, the correlation coefficient processor measures the mismatching effects in the analog devices by calculating a modified correlation coefficient ρ between the two signals A_E and B_E . Assume the desired signal $S(t)$ and the image signal $I(t)$ are uncorrelated and have zero means, from (9) and (10) we get

$$E[A_E B_E^*] = E[(h_1 S(n) + h_2 I^*(n))(h_2 S^*(n) + h_1 I(n))] \\ = h_1 h_2 E[|S(n)|^2] + h_1 h_2 E[|I(n)|^2]$$

$$E[|A_E|^2] = E[(h_1 S(n) + h_2 I^*(n))(h_1^* S^*(n) + h_2^* I(n))] \\ = |h_1|^2 E[|S(n)|^2] + |h_2|^2 E[|I(n)|^2]$$

$$E[|B_E|^2] = E[(h_2^* S(n) + h_1^* I^*(n))(h_2 S^*(n) + h_1 I(n))] \\ = |h_2|^2 E[|S(n)|^2] + |h_1|^2 E[|I(n)|^2]$$

where $E[\cdot]$ is the expectation notation [24]. The modified correlation coefficient ρ is defined and computed as

$$\rho = \frac{E[A_E B_E^*]}{E[|A_E|^2] + E[|B_E|^2]} \\ = \frac{h_1 h_2 (E[|S(n)|^2] + E[|I(n)|^2])}{(|h_1|^2 + |h_2|^2)(E[|S(n)|^2] + E[|I(n)|^2])} \\ = \frac{h_1 h_2}{|h_1|^2 + |h_2|^2}. \quad (12)$$

Note that ρ depends only on the mismatches in the analog devices.

We estimate the image signal component within the signal A_E by multiplying the input signal B_E with the correlation coefficient ρ . Then, we subtract the estimated image signal com-

ponent from the input signal A_E to obtain the output signal y_{out} . From (9), (10), and (12), we get

$$y_{out} = A_E - \rho \cdot B_E \\ = \frac{h_1 |h_1|^2}{|h_1|^2 + |h_2|^2} \cdot S(n) + \frac{h_2 |h_2|^2}{|h_1|^2 + |h_2|^2} \cdot I^*(n). \quad (13)$$

Although this subtraction attenuates the desired signal, it suppresses much more the image signal. The IRR performance for the output signal y_{out} can now be calculated as

$$\text{IRR}_{y_{out}} = \frac{\left| \frac{h_1 |h_1|^2}{|h_1|^2 + |h_2|^2} \right|^2}{\left| \frac{h_2 |h_2|^2}{|h_1|^2 + |h_2|^2} \right|^2} = \frac{|h_1|^6}{|h_2|^6}. \quad (14)$$

After cascading a single-stage image rejection processor with a modified Hartley image rejection mixer, we obtain an overall IRR for the output signal y_{out} as the cube of the IRR that can be achieved by using the modified Hartley image rejection mixer alone [see (11)].

C. The Multistage Image Rejection Processor

To improve the IRR performance, we introduce a multi-stage image rejection processor. Its simplified block diagram is shown in Fig. 4. We observe that multiple stages of digital desired/image signal separators are cascaded with a single-stage image rejection processor to make a multistage image rejection processor. Each stage of digital desired/image signal separator is used to further separate desired signal from image signal, and vice versa. Theoretically, we can obtain better and better IRR performance by cascading more and more stages of the digital desired/image signal separators with a final stage of single-stage image rejection processor.

Fig. 5 shows the block diagram of a digital desired/image signal separator. This device is a modification from a single-stage image rejection processor. In this device, the correlation coefficient processor is the same as the one in the single-stage image rejection processor. In addition to the original output signal A_{out} , an extra output signal B_{out} is generated to enhance

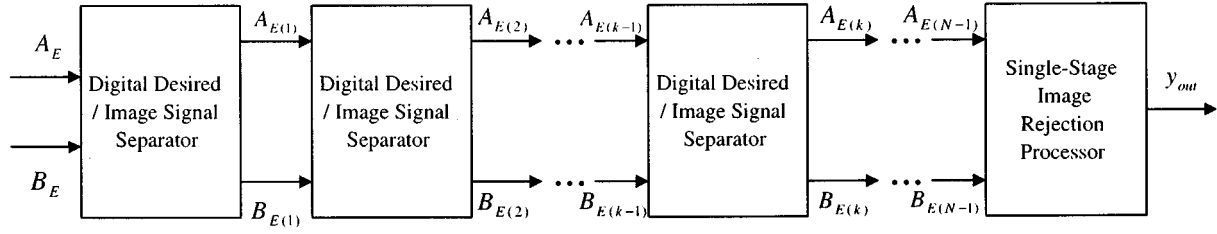


Fig. 4. The multistage image rejection processor.

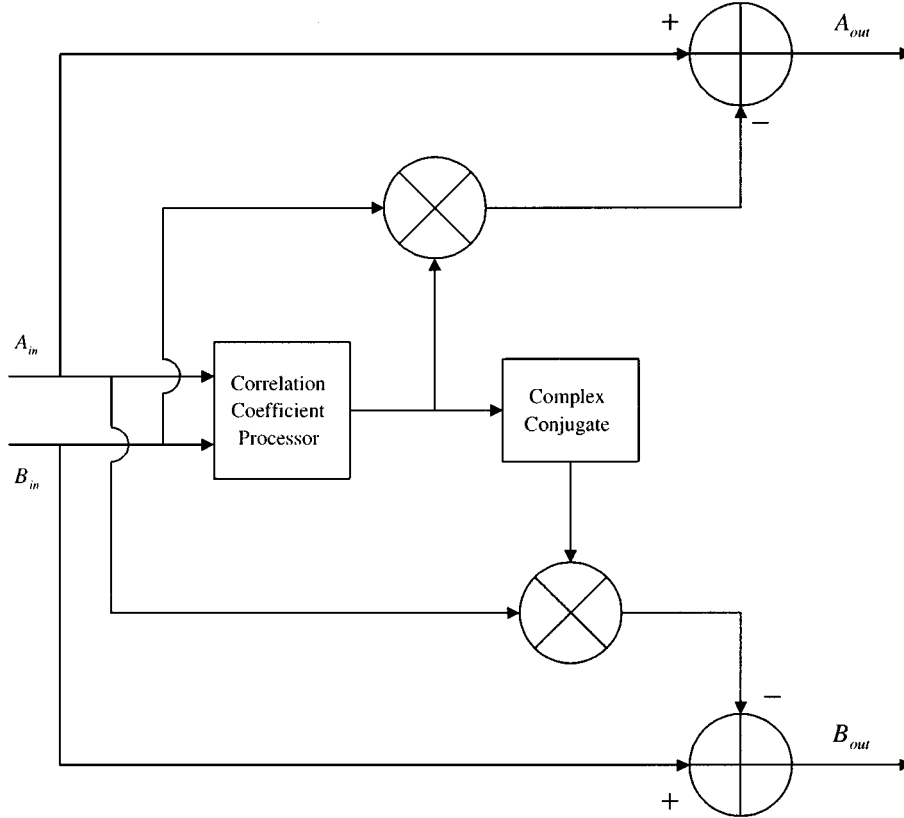


Fig. 5. Digital desired/image signal separator.

the image signal for the next stage input. To examine the function of this device, we derive the output signals A_{out} and B_{out} below. Let $A_{in} = A_E$, $B_{in} = B_E$, $A_{out} = A_E^{(1)}$, and $B_{out} = B_E^{(1)}$. From (13), we can directly calculate the first stage output signal $A_E^{(1)}$ as

$$\begin{aligned} A_E^{(1)} &= A_E - \frac{E[A_E B_E^*]}{E[|A_E|^2] + E[|B_E|^2]} \times B_E \\ &= \frac{h_1 |h_1|^2}{|h_1|^2 + |h_2|^2} \cdot S(n) + \frac{h_2 |h_2|^2}{|h_1|^2 + |h_2|^2} \cdot I^*(n). \end{aligned} \quad (15)$$

Reversing the order of A_E and B_E and applying the complex conjugate of the correlation coefficient, we can calculate the first stage output signal $B_E^{(1)}$ as

$$\begin{aligned} B_E^{(1)} &= B_E - \frac{E[A_E B_E^*]^*}{E[|A_E|^2] + E[|B_E|^2]} \times A_E \\ &= \frac{h_2^* |h_2|^2}{|h_1|^2 + |h_2|^2} \cdot S(n) + \frac{h_1^* |h_1|^2}{|h_1|^2 + |h_2|^2} \cdot I^*(n). \end{aligned} \quad (16)$$

Now we can rewrite (15) and (16) as

$$A_E^{(1)} = H_a^{(1)} S(n) + H_b^{(1)} I^*(n) \quad (17)$$

$$B_E^{(1)} = H_b^{*(1)} S(n) + H_a^{*(1)} I^*(n) \quad (18)$$

where

$$H_a^{(1)} = \frac{h_1 |h_1|^2}{|h_1|^2 + |h_2|^2} \quad \text{and} \quad H_b^{(1)} = \frac{h_2 |h_2|^2}{|h_1|^2 + |h_2|^2}.$$

Since $|H_a^{(1)}|/|H_b^{(1)}| > |h_1|/|h_2|$, the output signal $A_E^{(1)}$ preserves more desired signal as compared with its input signal A_E , and the output signal $B_E^{(1)}$ preserves more image signal as compared with its input signal B_E . In a similar way, we can derive the output signals $A_E^{(2)}$ and $B_E^{(2)}$ for the second stage of the digital desired/image signal separator as

$$A_E^{(2)} = H_a^{(2)} S(n) + H_b^{(2)} I^*(n) \quad (19)$$

$$B_E^{(2)} = H_b^{*(2)} S(n) + H_a^{*(2)} I^*(n) \quad (20)$$

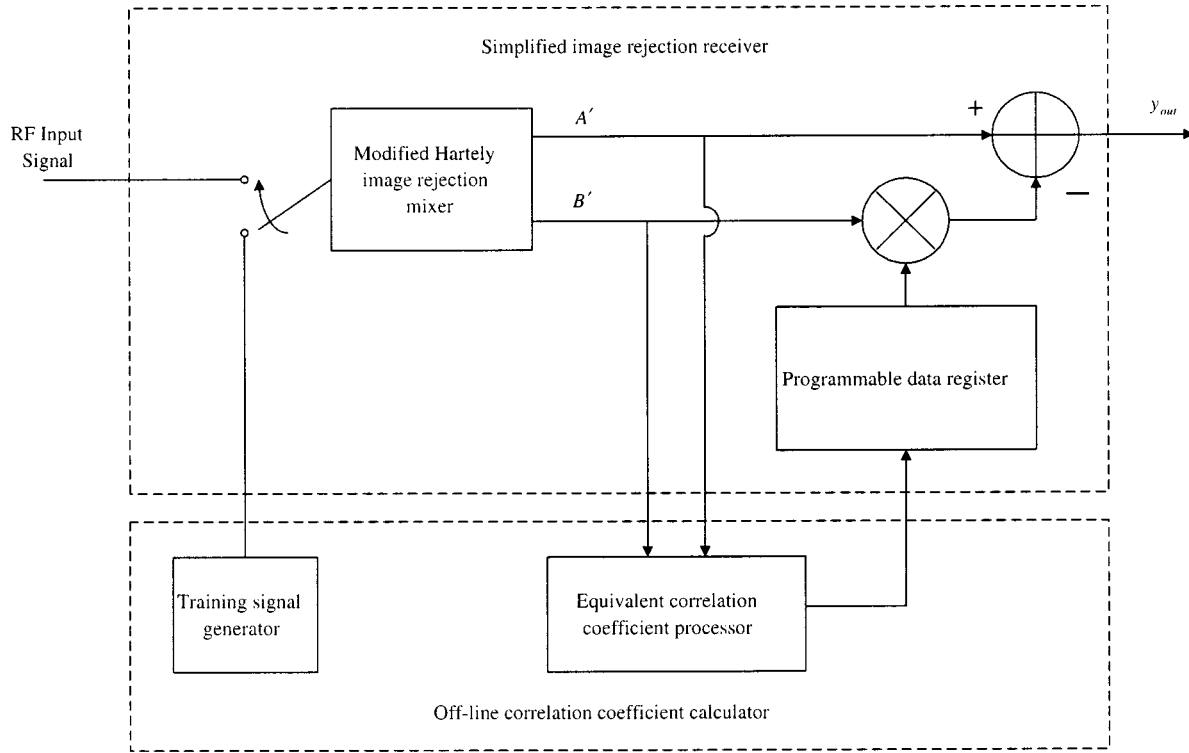


Fig. 6. A simplified implementation method for the proposed receiver.

where

$$H_a^{(2)} = \frac{H_a^{(1)} |H_a^{(1)}|^2}{|H_a^{(1)}|^2 + |H_b^{(1)}|^2}$$

and

$$H_b^{(2)} = \frac{H_b^{(1)} |H_b^{(1)}|^2}{|H_a^{(1)}|^2 + |H_b^{(1)}|^2}.$$

In a similar way, we can achieve better separation between the desired signal and the image signal by cascading more and more stages of digital desired/image signal separators. Finally, a single-stage image rejection processor is used to further eliminate the image signal and obtain the final output signal y_{out} .

From (17) and (18), we observe that the IRR for the output signal is the cube of the IRR for the input signal for each stage of the digital desired/image signal separator. We can calculate the overall IRR for the output signal y_{out} of the multistage image rejection processor as

$$IRR_{y_{out}} = P_r \times 3^N \quad (\text{dB}) \quad (21)$$

where P_r is the IRR of the modified Hartley image rejection mixer in dB scale, and N is the number of stages (including the final stage) in the multistage image rejection processor. A multistage image rejection processor requires higher computation power than a single-stage image rejection processor, but it greatly enhances the IRR performance.

III. A SIMPLIFIED IMPLEMENTATION METHOD FOR THE PROPOSED RECEIVER ARCHITECTURE

The image rejection receiver architecture we described above utilizes digital signal processing techniques to enhance the IRR performance. Extra computations, such as correlation coefficient calculations, are needed to implement the architecture. In this section, we propose a simplified implementation method for this receiver architecture to reduce its computation requirements. Here, we assume the mismatching effects in the analog devices are fixed such that the computation of the correlation coefficients can be done in an off-line processor.

Fig. 6 shows the block diagram of the simplified implementation method. The architecture now contains a simplified image rejection receiver and an off-line correlation coefficient calculator. The simplified image rejection receiver consists of a modified Hartley image rejection mixer, a programmable data register, a multiplier, and a subtractor. The off-line correlation coefficient calculator includes a training signal generator and an equivalent correlation coefficient processor. This implementation method operates in a training mode and a receiving mode separately. In the training mode, the training signal generator generates a desired signal and an image signal simultaneously, and sends them to the modified Hartley image rejection mixer. The desired signal and the image signal are assumed to be uncorrelated. The two output signals of the modified Hartley image rejection mixer are then sent to the equivalent correlation coefficient processor to calculate an equivalent correlation coefficient. To understand the meaning of the equivalent correlation coefficient, we reformulate the correlation coefficient for each stage of the multistage image rejection processor.

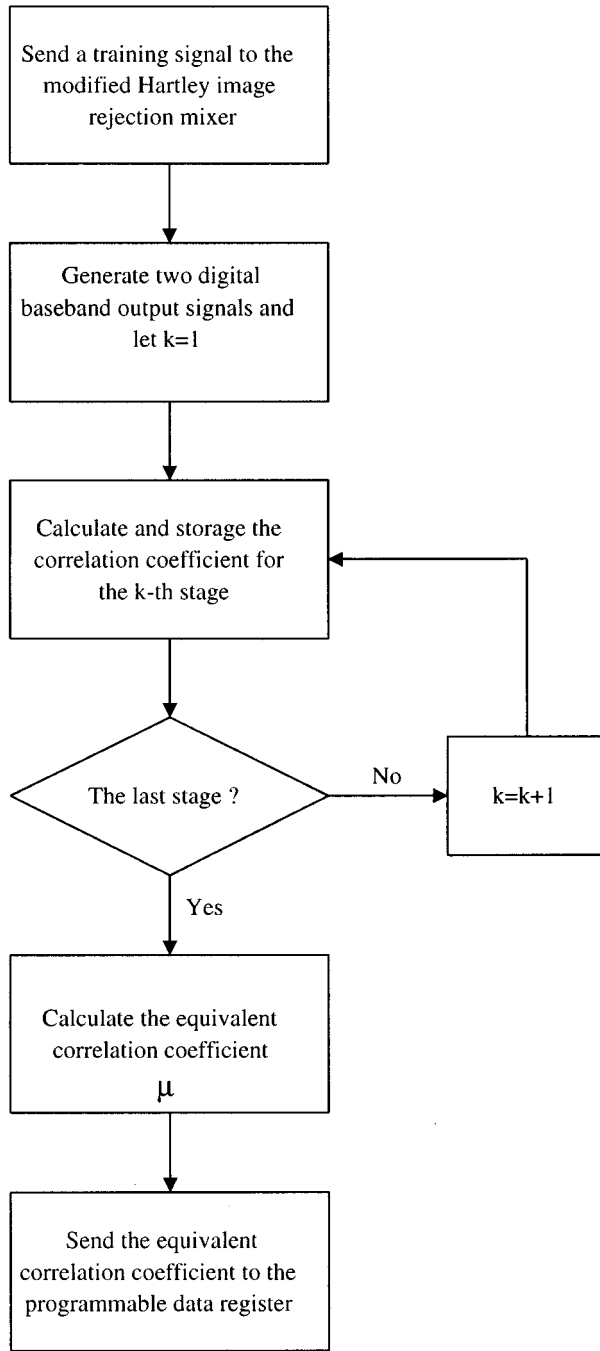


Fig. 7. The flow chart for the training mode.

From (15) and (16), the signals $A_E^{(1)}$ and $B_E^{(1)}$ can be represented in a matrix form as

$$\begin{bmatrix} A_E^{(1)} \\ B_E^{(1)} \end{bmatrix} = \begin{bmatrix} 1 & -\rho_0 \\ -\rho_0^* & 1 \end{bmatrix} \cdot \begin{bmatrix} A_E \\ B_E \end{bmatrix} \quad (22)$$

where ρ_0 is the correlation coefficient and

$$\rho_0 = \frac{E[A_E B_E^*]}{E[|A_E|^2] + E[|B_E|^2]}. \quad (23)$$

Through substitution, we can reformulate the second stage correlation coefficient of the multistage image rejection processor as

$$\rho_1 = \frac{E[A_E^{(1)} B_E^{*(1)}]}{E[|A_E^{(1)}|^2] + E[|B_E^{(1)}|^2]} = \frac{\epsilon}{\xi} \quad (24)$$

where

$$\begin{aligned} \epsilon &= E[A_E^{(1)} B_E^{*(1)}] \\ &= E[(A_E - \rho_0 \cdot B_E)(B_E^* - \rho_0^* \cdot A_E^*)] \\ &= E[A_E B_E^*] - \rho_0 \cdot (E[|A_E|^2] + E[|B_E|^2]) \\ &\quad + \rho_0^2 \cdot E[A_E^* B_E] \end{aligned}$$

and

$$\begin{aligned} \xi &= E[|A_E^{(1)}|^2] + E[|B_E^{(1)}|^2] \\ &= E[(A_E - \rho_0 \cdot B_E)(A_E^* - \rho_0^* \cdot B_E^*)] \\ &\quad + E[(B_E - \rho_0^* \cdot A_E)(B_E^* - \rho_0 \cdot A_E^*)] \\ &= (1 + |\rho_0|^2)(E[|A_E|^2] + E[|B_E|^2]) \\ &\quad - 2\rho_0 \cdot E[A_E^* B_E] - 2\rho_0^* \cdot E[A_E B_E^*]. \end{aligned}$$

Substituting (23) to (24), we can obtain ρ_1 as

$$\rho_1 = \frac{\rho_0 \cdot |\rho_0|^2}{1 - 3 \cdot |\rho_0|^2}. \quad (25)$$

In a similar way, we can deduce that the n th stage correlation coefficient can be represented by the $(n-1)$ th stage correlation coefficient as

$$\rho_n = \frac{\rho_{(n-1)} \cdot |\rho_{(n-1)}|^2}{1 - 3 \cdot |\rho_{(n-1)}|^2}. \quad (26)$$

After computing the correlation coefficient for each stage, we can calculate an equivalent correlation coefficient for a multi-stage image rejection processor.

Consider an N -stage image rejection processor, the output signal $A_{E(N)}$ of the N th stage can be represented as

$$\begin{aligned} A_{E(N)} &= \begin{bmatrix} 1 & -\rho_{N-1} \end{bmatrix} \cdot \begin{bmatrix} A_E^{(N-1)} \\ B_E^{(N-1)} \end{bmatrix} \\ &= \begin{bmatrix} 1 & -\rho_{N-1} \end{bmatrix} \cdot \begin{bmatrix} 1 & -\rho_{N-2} \\ -\rho_{N-2}^* & 1 \end{bmatrix} \\ &\quad \cdots \begin{bmatrix} 1 & -\rho_0 \\ -\rho_0^* & 1 \end{bmatrix} \cdot \begin{bmatrix} A_E \\ B_E \end{bmatrix} \\ &= [\phi_1 \ \phi_2] \cdot \begin{bmatrix} A_E \\ B_E \end{bmatrix} \\ &= \Phi \cdot \begin{bmatrix} A_E \\ B_E \end{bmatrix} \end{aligned} \quad (27)$$

where $\rho_0, \rho_1, \dots, \rho_{N-2}, \rho_{N-1}$ are the correlation coefficients of all the stages and Φ is defined as an equivalent correlation matrix, which is represented by

$$\begin{aligned} \Phi &= [\phi_1 \ \phi_2] \\ &= \begin{bmatrix} 1 & -\rho_{N-1} \end{bmatrix} \cdot \begin{bmatrix} 1 & -\rho_{N-2} \\ -\rho_{N-2}^* & 1 \end{bmatrix} \\ &\quad \cdots \begin{bmatrix} 1 & -\rho_0 \\ -\rho_0^* & 1 \end{bmatrix}. \end{aligned} \quad (28)$$

TABLE I
SIMULATION PARAMETERS

Resolution of the A/D converters, M	8, 10, 12 bits
Number of stages (including the final stage), N	1 ~ 7
Phase mismatch, θ	$0^\circ \sim 76^\circ$
Gain mismatch, m	0.5 dB ~ 10 dB
Input "desired signal to image signal power ratio", α_{in}	0 dB ~ -95 dB

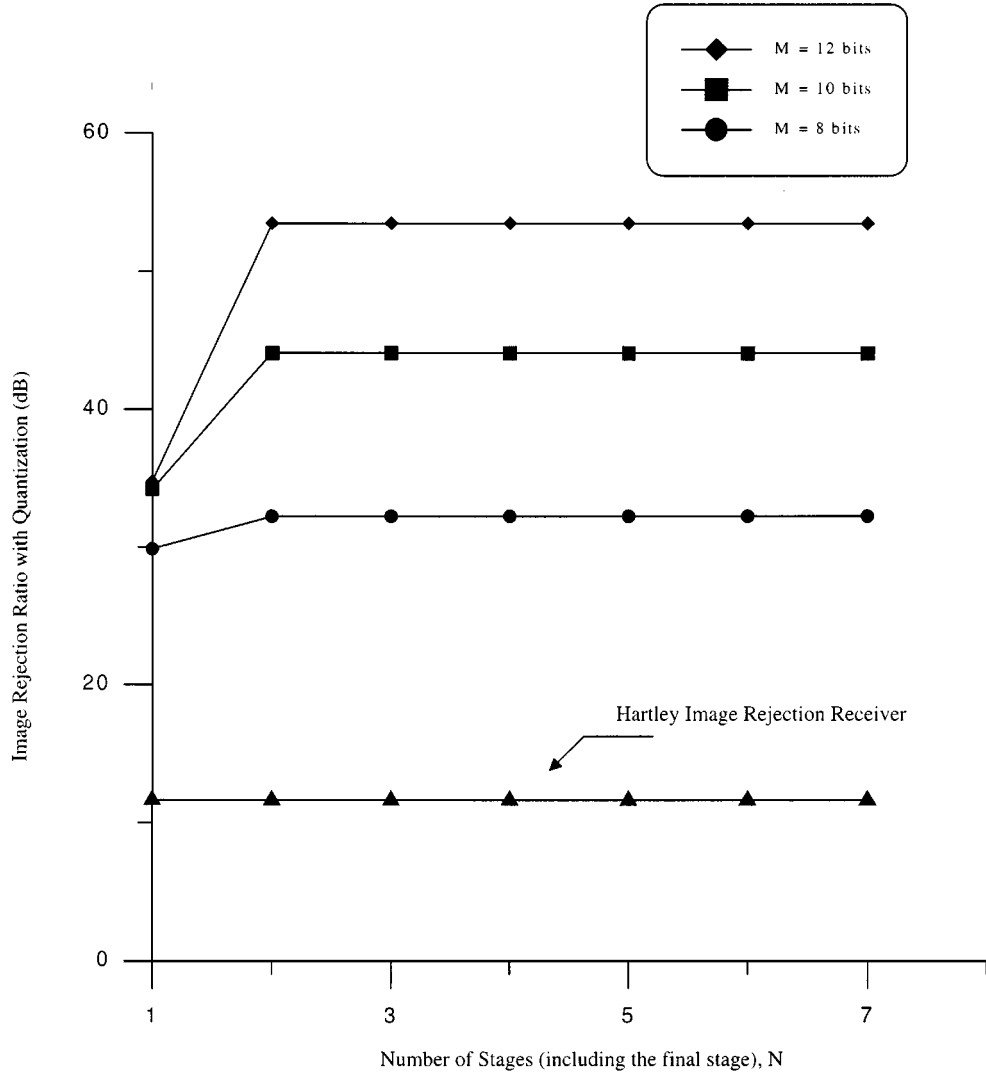


Fig. 8. Image rejection ratio performance at different A/D resolutions ($\alpha_{in} = 0$ dB, $m = 2$ dB, and $\theta = 15^\circ$).

Both ϕ_1 and ϕ_2 are functions of ρ_0 according to (26), and we define the equivalent correlation coefficient μ as

$$\mu \equiv -\frac{\phi_2}{\phi_1}. \quad (29)$$

After the equivalent correlation coefficient μ is computed, we send it to the programmable data register (see Fig. 6) and complete the training mode operation. The training mode operation can be understood in more detail by examining the flow chart shown in Fig. 7. This whole training process can be done as an off-line procedure.

In the receiving mode, an RF input signal is received from an antenna and goes through the modified Hartley image rejection

mixer to obtain two digital output signals, A' and B' . We subtract the signal A' from the product of the signal B' and the stored equivalent correlation coefficient μ to obtain the output signal y_{out} , i.e.,

$$y_{out} = A' - \mu \cdot B'. \quad (30)$$

According to the analysis we have done above for the training mode, the IRR performance of the output signal y_{out} in Fig. 6 is equivalent to that of a multistage image rejection processor. The simplified implementation method eliminates most of the computations by calculating an equivalent correlation coefficient. This can be done when the receiver is being manufactured. In practical implementation, the mismatches in the analog

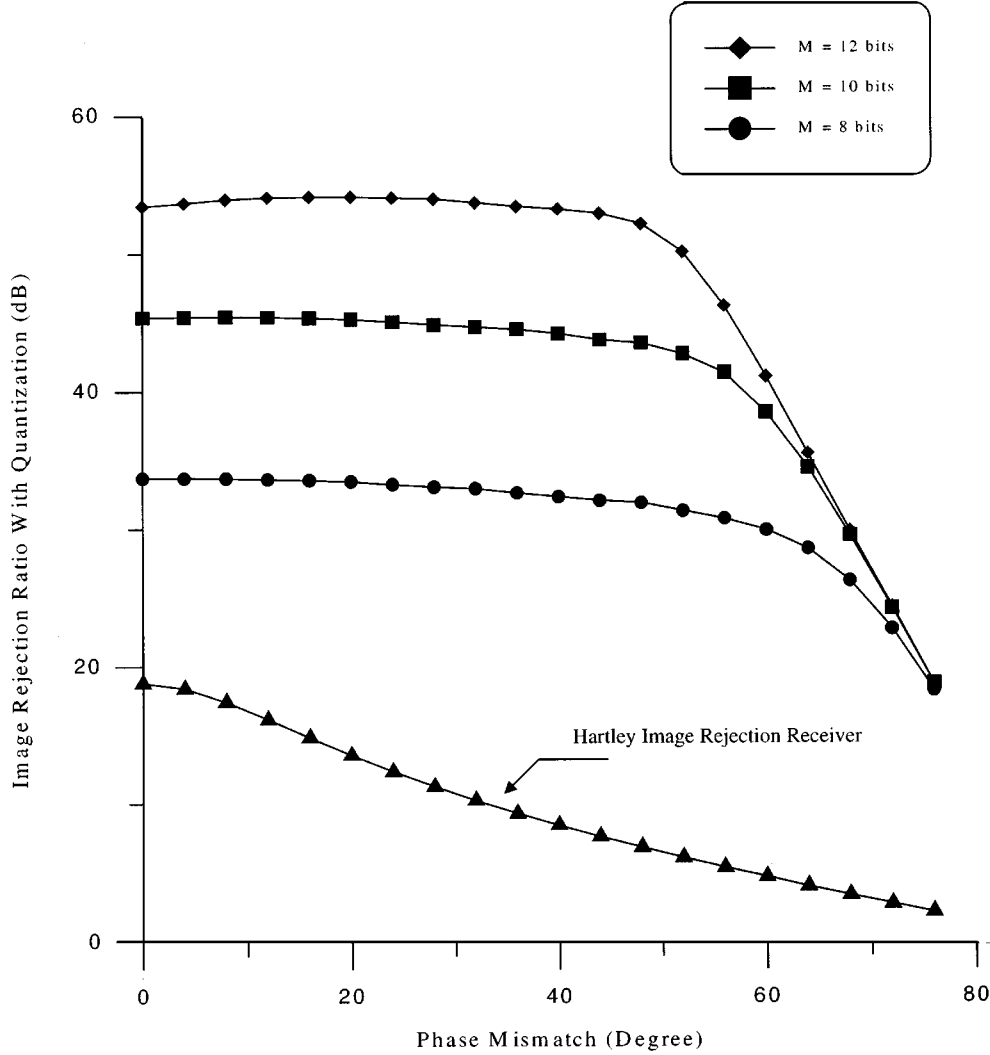


Fig. 9. Image rejection ratio performance at different A/D resolutions ($N = 2$, $\alpha_{in} = 0$ dB, and $m = 1$ dB).

devices might be a function of frequency and temperature. In such a case, we can calibrate the receiver system at a different frequency and temperature in advance. In real system operation, we can dynamically adjust the equivalent correlation coefficient if we can closely monitor the variations in frequency and temperature.

IV. PERFORMANCE VERIFICATION BY SIMULATION

The performance of the hybrid image rejection receiver was evaluated by computer simulation. The quantization effect introduced by the A/D converters [25] was included in our evaluation. The simplified implementation method for the proposed image rejection receiver as shown in Fig. 6 was adopted in our simulation.

A. Simulation Method and Parameters

In our simulation, we assume the input signals are two complex tones in the training mode and two complex Gaussian signals in the receiving mode, respectively. In the training mode, the desired signal $S_T(t)$ and the image signal $I_T(t)$ are assumed

to be complex baseband sinusoidal signals with frequency 2 kHz and 3 kHz, that is,

$$S_T(t) = \cos(2\pi \cdot 2 \times 10^3 t) + j \cdot \sin(2\pi \cdot 2 \times 10^3 t)$$

$$I_T(t) = \cos(2\pi \cdot 3 \times 10^3 t) + j \cdot \sin(2\pi \cdot 3 \times 10^3 t).$$

In the receiving mode, the desired signal $S_R(t)$ and the image signal $I_R(t)$ are assumed to be complex baseband signals where

$$S_R(t) = n_{c1}(t) + j \cdot n_{s1}(t)$$

$$I_R(t) = n_{c2}(t) + j \cdot n_{s2}(t)$$

where $n_{c1}(t)$, $n_{s1}(t)$, $n_{c2}(t)$, and $n_{s2}(t)$ are independently generated Gaussian signals. Other simulation parameters are given in Table I. In order to investigate the improvement of the IRR performance in cascading a multistage image rejection processor, the number N of stages of the multistage image rejection processor was varied from 1 to 7. The phase mismatch parameter θ and the gain mismatch parameter m were used to model the imbalance of the two arms (see Fig. 2). Due to the mismatches in the two arms, the input signal power to the A/D converters is different in general. Without loss of generality, we assume the signal power in the lower arm is stronger than

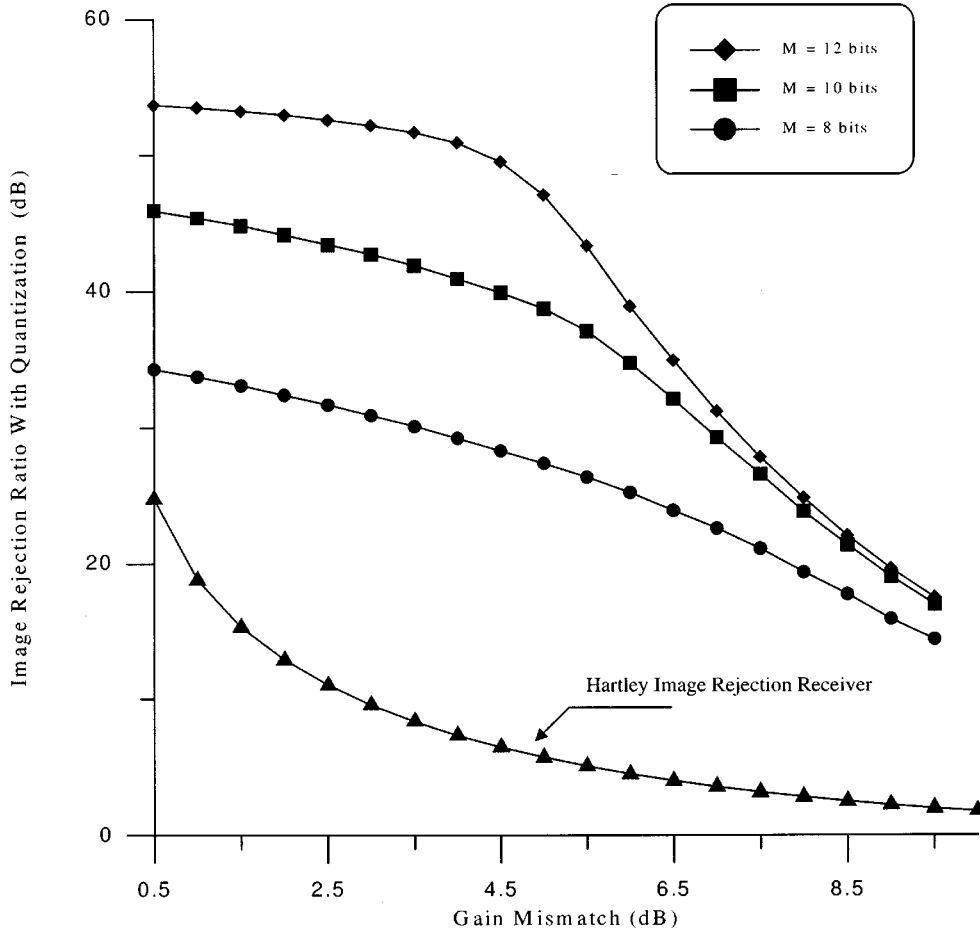


Fig. 10. Image rejection ratio performance at different A/D resolutions ($N = 2$, $\alpha_{in} = 0$ dB, and $\theta = 1^\circ$).

the signal power in the upper arm. In order to minimize the quantization distortion, we normalize the input signals to fit in the dynamic range of the A/D converters according to the signal power in the lower arm. With the complex sinusoidal input signals, the input signals to the A/D converters were limited by the maximum magnitude of the input signal in the lower arm. With the complex Gaussian input signals, the input signals to the A/D converters were limited by three times of the standard deviation of the input signal in the lower arm. In the training mode, the input “desired signal to image signal power ratio” parameter α_{in} was set to 0 dB. In the receiving mode, the input “desired signal to image signal power ratio” parameter α_{in} was varied within the range as shown in Table I.

Including the quantization effect, the output signal y_{out} of the proposed receiver can be represented as

$$y_{out} = y_d + y_{im} + Q_n \quad (31)$$

where y_d is the desired signal component, y_{im} is the image signal component, both from floating-point calculation, and Q_n is the overall quantization noise. From (30), (9), and (10), the desired signal component y_d can be calculated as $y_d = (h_1 - \mu \cdot h_2^*) \cdot S(n)$ by replacing A' and B' with A_E and B_E . We define an image rejection ratio (IRR) with quantization noise as

$$IRR \equiv 10 \log \left(\frac{E[|y_d|^2]}{E[|y_{out} - y_d|^2]} \right) - \alpha_{in} \quad (\text{dB}). \quad (32)$$

This IRR measure is used to evaluate the performance of the proposed image rejection receiver in our simulation.

B. Simulation Results

To examine the quantization effect on the IRR performance, we simulated the simplified implementation method at 8, 10, and 12 bits resolutions of the A/D converters. Fig. 8 shows the simulated IRR performance versus the number of stages (including the final stage) N . In this simulation, the input “desired signal to image signal power ratio” α_{in} was set to 0 dB. The gain mismatch and the phase mismatch were set to 2 dB and 15° , respectively. The IRR performance of the original Hartley image rejection receiver, which is computed by (10), is also shown for comparison purpose. When the number of stages is one ($N = 1$), we observe that the IRR of our receiver is nearly three times the IRR (in dB scale) obtainable from the original Hartley image rejection receiver, which agrees with (21). As the number of stages increases, the IRR performance improves and remains a constant when the number of stages exceeds two. In addition, we observe that the IRR performance becomes better and better as the bit resolution increases.

Fig. 9 shows the simulated IRR performance versus phase mismatches. Here, the number of stages (N) was set to 2. The input “desired signal to image signal power ratio” α_{in} was set to 0 dB and the gain mismatch was set to 1 dB. We observe from this figure that the IRR performance of our receiver is much

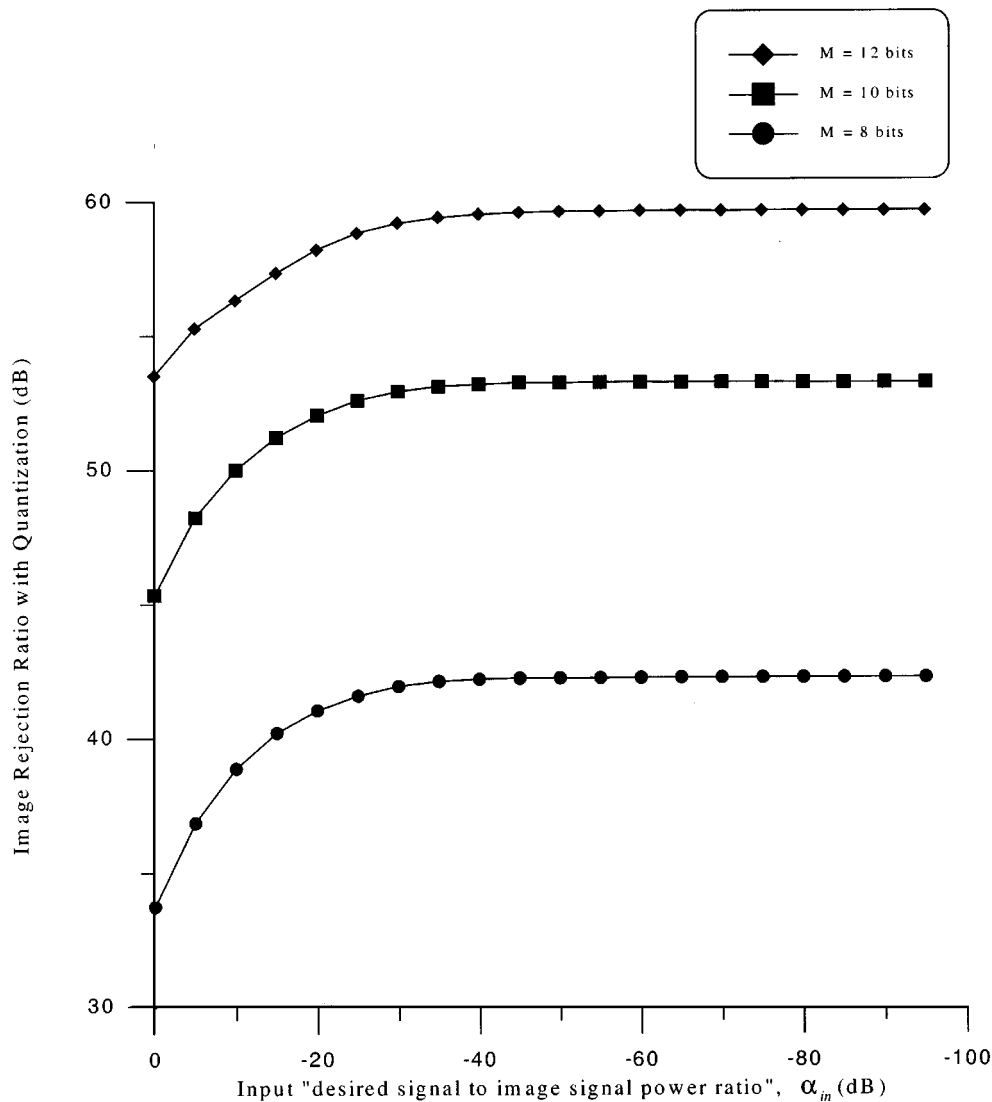


Fig. 11. Image rejection ratio performance at different A/D resolutions ($N = 2$, $\theta = 1^\circ$, and $m = 1$ dB).

better than the original Hartley image rejection receiver. The IRR performance also becomes better as the bit resolution increases. In addition, IRR does not vary much until the phase mismatch exceeds about 40° .

Fig. 10 shows the simulated IRR performance versus gain mismatches and the IRR performance of the original Hartley image rejection receiver. In this simulation, the number of stages (N) was also set to 2. The input “desired signal to image signal power ratio” α_{in} was set to 0 dB and the phase mismatch was set to 1° . From this figure, we again observe that the IRR performance of our receiver is much better than the original Hartley image rejection receiver, and it becomes better as the bit resolution increases. The IRR performance of the original Hartley image rejection receiver decays rapidly as the gain mismatch increases. However, the IRR performance of our receiver degrades slowly as the gain mismatch initially increases.

To investigate the effect of the input “desired signal to image signal power ratio” on the IRR performance, we simulated the simplified implementation method at different α_{in} values when the number of stages was set to 2. Fig. 11 shows the simulated

IRR performance versus α_{in} values. The gain mismatch was set to 1 dB and the phase mismatch was set to 1° . From the figure, we observe that the IRR performance improves as the bit resolution increases. In addition, the IRR performance improves as α_{in} decreases and remains at a constant value when α_{in} is below about -30 dB.

From the above simulation results, we found that the IRR performance of the hybrid image rejection receiver is limited by the quantization effect. Therefore, a higher resolution A/D is needed to achieve better IRR performance. For example, if we want to achieve a 50 dB of IRR, we need to use an A/D converter with 12 bits resolution in the hybrid receiver system.

Although the IRR performance is limited by the quantization effect, it is quite insensitive to phase mismatch in the hybrid receiver system. We can achieve good IRR performance even though the phase matching is relatively poor. On the other hand, gain mismatch affects the IRR performance more but it can be corrected also more easily. Therefore, the matching requirements for the analog devices in the hybrid image rejection receiver can be greatly relaxed.

V. CONCLUSION

The mismatching effect in the analog devices is the main problem of a Hartley image rejection receiver. In this paper, we presented a hybrid image rejection receiver architecture. This architecture utilizes both analog and digital signal processing techniques to compensate for the mismatching effect and suppress the image signal. This method is shown to be able to effectively enhance the image rejection ratio (IRR) performance.

We also proposed a simplified implementation method for the hybrid image rejection receiver to reduce its computation requirements. The performance of the simplified implementation method was simulated to include the quantization effect. Our simulation results demonstrated that the IRR performance of the hybrid image rejection receiver is much better than the original Hartley image rejection receiver and is insensitive to the phase mismatch. This architecture not only greatly relaxes the matching requirements for the analog devices but also provides a feasible solution for an IC implementation.

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