Journal of The Electrochemical Society, **148** (6) F127-F132 (2001)
0013-4651/2001/148(6)/F127/6/$7.00 © The Electrochemical Society, Inc.

Physical and Electrical Characteristics of Methylsilane- and Trimethylsilane-Doped Low Dielectric Constant Chemical Vapor Deposited Oxides

Zhen-Cheng Wu,[a,z] Zhi-Wen Shiung,[a] Chiu-Chih Chiang,[a] Wei-Hao Wu,[a] Mao-Chieh Chen,[a,*] Shwang-Ming Jeng,[b] Weng Chang,[b] Pei-Fen Chou,[b] Syun-Ming Jang,[b] Chen-Hua Yu,[b] and Mong-Song Liang[b]

[a]*Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan*
[b]*Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan*

This work investigates the physical and electrical properties of two species of inorganic C-doped low dielectric constant (low-*k*) chemical vapor deposited (CVD) organosilicate glasses (OSGs, α-SiCO:H). They are both deposited by plasma-enhanced CVD (PECVD) processes using methylsilane [$(CH_3)SiH_3$, 1 MS]- and trimethylsilane [$(CH_3)_3SiH$, 3 MS]-based gases as the reagents, and are designated as OSG1 and OSG2, respectively. Experimental results indicate that the thermal stability temperature of OSG1 is 500°C, while that of OSG2 is 600°C, based on the results of thermal annealing for 30 min in an N_2 ambient. The deterioration of the low-*k* property in OSG1 is predominately due to the thermal decomposition at temperatures above 500°C of methyl ($-CH_3$) groups, which are introduced to lower the density and polarizability of OSGs. For the Cu-gated oxide-sandwiched low-*k* dielectric metal-insulator-semiconductor (MIS) capacitors, Cu permeation was observed in both OSG1 and OSG2 after the MIS capacitors were bias-temperature stressed at 150°C with an effective applied field of 0.8 MV/cm. Moreover, Cu appeared to drift more readily in OSG1 than in OSG2, presumably because OSG1 has a more porous and less cross-linked structure than OSG2. The Cu penetration can be mitigated by a thin nitride dielectric barrier.
© 2001 The Electrochemical Society. [DOI: 10.1149/1.1369373] All rights reserved.

Manuscript submitted August 7, 2000; revised manuscript received January 3, 2001.

As the feature dimension of the device in integrated circuits (ICs) scales down below 0.18 μm, on-chip interconnects become a dominant factor in determining the overall IC chip performance, packing density, reliability, and manufacturing cost of deep submicrometer ultralarge-scale integrated (ULSI) circuits. With Cu successfully integrated with SiO_2 using dual damascene processes in advanced sub-0.25 μm circuits for improved interconnect conductivity and reliability, the process integration of Cu with low dielectric constant (low-*k*) dielectrics has also received extensive attention.[1] Realizing the robust combination of Cu and low-*k* dielectrics in the prevalent Cu dual damascene architecture will entail the further performance improvement in driving speed, crosstalk interference, and dynamic power dissipation by the reduction in the interconnect parasitic capacitance (intra/interlevel capacitive load).[2] Currently, low-*k* dielectrics are being extensively studied and developed on both organic (carbon-based) and inorganic (SiO_2-based) materials using both spin-on (SO) and chemical vapor deposition (CVD) techniques.[2-11] Low-*k* films deposited by CVD are lately attracting immense attention for possible back-end-of-line (BEOL) applications because CVD techniques provide several crucial advantages, such as superior gap-filling capability and extremely uniform coating of large areas, which is necessary to future 300 mm wafers.[12] Furthermore, the CVD method is a dry process and generally needs fewer processing steps and lower processing costs than the spin-on method.[3,5,12] These characteristics make the CVD process easier for equipment manufacturers to integrate with other key processes, which may become a necessity for the final production yield consideration.

Among various low-*k* CVD films, SiO_2-based dielectrics have attracted enormous interest because of their physical rigidity, mechanical strength, and process extendibility, which together minimize integration risks and costs. Previous work has shown the benefits of incorporating fluorinated silicate glass (FSG, $k = 3.5\text{-}3.7$) into BEOL applications, as opposed to using the conventional undoped silicate glass (USG, $k = 3.9\text{-}4.1$).[10,13,14] Nevertheless, accommodating dielectrics with even lower *k* values is inevitable as Cu interconnects are further scaled down to the 0.15/0.13 μm node. C-doped low-*k* CVD organosilicate glasses (OSGs) become feasible candidates because of their lower *k* values (<3.0) than that of FSG. In this work, we investigate the thermal stability and electrical reliability issues of two species of newly developed OSGs, methylsilane- and trimethylsilane-doped oxides, with regard to integration with Cu metallization.

Experimental

Electrical measurements were made on Cu- and TaN-gated oxide-sandwiched low-*k* dielectric metal-insulator-semiconductor (MIS) capacitors. Figure 1 schematically illustrates the cross section of the Cu- and TaN-gated capacitors. The TaN-gated capacitors are used as control samples since TaN neither mixes with the silicon oxide layer nor oxidizes under the thermal conditions used in this study.[15] Samples were prepared by first growing a 18 nm thick thermal oxide on p-type (100)Si wafers at 1000°C in a dry oxygen atmosphere. This oxide layer is required to form a stable dielectric-to-substrate interface for well-behaved capacitance-voltage (C-V) characteristics. Two species of low-*k* dielectric inorganic CVD organosilicate glasses (OSGs, α-SiCO:H) were investigated; they are referred to hereinafter as OSG1 ($k = 2.9\text{-}3.0$) and OSG2 ($k = 2.5\text{-}2.7$), both of which were deposited over the thermal oxide to a thickness of 500 nm by plasma-enhanced CVD (PECVD) processes in a parallel plate reactor operating at 13.56 MHz. The discharge was struck between two 26.3 cm diam electrodes spaced 300 mil apart. The OSG1 films were deposited using the gas mixture of methylsilane [$(CH_3)SiH_3$] and nitrous oxide (N_2O) as the reactive gases with the following conditions: substrate temperature, 17°C; total gas pressure, 1-10 Torr; rf power, 50-100 W; and $(CH_3)SiH_3/N_2O$ flow ratio of 2/5. The OSG2 films were grown utilizing the gas mixture of trimethylsilane [$(CH_3)_3SiH$] and oxygen (O_2) as the reagents with the following conditions: substrate temperature, 350°C; total gas pressure, 1-10 Torr; rf power, 400-600 W; and $(CH_3)_3SiH/O_2$ flow ratio of 1/6. A 50 nm thick PECVD USG (undoped silicate glass, $k = 4.2$) was then deposited on the low-*k* CVD dielectrics. The USG films were deposited in a parallel plate reactor operating at 13.56 MHz at the following conditions: substrate temperature, 400°C; total gas pressure, 1-5 Torr; rf power, 1000-1500 W; and $SiH_4/N_2/N_2O$ flow ratio of 3/16/95. This oxide cap may be required to act as a chemical mechanical polishing (CMP) hard mask in the Cu damascene architecture and a barrier to

* Electrochemical Society Active Member.
z E-mail:u8511503@cc.nctu.edu.tw

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

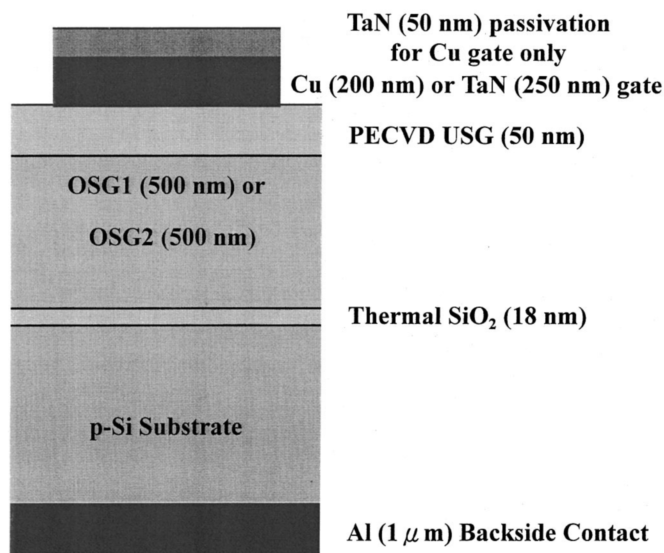

Figure 1. Schematic cross section of Cu- and TaN-gated oxide-sandwiched OSG1 and OSG2 MIS capacitors studied in this work.

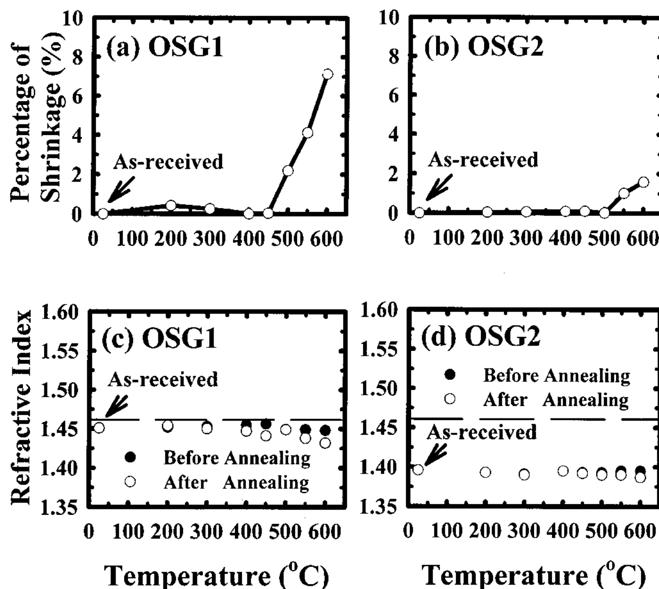

Figure 2. Temperature dependence of (a) and (b) percentage shrinkage of film thickness and (c) and (d) refractive index for OSG1 and OSG2 films.

minimize the absorption of moisture in the low-*k* films. Another split of samples with a 75 nm thick PECVD nitride (SiN, $k = 7\text{-}9$) barrier replacing this oxide cap layer were also prepared to examine the SiN barrier effectiveness against Cu penetration. The SiN barrier was deposited in a parallel plate reactor operating at 13.56 MHz at the following conditions: substrate temperature, 400°C; total gas pressure, 1-5 Torr; rf power, 400-600 W; and SiH_4/NH_3 flow ratio of 1/8. The samples underwent a degas bake at 400°C for 30 min in an N_2 ambient to remove absorbed moisture in the dielectric stack prior to the metal electrode deposition. A Cu film of 200 nm thickness was then sputter deposited using a dc magnetron sputtering system with a base pressure of $1\text{-}2 \times 10^{-6}$ Torr and no intentional substrate heating. The Cu surface was further covered with a 50 nm thick TaN overlayer, which was reactively sputtered in the same sputtering system without breaking the vacuum, using a Ta target in a gas mixture of Ar and N_2 with Ar/N_2 flow rates of 24/6 sccm. The TaN overlayer prevents oxidation of the Cu layer in the subsequent high-temperature process. For the TaN-gated control samples, a 250 nm thick TaN layer was reactively sputter deposited directly on the oxide (USG) cap layer. A lift-off process, instead of a chemical wet etching of the vulnerable low-*k* dielectric stack, was used to define gate electrodes in a circular area of 0.8 mm diam. A 1 μm thick Al layer was thermally evaporated on the back side of the Si substrates for all samples to achieve a better contact for electrical measurements.

The completed Cu- and TaN-gated MIS capacitors were thermally annealed at 400°C for 1 h in an N_2 ambient. This annealing step eliminates the plasma damage during gate electrode sputtering, and provides the driving force for Cu permeation. The MIS capacitors were then bias-temperature stressed (BTS) at 150°C with an effective applied field of 0.8 MV/cm for 30 min, which is long enough for the mobile charges to drift across the stacked insulator layer. The bias during BTS was provided by an HP 4145B semiconductor parameter analyzer, and the room temperature C-V characteristic was measured by a Keithley package 82 system. Notably, the MIS capacitors were first baked at 200°C on the thermal chuck for 1 h in the N_2 ambient to dehydrate the CVD dielectric stack prior to any BTS and/or electrical measurement and that all BTS measurements were performed with a continuous N_2 purge to avoid the uptake of moisture in the CVD dielectric films throughout testing. High frequency C-V characteristics of the MIS capacitors, sweeping from inversion to accumulation, were measured at a frequency of 1 MHz.

Several techniques were utilized for intrinsic physical property measurements. Blanket samples of (OSG1, OSG2)/thermal oxide/Si structures were prepared following the same processing sequence with the MIS capacitors used for electrical measurements except that both the upper USG cap layer and metal electrodes were omitted. Notably, the samples were first thermally annealed at 400°C for 30 min in an N_2 ambient to remove absorbed moisture in the CVD dielectric films prior to any physical analysis. The *k* value of the films was evaluated from the maximum capacitance values obtained from the high frequency C-V characteristics measured at 1 MHz on the Al-gated MIS capacitors; the area correction of the Al gate electrodes was made by optical microscopy (OM). Both the film thickness and the refractive index of the CVD dielectric layers were measured using a well-calibrated N&K analyzer at 6328 Å wavelength. Fourier transform infrared spectroscopy (FTIR) and thermal desorption mass spectroscopy (TDS) were used to characterize the chemical bonding evolution and outgassing behavior of the low-*k* dielectrics during the thermal annealing process. Rutherford backscattering spectrometry (RBS) was used to determine the atomic compositions of the OSG α-SiCO:H films. Secondary ion mass spectroscopy (SIMS) was employed to probe the possible presence of Cu in the dielectric stacks of the MIS capacitors.

Results and Discussion

Physical properties and thermal stability of OSG1 and OSG2 dielectric films.—Figure 2 shows the thickness shrinkage and refractive index for OSG1 and OSG2 thermally annealed at various temperatures. Evidently, the film thickness for OSG1 shrank (>2%) upon annealing at temperatures above 500°C, and the refractive index also exhibited a decreasing tendency, implying changes in film composition and bonding structure in OSG1, while similar changes to a minor extent were also observed for OSG2 at temperatures above 600°C. The reference value of 1.46 for the refractive index of the thermal oxides is indicated by a dashed line. Refractive indexes below 1.46 were proposed herein to indicate porous or less dense materials like OSGs.[16] In fact, these low density OSG films contain atomic scale nanoporosity or microvoid, which is closely related to the incorporation of CH_3 moieties into the films from organosilicon gas, $(CH_3)_xSiH_{4-x}$.[17-20] Figure 3 presents the FTIR spectra for OSG1 and OSG2 thermally annealed at various temperatures. Two remarkable features exist in the evolution of the absorption peaks. First, the Si-OH peak at about 3700 cm^{-1} did not appear in the

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

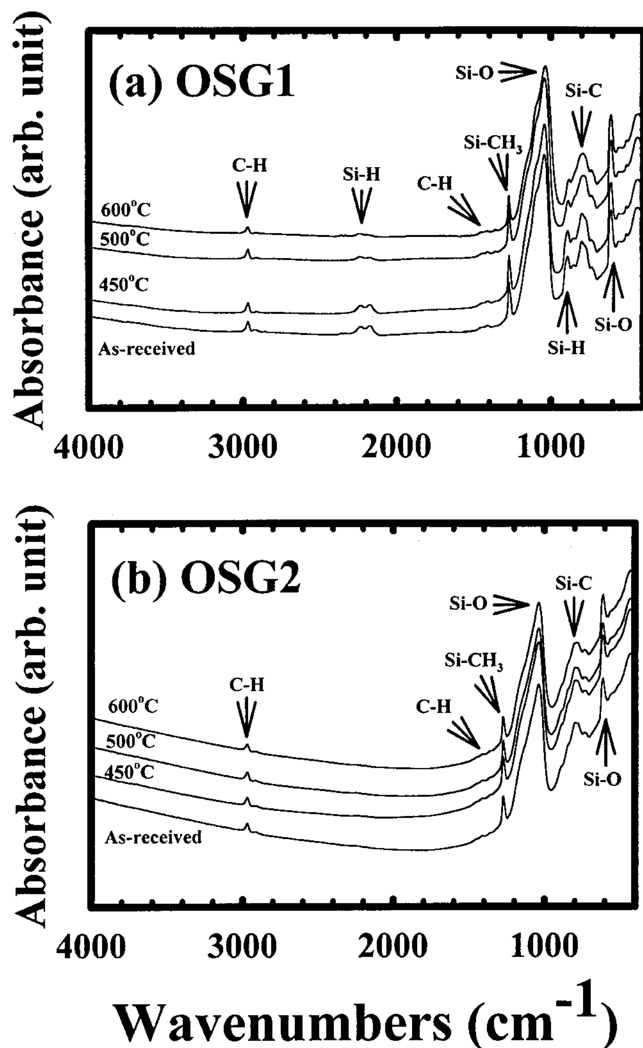

Figure 3. FTIR absorption spectra of (a) OSG1 and (b) OSG2 films annealed at various temperatures for 30 min in an N_2 ambient.

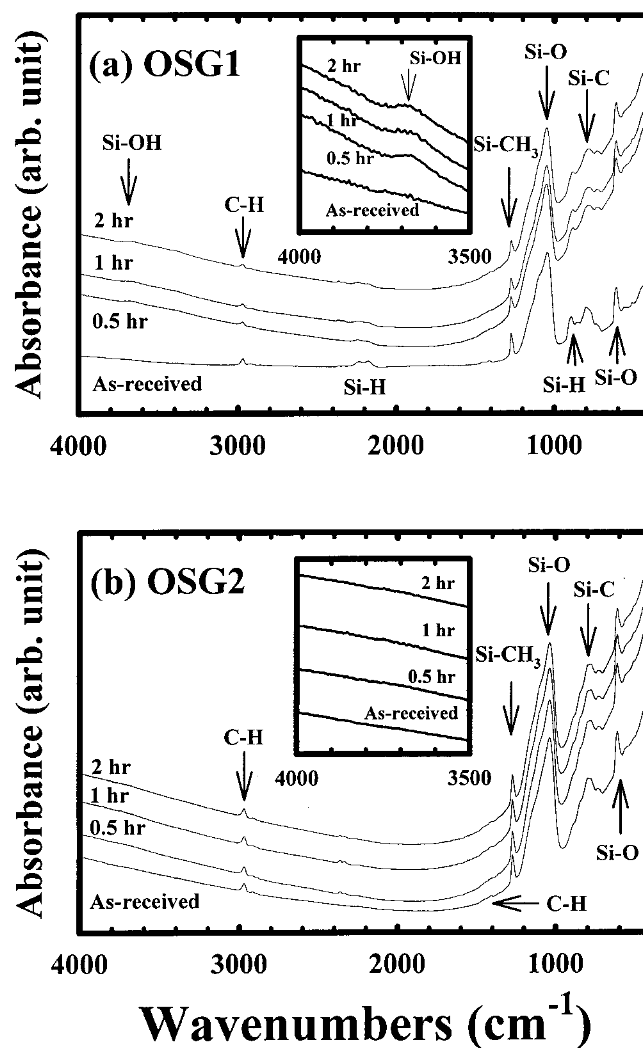

Figure 4. FTIR absorption spectra of (a) OSG1 and (b) OSG2 films immersed in boiling water for various periods of time. The inset shows a part of the enlarged spectra.

FTIR spectra for either OSG1 or OSG2, indicating that the low-*k* CVD OSG dielectrics used herein were not susceptible to moisture uptake in the normal ambient. However, immersing the OSG1 film in boiling water for 30 min caused the Si-OH peak to appear in the FTIR spectra, whereas it remained stable for the OSG2 film even after immersion in boiling water for 2 h, as shown in Fig. 4. Despite the presumption that incorporating CH_3 groups into the Si-O network could cause OSGs to become hydrophobic, moisture uptake in OSG1 by immersing in boiling water may be associated with its porous structure.[2-4,7,21] Since moisture uptake in the porous film should be easier because of the film's effective larger surface area, OSG1 is presumed to be more porous than OSG2.[22,23] Such a susceptibility to moisture may adversely affect the electrical reliability of OSG1 with respect to integration with Cu metallization. Second, both OSG1 and OSG2 are hybrid materials whose infrared spectra consist of both organic and inorganic absorption peaks. The organic Si-CH_3 bonds reduce the density and polarizability of OSG films due to the steric hindrance of CH_3 groups, while the inorganic Si-O bonds constitute the main OSG network. The Si-O stretch peak at 1042 cm^{-1} in OSG1 contains a shoulder at higher wavenumbers, indicating that the open chain and caged Si-O structural configuration coexist in this bond, whereas such a Si-O shoulder is unclear in OSG2. This major distinction of the Si-O bonding configuration implies different chemical bonding schemes between OSG1 and OSG2. Figure 5 shows the peak height ratio of Si-CH_3 (1273 cm^{-1}) to Si-O (1042 cm^{-1}) in the OSG films. The peak height ratio in OSG1 remained constant at temperatures of up to 500°C, but dropped sharply at a temperature of 600°C (Fig. 5a), while the ratio in OSG2 remained unchanged all the way to temperatures of up to 600°C (Fig. 5b). Thus, degradation of the low-*k* property of OSG1, most importantly the *k* value, can be expected at temperatures above 500°C. Figure 6 shows the dielectric constants of OSG1 and OSG2 thermally annealed at various temperatures, with the data of USG included for comparison. The smaller *k* value of OSG2 than that of OSG1 represents a less polarizable bonding geometry in OSG2, despite the similar atomic ratio of C to Si (0.75-0.82), as determined by RBS, in both as-received OSG films studied herein. Moreover, as expected, the dielectric constant for OSG1 increased dramatically when temperatures exceeded 500°C. Conceivably, the *k* value in OSG1 deteriorated predominately because of the partial removal of the CH_3 groups, making the film prone to moisture uptake, and to appearing hydrophilic at localized areas on its surface. This result is further confirmed from the measured TDS spectra (not shown), wherein the desorption of CH_3 increased markedly at temperatures above 500°C. In summary, the thermal stability of OSG1 was found to be 500°C, while that of OSG2 was 600°C, both higher than that of organic PAE-2 with aromatic structures.[24]

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

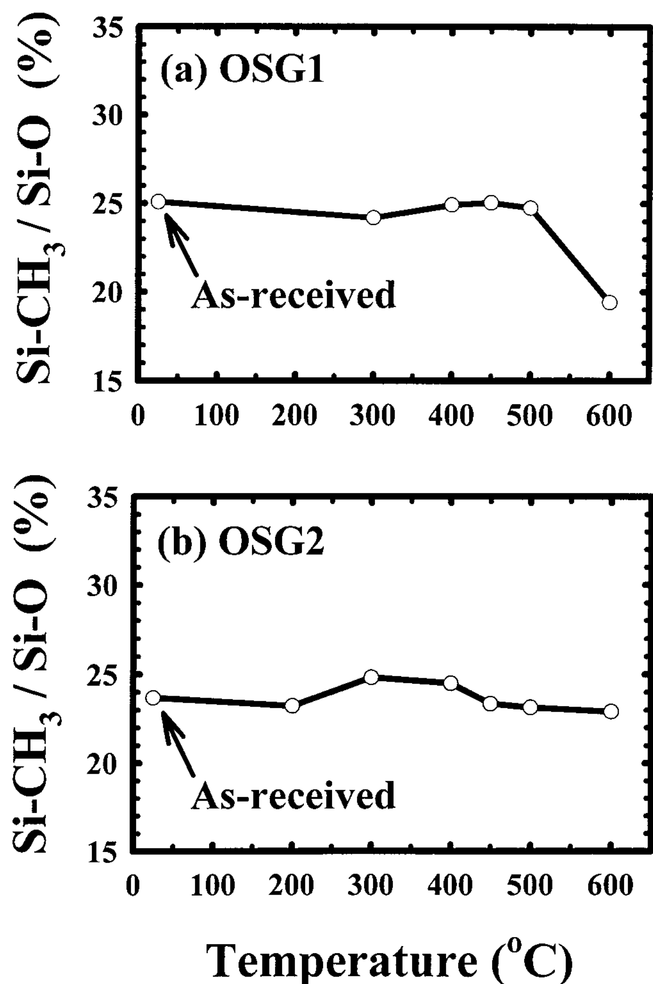

Figure 5. Temperature dependence of peak height ratios of Si-CH_3/Si-O for (a) OSG1 and (b) OSG2 films, as determined from FTIR spectra.

Electrical characteristics of oxide-sandwiched OSG1 and OSG2 capacitors.—Figure 7 shows C-V curves of the Cu- as well as TaN-gated oxide-sandwiched OSG1 and OSG2 MIS capacitors before and after BTS at 150°C. The BTS was first applied with a positive bias (on the gate electrode) corresponding to an effective field of 0.8 MV/cm for 30 min, and followed by application with a negative bias under the same conditions. For both of the OSG1 and OSG2 capacitors, the negative flatband voltage shift (ΔV_{FB}) of the Cu-gated capacitor resulting from the positive BTS was clearly larger than that of the TaN-gated capacitor, implying the presence of positively charged mobile Cu ions in both Cu-gated OSG1 and OSG2 films. Moreover, Cu ions obviously drift more readily in OSG1 than in OSG2. Such a fast permeation of Cu in OSG1 is presumably due to the more porous structure of OSG1, which contains high density nanometer-sized pores with radii of about 4-12 Å and total volume fraction of about 36%. These nanopores act as fast diffusion short-cuts via which Cu can drift rapidly in porous OSG1. Meanwhile, CVD dielectrics deposited at higher temperatures like OSG2 generally possess a more cross-linked bonding structure that the Cu drift in OSG2 may be prohibited owing to the miniature free volume in the OSG2's Si-O network.[25-28] Moreover, it was also reported that water vapor in the ambient greatly compounded the permeation of Cu in the oxide network, either by causing deep level electron traps,[28,29] or by hydration energy. As a result, even with continuous N_2 purging during BTS measurements, Cu drift in OSG1 may also be enhanced by the uptake of a trace of H_2O, due to the susceptibility to moisture that differentiates OSG1 from OSG2. The smaller

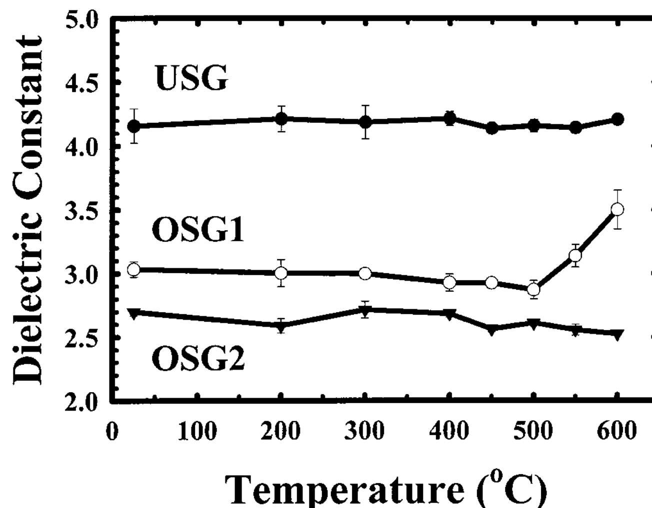

Figure 6. Dielectric constant *vs.* annealing temperature for USG, OSG1, and OSG2 films.

negative ΔV_{FB} associated with the TaN-gated OSG1 capacitor compared with the Cu-gated counterpart resulted from the contaminated ionic charges, such as the alkali or hydrogen-related impurity in the upper USG cap layer.[30] This relationship can be verified by the fact that replacing the USG cap layer with a SiN cap layer resulted in negligible ΔV_{FB}. These contaminated ionic charges may also exist in the USG cap layer of the OSG2 capacitor, but probably due to the sturdy cross-linked structure of OSG2, these ionic charges are not able to drift in OSG2 as easily as they did in OSG1. Meanwhile, the large positive ΔV_{FB} and marked distortion in C-V resulting from the negative BTS on the Cu-gated and TaN-gated OSG1 capacitors may be associated with natural dielectric degradation, and is not related to Cu ion drift. These OSG1 capacitors were seriously damaged

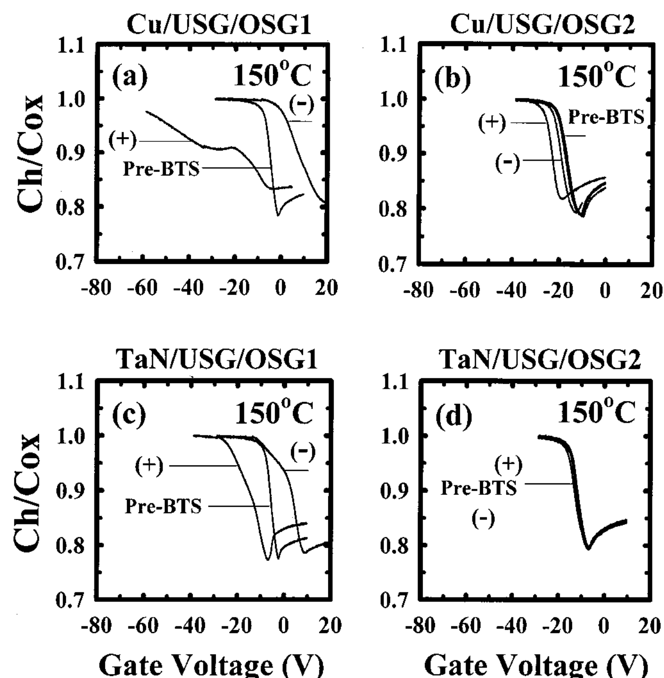

Figure 7. C-V characteristics of Cu- and TaN-gated oxide-sandwiched OSG1 and OSG2 MIS capacitors before and after BTS at 150°C with an effective applied field of 0.8 MV/cm for 30 min. The positive (+) bias was applied first, followed by the negative (−) bias at the same conditions.

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

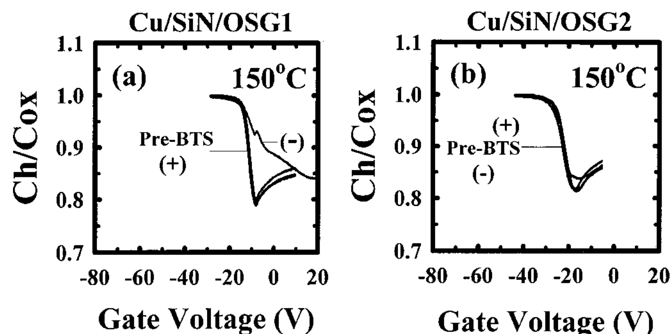

Figure 8. C-V characteristics of Cu-gated and SiN-capped (a) OSG1 and (b) OSG2 MIS capacitors before and after BTS. The conditions of BTS are the same as those of Fig. 7.

because a succeeding positive BTS induced many positive bulk charges and interface states. Such a dielectric degradation of OSG1 is presumably related to its intrinsic porous film structure that the OSG1 film is not able to withstand the stress field applied herein. Figures 8 and 9 show, respectively, the C-V curves and SIMS depth profiles of the BTS stressed Cu-gated OSG1 and OSG2 capacitors with a 75 nm thick SiN cap layer sandwiched between the OSG dielectrics and the Cu electrodes. The SIMS depth profiles of the Cu-gated USG capped OSG1 and OSG2 capacitors after the positive BTS are also included for comparison. The SiN cap layer achieves significant improvements in the OSG1 and OSG2 films, both in the absence of negative ΔV_{FB} with regard to the positive BTS, and in the absence of Cu penetration. Moreover, based on the results of SIMS depth profiles, the permeation of Cu appeared to be more severe in OSG1 than in OSG2. This finding was in complete accord with the results of electrical measurements that the negative ΔV_{FB} resulting from the positive BTS on the Cu-gated OSG2 capacitors was much smaller than that on the Cu-gated OSG1 capacitors. Thus, it was concluded, from all the above observations, that the large negative ΔV_{FB} in the Cu-gated oxide-sandwiched OSG1 and OSG2 MIS capacitors was caused by the presence of Cu ions after the positive BTS, and the 75 nm thick SiN cap layer acted as an effective dielectric barrier against Cu permeation.

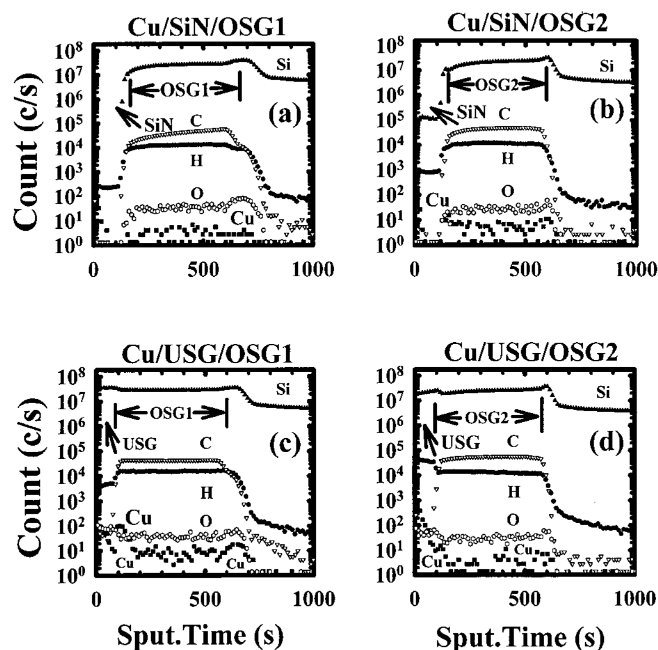

Figure 9. SIMS depth profiles of Cu-gated (a) SiN-capped OSG1, (b) SiN-capped OSG2, (c) USG-capped OSG1, and (d) USG-capped OSG2 MIS capacitors after a positive BTS at 150°C with an effective applied field of 0.8 MV/cm for 30 min. The Cu gate was removed prior to the SIMS measurements.

Conclusion

Two species of inorganic low-*k* C-doped CVD organosilicate glasses (OSGs, α-SiCO:H) were assessed for their structural stability under various thermal annealing conditions and electrical reliability with regard to integration with Cu metallization. The thermal stability temperature of 1 MS-doped oxides (OSG1) was found to be 500°C, while that of 3 MS-doped oxides (OSG2) was 600°C. Although Cu permeation was observed in both OSG dielectrics, Cu appeared to drift more readily in OSG1 than in OSG2. The distinct difference between the observed Cu drift behavior in OSG1 and OSG2 was presumably due to the more porous and less cross-linked structure of OSG1. Moreover, the nitride layer (75 nm) was verified to be an effective dielectric barrier against Cu penetration.

Acknowledgments

The authors thank Dr. Ming-Shih Tsai of NDL and Dr. Bing-Yue Tsui of NCTU for their valuable discussion and suggestions, and Chih-Jian Chen, Tien-I Bao, and Ai-Juan Chen of TSMC for their technical assistance.

National Chiao-Tung University assisted in meeting the publication costs of this article.

References

1. D. Edelstein, J. Heidenreich, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, P. Roper, T. McDevitt, W. Motsiff, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, R. Schulz, L. Su, S. Luce, and J. Slattery, in *Proceeding of 1997 IEEE IEDM*, p. 773, IEEE (1997).
2. L. Peters, *Semicond. Int.,* **1998**, 64 (Sept).
3. L. Peters, *Semicond. Int.,* **2000**, 52 (Jan).
4. L. Peters, *Semicond. Int.,* **1999**, 56 (Nov).
5. J. Baliga, *Semicond. Int.,* **1998**, 139 (June).
6. M. Matsuura, Y. Hayashide, H. Kotani, T. Nishimura, H. Iuchi, C. D. Dobson, A. Kiermasz, K. Beekmann, and R. Wilby, in *Proceedings of 1994 IEEE IEDM*, p. 117, IEEE (1994).
7. M. Matsuura, I. Tottori, K. Goto, K. Maekawa, Y. Mashiko, and M. Hirayama, in *Proceedings of 1997 IEEE IEDM*, p. 785, IEEE (1997).
8. A. R. K. Ralston, J. F. Gaynor, A. Singh, L. V. Le, R. H. Havemann, M. A. Plano, T. J. Cleary, J. C. Wing, and J. Kelly, in *Proceedings of 1997 IEEE VlSI Symposium*, p. 81, IEEE (1997).
9. M. Moussavi, G. Passemard, J. C. Maisonobe, and P. Turek, in *Proceedings of 1999 IEEE IITC Symposium*, p. 50, (1999).
10. W. Chang, S. M. Jang, C. H. Yu, S. C. Sun, and M. S. Liang, in *Proceedings of 1999 IEEE IITC Symposium*, p. 131, IEEE (1999).
11. M. Naik, S. Parikh, P. Li, J. Educato, D. Cheung, I. Hashim, P. Hey, S. Jenq, T. Pan, F. Redeker, V. Rana, B. Tang, and D. Yost, in *Proceedings of 1999 IEEE IITC Symposium*, p. 181, IEEE (1999).
12. T. M. Lu and J. A. Moore, *MRS Bull.,* **1997**, 28 (Oct).
13. J. Ida, M. Yoshimaru, T. Usami, A. Ohtomo, K. Shimokawa, A. Kita, and M. Ino, in *Proceedings of 1994 IEEE VLSI Symposium*, p. 59, IEEE (1994).
14. T. Fukuda, T. Hosokawa, Y. Nakamura, K. Katoh, and N. Kobayashi, in *Proceedings of 1996 IEEE VLSI Symposium*, p. 114, IEEE (1996).
15. J. C. Chuang and M. C. Chen, *J. Electrochem. Soc.,* **145**, 4029 (1998).
16. C. Falcony, J. C. Alonso, A. Ortiz, M. Garcia, E. P. Zironi, and J. Rickards, *J. Vac. Sci. Technol. A,* **11**, 2945 (1993).
17. R. P. Mandal, D. Cheung, W. F. Yau, B. Cohen, S. Rengarajan, and E. Chou, in *Proceedings of 1999 IEEE/SEMI Advanced Semiconductor Manufacturing Conference*, p. 299, IEEE (1999).
18. R. P. Mandal, V. Rana, M. Naik, D. Yost, D. Cheung, and W. F. Yau, in *Proceedings of 1999 VMIC*, p. 585 (1999).
19. A. Grill and V. Patel, *J. Appl. Phys.,* **85**, 3314 (1999).
20. B. K. Hwang, M. J. Loboda, G. A. Cerny, R. F. Schneider, J. A. Seifferly, and T. Washer, in *Proceedings of 2000 IEEE IITC*, p. 52, IEEE (2000).
21. A. Nara and H. Itoh, *Jpn. J. Appl. Phys.,* **36**, 1477 (1997).
22. A. Jain, S. Rogojevic, S. V. Nitta, V. Pisupatti, W. N. Gill, P. C. Wayner Jr., and J. L. Plawsky, *Mater. Res. Soc. Symp. Proc.,* **565**, 29 (1999).
23. N. Lifshitz and G. Smolinsky, *J. Electrochem. Soc.,* **136**, 2335 (1989).
24. Z. C. Wu, C. C. Wang, R. G. Wu, Y. L. Liu, P. S. Chen, Z. M. Zhu, M. C. Chen, J. F. Chen, C. I. Chang, and L. J. Chen, *J. Electrochem. Soc.,* **146**, 4290 (1999).
25. A. L. S. Loke, J. T. Wetzel, P. H. Townsend, T. Tanabe, R. N. Vrtis, M. P. Zussman, D. Kumar, C. Ryu, and S. S. Wong, *IEEE Trans. Electron Devices,* **ED-46**, 2178 (1999).
26. Y. Uchida, K. Taguchi, T. Nagai, and M. Matsumura, in *Proceedings of 1998 DUMIC*, p. 46 (1998).

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

27. A. Grill, L. Perraud, V. Patel, C. Jahnes, and S. Cohen, *Mater. Res. Soc. Symp. Proc.,* **565**, 107 (1999).
28. J. D. Mcbrayer, R. M. Swanson, and T. W. Sigmon, *J. Electrochem. Soc.,* **133**, 1242 (1986).
29. Y. S. Diamand, A. Dedhia, D. Hoffstetter, and W. G. Oldham, *J. Electrochem. Soc.,* **140**, 2427 (1993).
30. A. L. S. Loke, C. Ryu, C. P. Yue, J. S. H. Cho, and S. S. Wong, *IEEE Electron Device Lett.,* **EDL-17**, 549 (1996).

Downloaded on 2014-04-27 to IP 140.113.38.11 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).