



## Interface traps and random dopants induced characteristic fluctuations in emerging MOSFETs

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### ARTICLE INFO

#### Article history:

Received 24 February 2011

Received in revised form 20 March 2011

Accepted 23 March 2011

Available online 30 March 2011

#### Keywords:

High- $\kappa$ /metal gate

Interface trap

Random dopant

Threshold voltage fluctuation

Interface trap fluctuation

Random dopant fluctuation

Combination of interface trap and random dopant fluctuations

### ABSTRACT

In this work, we study the effect of interface traps (ITs) and random dopants (RDs) on characteristics of 16-nm MOSFETs. Totally random generated devices with 2D ITs between the interface of silicon and HfO<sub>2</sub> film as well as 3D RDs inside the silicon channel are simulated. Fluctuations of threshold voltage and on/off state current for devices with different EOT of insulator film are analyzed and discussed. The results of this study indicate ITs and RDs statistically correlate to each other and RDs govern device variability, compared with the influence of ITs. Notably, the position of ITs and RDs induces rather different fluctuation in spite of the same number of ITs and RDs are investigated.

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## 1. Introduction

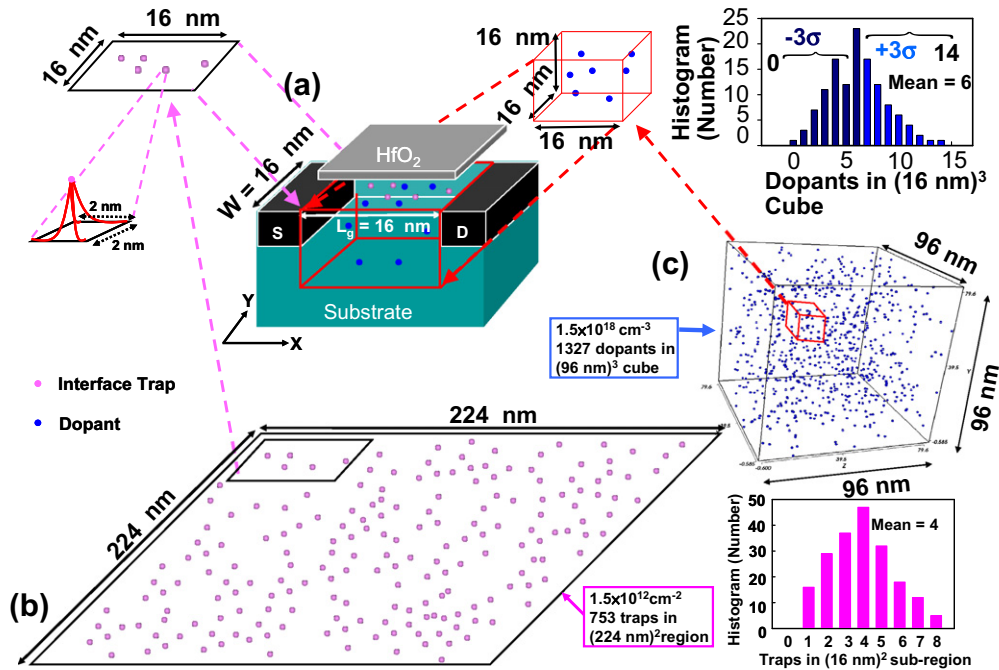
Characteristic variability of nano-CMOS devices increases as device dimension reduces [1–5], for example, the RD-induced threshold voltage fluctuation ( $\sigma V_{th}$ ) up to 40 mV for 20-nm planar CMOS has been experimentally quantified [3]. RD fluctuation (RDF) has been recognized as one of the major limitations in device scaling; recently, high- $\kappa$ /metal gate (HKMG) plays a key technology to reduced intrinsic parameter fluctuation, and leakage current for sub-45-nm generations [3,4]. However, the generation of ITs on the interface of silicon and high- $\kappa$  introduces a new source of fluctuation for the degradation of device characteristics [6–10]. In this work, we intensively study the distributions of ITs and RDs induced characteristic fluctuation of 16-nm MOSFETs using an experimentally calibrated 3D device simulation. 2D ITs on the interface of silicon and HfO<sub>2</sub> film and 3D RDs inside the silicon channel are simultaneously considered in the 3D device simulation [3,4]. Physical findings on  $\sigma V_{th}$  and variability of  $I_{on}/I_{off}$  versus the number and position of ITs and/or RDs are discussed.

## 2. Simulation methodology

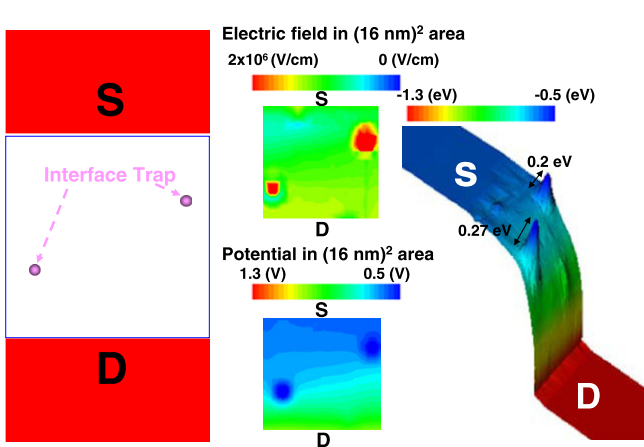
The validated performance of studied HKMG device, according to ITRS roadmap for low operating power, is experimentally quantified in our recent study [3]. Note that the threshold voltage of 16-nm N-MOSFET is equal to 250 mV. The devices we examined are the 16-nm planar MOSFETs (width: 16 nm) with amorphous-based TiN/HfO<sub>2</sub> gate stacks; an EOT of 0.8 and 1.2 nm are shown in Fig. 1(a). For the simulation of IT fluctuation (ITF), we first generate 753 acceptor-like traps in a large plane in Fig. 1(b), where the trap's concentration in the large plane is around  $1.5 \times 10^{12} \text{ cm}^{-2}$  based upon experimental characterization, and the total number of generated traps mainly follows the Poisson distribution. Then, the statistically generated large plane is partitioned into many sub-planes, where the number of traps in the sub-planes may vary from one to eight and the average is four. The energy of each trap on each sub-plane is assigned according to the distribution of trap density [6–9]. We explore the density of ITs varying from  $5 \times 10^{11}$  to  $5 \times 10^{12} \text{ cm}^{-2}$ . We repeat this process until all sub-regions are assigned. RDs' number and position in the channel region are statistically generated discrete dopants, as shown in Fig. 1(c), which are also incorporated into the 3D device simulation and performed on our parallel computing system. The detail of RDF simulation technique was reported in our previous works [3,4]. Therefore, about 200 samples are generated for the 3D device

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**Fig. 1.** (a) The source of randomness (pink dots are interface traps and blue dots are discrete dopants) and simulation settings for fluctuations of random ITs and RDs. (b) We first generate 753 acceptor-like traps in a large plane, where the trap's concentration in the plane is around  $1.5 \times 10^{12} \text{ cm}^{-2}$  and the total number of generated traps follow the Poisson distribution. The energy of each trap on the plane is assigned according to distribution of trap's density. Then the entire plane is partitioned into sub-planes (size:  $16 \text{ nm} \times 16 \text{ nm}$ ), where the number of traps in all sub-planes may vary from one to eight and the average number is four. (c) Discrete dopants randomly distributed in  $(96 \text{ nm})^3$  cube with the average concentration of  $1.5 \times 10^{18} \text{ cm}^{-3}$ . There will be 1327 dopants within the cube and dopants vary from 0 to 14 (the average number is six) for all 216 sub-cubes. The size of each sub-cube is  $(16 \text{ nm})^3$ . The total sub-cubes and sub-planes are then mapped into device's 3D channel and 2D surface for RDs and ITs' position/number-sensitive simulation (b). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

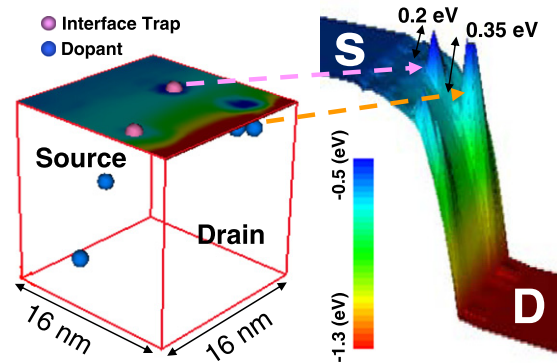


**Fig. 2.** The on-state ( $V_G = V_D = 0.8 \text{ V}$ ) electric field and potential distribution of the channel surface extracted from one of simulated 16-nm transistors, where  $EOT = 0.8 \text{ nm}$ . The device fluctuated by two random ITs at Si/HfO<sub>2</sub> oxide interface. The traps between the interface of Si and high- $\kappa$  oxide irregularly twist the local electric field and the potential, where the barrier is affected by ITF clearly.

simulation to estimate the ITs and RDs induced characteristic fluctuation in MOSFETs.

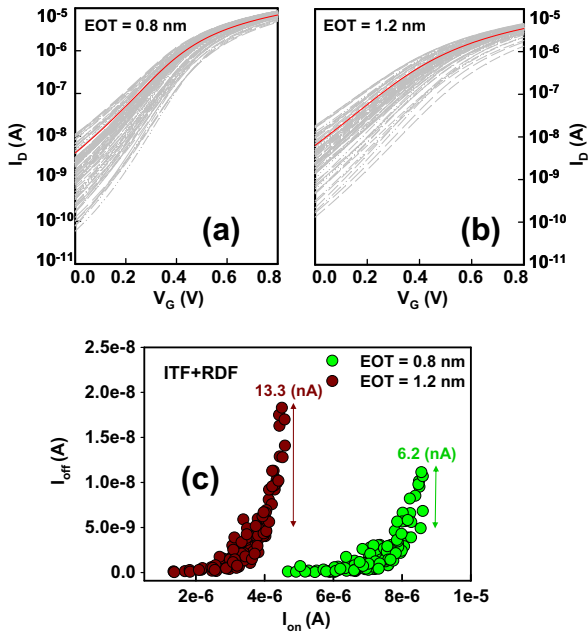
**3. Results and discussion**

Fig. 2 shows the on-state ( $V_G = 0.8 \text{ V}$  and  $V_D = 0.8 \text{ V}$ ) electric field and the potential distributions of the channel surface extracted from one of about 200 simulated transistors, where they are fluctuated by random ITs. The traps between the interface of Si and high- $\kappa$  irregularly twist the local electric field and the potential.

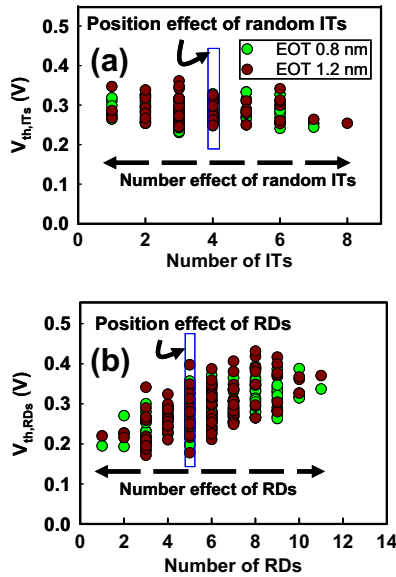


**Fig. 3.** The on-state ( $V_G = V_D = 0.8 \text{ V}$ ) potential distribution of the channel surface from one of simulated 16-nm transistors, where  $EOT = 0.8 \text{ nm}$ . The device fluctuated by six random "ITs + RDs" simultaneously. The interactions of two random ITs (at Si/HfO<sub>2</sub> oxide interface) and four random RDs (locating inside the silicon channel below the channel surface) on the band profile is clearly shown in the right plot.

Notably, the barrier is affected by ITF clearly. The barrier induced by RDs was discussed in our recent work [3]. Fig. 3 shows the on-state potential distribution of the channel surface extracted from one of about 200 simulated transistors fluctuated by random "ITs + RDs" simultaneously. The interaction effect of "ITs + RDs" on the band profile is clearly shown. Fig. 4(a) and (b) shows the totally random "ITs + RDs" fluctuated  $I_D - V_G$  curves simultaneously for N-MOSFETs with  $EOT$  of 0.8 and 1.2 nm, respectively. The plot of  $I_{on} - I_{off}$  characteristics for "ITs + RDs"-induced fluctuations is shown in Fig. 4(c). For devices with similar  $I_{on}$ , the maximum difference of  $I_{off}$  is declined from approximately 13.3 to 6.2 nA as the  $EOT$  is scaled from 1.2 to 0.8 nm. The result shows that the device with



**Fig. 4.** (a) and (b) The totally random ITs- and RDs-induced fluctuations of  $I_D$ - $V_G$  curves simultaneously for N-MOSFETs with EOT of 0.8 and 1.2 nm, respectively, where the red lines indicate the nominal cases (i.e., the 3D simulation without ITF and RDF). (c) The  $I_{on}$ - $I_{off}$  characteristics of about 200 simulated transistors fluctuated by ITs and RDs. For devices with similar  $I_{on}$ , the maximum difference of  $I_{off}$  is declined from approximately 13.3 to 6.2 nA as the EOT is scaled from 1.2 to 0.8 nm respectively.



**Fig. 5.** (a) and (b) The large-scale statistically computed  $V_{th}$  as a function of random traps' and dopants' number for the N-MOSFET devices with EOT of 0.8 and 1.2 nm, respectively. The random position effect of ITs- and RDs-induces rather different fluctuation in spite of the same number of ITs and RDs, as marked in the inset.

EOT of 1.2 nm possesses sizeable ITF and RDF due to the weakened metal gate controllability. The large scale statistically simulated threshold voltage as a function of random interface traps' and random dopants' number for the 16-nm N-MOSFET devices is shown in Fig. 5(a) and (b). Compared with ITs-number-induced  $\sigma V_{th}$ , the results imply that RDF influence  $\sigma V_{th}$  notably. From RDs-number

**Table 1**

Summary of the ITs-, RDs- and "ITs + RDs"-induced threshold voltage fluctuation. We note that the  $\sigma V_{th,ITs+RDs}$  is smaller than the result of statistically independent identical distribution  $\sqrt{\sigma^2 V_{th,ITs} + \sigma^2 V_{th,RDs}}$  due to a charges' correlation between random ITs and RDs in N-MOSFETs devices with EOT of 0.8 and 1.2 nm, respectively.

(nm)	$\sigma V_{th,ITs}$ (mV)	$\sigma V_{th,RDs}$ (mV)	$\sigma V_{th,ITs+RDs}$ (mV)
EOT = 0.8	26.3	43	45.4
EOT = 1.2	31.4	47.6	56.2

point of view, the equivalent channel doping concentration increases when the dopant number increases; this substantially alters the threshold voltage and the on/off state currents. Additionally, the position of ITs- and RDs-induces rather different fluctuation in spite of the same number of traps and dopants, as marked in inset of Fig. 5(a) and (b). Furthermore, the magnitude of spreading distance increases as the number of dopants increases. Table 1 summarizes the ITs-, RDs- and "ITs + RDs"-induced threshold voltage fluctuation; device with EOT of 0.8 nm exhibits  $\sigma V_{th,ITs}=26.3$  mV,  $\sigma V_{th,RDs} = 43$  mV and  $\sigma V_{th,ITs+RDs} = 45.4$  mV. We note that  $\sigma V_{th,ITs+RDs} = 45.4$  mV is smaller than the result of statistically independent identical distribution  $\sqrt{\sigma^2 V_{th,ITs} + \sigma^2 V_{th,RDs}} = 50.4$  mV due to a charges' correlation between ITF and RDF in N-MOSFETs. Physically, it implies that ITF and RDF should be considered at the same time for simulating HKMG device. Similarly, for device with EOT = 1.2 nm they are 31.4, 47.6 and 56.2 mV respectively.

**4. Conclusions**

In this study, we have explored the ITF and/or RDF with EOT of 0.8 and 1.2 nm on 16-nm HKMG planar MOSFETs. We have estimated the  $V_{th}$  as a function of trap number and dopant number for the N-MOSFET devices and ITs and RDs position induced different fluctuations of characteristics in spite of the same number of dopants and traps. The  $\sigma V_{th}$  induced by ITs is lower than that of RDs owing to a low density of acceptor-like interface traps. RDF dominates the characteristic fluctuation when considers both the ITF and RDF together. We currently calibrate the ranges of ITs' density and energy with experimentally measured results.

**Acknowledgments**

This work was supported in part by National Science Council (NSC), Taiwan under Contract No. NSC-99-2221-E-009-175 and by TSMC, Hsinchu, Taiwan under a 2010-2011 grant.

**References**

- [1] T. Mizuno, J. Okamura, A. Toriumi, IEEE Trans. Electron Devices 41 (1994) 2216–2221.
- [2] G. Roy, A.R. Brown, F. Adamu-Lema, S. Roy, A. Asenov, IEEE Trans. Electron Devices 53 (2006) 3063–3070.
- [3] Y. Li, S.-M. Yu, J.-R. Hwang, F.-L. Yang, IEEE Trans. Electron Devices 55 (2008) 1449–1455.
- [4] Y. Li, C.-H. Hwang, T.-Y. Li, M.-H. Han, IEEE Trans. Electron Devices 57 (2010) 437–447.
- [5] G. Panagopoulos, K. Roy, IEEE Trans. Electron Devices 58 (2011) 392–403.
- [6] A. Appaswamy, P. Chakraborty, J. Cressler, IEEE Electron Device Lett. 31 (5) (2010) 387–389.
- [7] P. Andricciola, H.P. Tuinhout, B. De Vries, N.A.H. Wils, A.J. Scholten, D.B.M. Klaassen, In: IEDM Tech. Dig. 711–714 (2009).
- [8] P.K. Hurley, K. Cherkaoui, S. McDonnell, G. Hughes, A.W. Groenland, Microelectron. Reliab. 47 (2007) 1195–1201.
- [9] M. Cassé1, K. Tachi1, S. Thiele, T. Ernst, Appl. Phys. Lett. 96 (2010) 123506.
- [10] M.F. Bukhori, S. Roy, A. Asenov, IEEE Trans Electron Devices Dev. 57 (2010) 795–803.