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Japanese Journal of Applied Physics
Vol. 47, No. 4, 2008, pp. 2438–2441

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Using Spike-Anneal to Reduce Interfacial Layer Thickness and Leakage Current in Metal–Oxide–Semiconductor Devices with TaN/Atomic Layer Deposition-Grown HfAlO/Chemical Oxide/Si Structure

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(Received October 1, 2007; accepted December 20, 2007; published online April 25, 2008)

In this study, the characteristics of Ta/chemical SiO_2/Si devices with their chemical oxides formed by various chemicals, including HNO_3, SC1, and H_2SO_4+H_2O_2 solutions, were first investigated. We found the HNO_3 split depicts the lowest leakage current and the best hysteresis behavior. Next, chemical oxide formed by HNO_3 was applied to form the interfacial SiO_2 layer for metal–oxide–semiconductor (MOS) devices with Ta/HfAlO/chemical SiO_2/Si structrue. The effects of a high-temperature spike anneal were then studied. We found that the spike-anneal process can effectively reduce the thickness of the chemical oxide from 10 to 7 Å, thus is beneficial in preserving the low effective oxide thickness (EOT) of the structure. Furthermore, both the gate leakage current and stress-induced leakage current (SILC) were also effectively suppressed by the high-temperature spike-anneal. [DOI: 10.1143/JJAP.47.2438]

KEYWORDS: chemical oxide, HNO_3, spike-annealing, ALD, HfAlO

1. Introduction

According to the ITRS Roadmap, the gate oxide thickness in 2007 is slated to reduce to 1.1 nm.[1)] However, the leakage current of nanometer-scale SiO_2 thin film is known to increase dramatically and becomes impractical because of large power dissipation. In recent years, high-*k* dielectric has obtained much attention as a potential candidate to replace SiO_2 gate insulator for very large scale integration (VLSI) applications.[2–7)] High gate capacitance or low equivalent oxide thickness thus can be achieved simultaneously with low gate current. Concurrently, one of the most promising deposition techniques for high-*k* materials is atomic layer deposition (ALD), as it is manufacturabe and provides excellent conformality and uniformity.[8,9)] For ALD, materials are deposited layer by layer in a self-limiting fashion, allowing for inherent atomic scale control. The most widely used ALD precursors for metal oxides are metal–chlorides, such as $HfCl_4$ and $Al(CH_3)_3$. Unfortunately, metal oxide formed by ALD using metal chloride precursors exhibits poor initial deposition on H-terminated Si, necessitating the use of an interfacial SiO_2 or Si_3N_4 layer to achieve uniform growth. This is expecially true for SiO_2 formed by chemical oxide, as it is without incubation period from the onset of the first pulse.[10)] However, the existence of an interfacial layer between the high-*k* layer and silicon substrate defeats the purpose of achieving low effective oxide thickness (EOT) and low gate current. Since an EOT of less than 1 nm will soon be required, the need for an initial few monolayers of a material with lower dielectric constant represents a serious drawback. Interfacial SiO_2 layers are conventionally grown by thermal oxidation at temperatures above 800 °C in O_2 or N_2O. The high performance of metal–oxide–semiconductor (MOS) devices relies on the nearly perfect Si/SiO_2 interfaces. However, the control of SiO_2 thickness becomes very difficult because of the high Si oxidation rate at high temperatures. In the present study, we will discuss the use of chemical oxide formed in HNO_3, SC1, or H_2SO_4+H_2O_2. A high-temperature spike-anneal treatment is proposed to reduce the chemical oxide thickness, making it suitable to serve as the interfacial layer of high-*k* dielectric. Characteristics of TaN/HfAlO/chemical oxide/Si devices are also compared and discussed.

2. Device Fabrication

The starting 6-in. Si(100) wafers with resistivity of 15–25 Ω cm were first cleaned using RCA methods. First to study the effects of various chemical oxides on the characteristics of TaN/chemical oxide/Si structures, the chemical oxide was formed by immersing wafers in different chemical solutions (i.e., HNO_3, SC1, or H_2SO_4+H_2O_2). Next, TaN layer was then formed in a physical vapor deposition (PVD) system, followed by rapid thermal anneal (RTA) at 850 °C for 30 s to serve as the gate electrode. Finally, Al was deposited on the backside of wafers by sputtering. Wafers then received a post-metal anneal (PMA) treatment at 400 °C for 30 min in forming gas. Next, MOS devices with TaN/HfAlO/chemical oxide/Si structures were fabricated, using chemical oxide formed by HNO_3 immersion. Briefly, chemical oxide was first formed by immersing wafers in nitric acid solutions, followed by various spike-anneal (i.e., 1000 and 1050 °C). Next, the HfAlO films were grown using ALD process, by alternating pulses of $HfCl_4$, H_2, O, and $Al(CH_3)_3$ at 300 °C. TaN layer was then formed in a PVD system, followed by RTA at 850 °C for 30 s to serve as the gate electrode. Finally, Al was deposited on the backside of wafers by sputtering. Wafers then received a PMA treatment at 400 °C for 30 min in forming gas. Current–voltage (*I*–*V*) characteristics were measured using an HP 4145 picoammeter, while capacitance–voltage (*C*–*V*) characteristics were recorded with an HP4284 at an operating frequency of 100 kHz.

3. Results and Discussion

Figure 1 shows *C*–*V* and hysteresis characteristics of the samples with TaN/Chemical SiO_2/Si(100) structure. The

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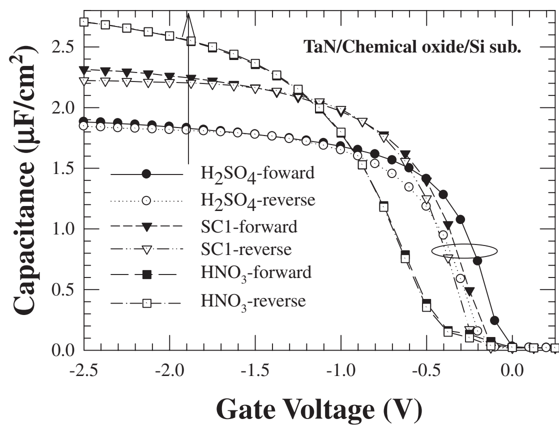


Fig. 1. C–V and hysteresis curves for TaN/chemical SiO_2/Si(100) with the SiO_2 layer formed in HNO_3, SC1, and H_2SO_4+H_2O_2, respectively.

SiO_2 layer was formed in HNO_3, SC1, and H_2SO_2+H_2O_2, respectively. It can be seen that with the same immersion time (i.e., 10 min), the HNO_3-split depicts the highest capacitance value. The hysteresis window, which may hinder the device application as it is an indication of MOS field-effect transistor (MOSFET) instability, was defined as the difference between flat-band voltages when the C–V curves were swept from 0.25 to −2.5 V and *vice versa*. From Fig. 1, the hysteresis window was found to be 137 mV for H_2SO_4+H_2O_2 split, 75 mV for SC1 split, and almost nil for the HNO_3 split. Table I shows the oxide thickness, gate leakage current (J_g, which was defined as $V - V_{FB} = -1$ V) for the three different chemical oxides. It is interesting to note that HNO_3 split has the lowest oxide thickness and J_g. Therefore, HNO_3–oxide, spike-annealed at either 1000 or 1050 °C, was chosen to form the interfacial oxide in all TaN/HfAlO/chemical SiO_2/Si(100) devices used in this study. Figure 2 shows C–V characteristics for TaN/HfAlO/chemical SiO_2/Si(100) devices. It can be seen that the EOT is reduced after the high-temperature spike-anneal as compared with ideal simulation results for the split without the spike anneal.[11] When the scaled chemical oxide get thinner, flatband voltage can shift toward ideal value.[12] In addition, the flatband voltages in Fig. 2 was different from those in Fig. 1, this may be due to the high-k dielectric stack on chemical oxide, which changed the EOT and trap density. To study the effect of spike anneal, high-resolution transmission electron

Table I. Oxide thickness, J (at $V - V_{FB} = -1$ V) for various chemical oxides.

Sample	Chemical oxide	EOT (Å)	J_g (A/cm^2) at $V - V_{fb} = -1$ V
1	H_2SO_4+H_2O_2	14.5	6.212
2	SC1	10.5	11.815
3	HNO_3	9	4.2881

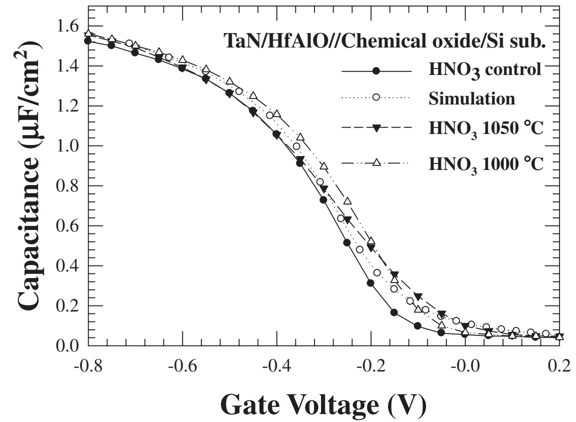


Fig. 2. C–V curves for TaN/HfAlO/chemical SiO_2/Si(100). The interfacial SiO_2 layer was formed in HNO_3, followed by a high-temperature spike-anneal (1000 and 1050 °C).

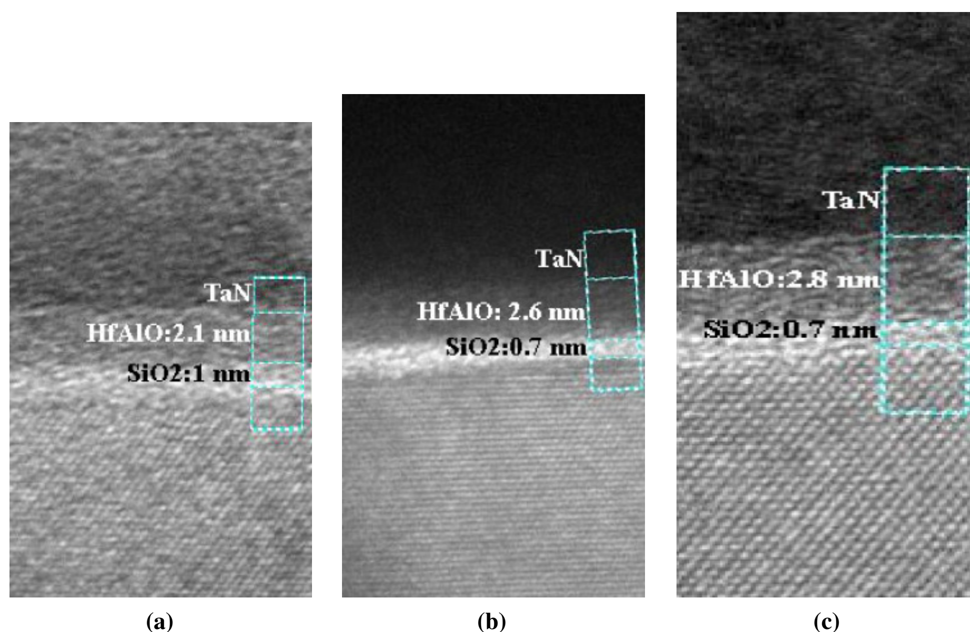
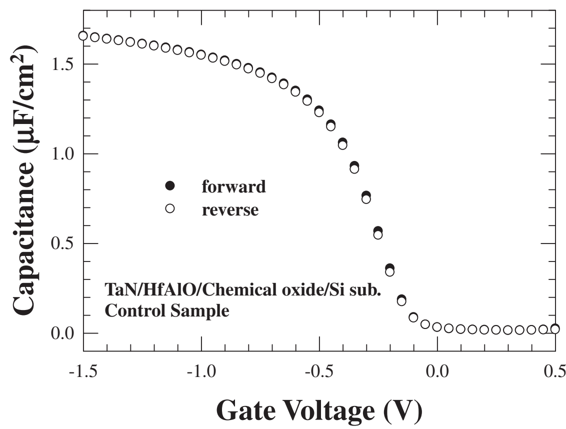


Fig. 3. (Color online) TEM pictures for interfacial layer: (a) without spike anneal, (b) with spike anneal at 1000 °C, and (c) with spike anneal at 1050 °C.



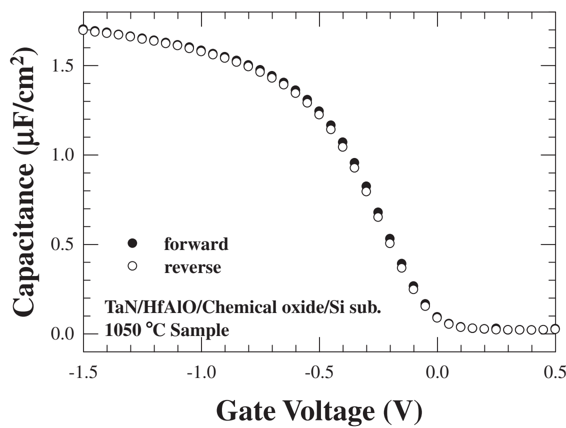


Fig. 4. C–V and hysteresis curves for TaN/HfAlO/chemical SiO_2/Si in (a) control sample without spike anneal and (b) sample with 1050 °C spike anneal.

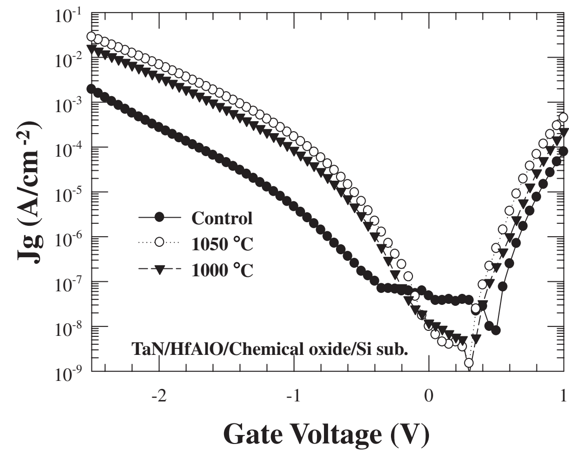


Fig. 5. Gate leakage current versus voltage for all splits.

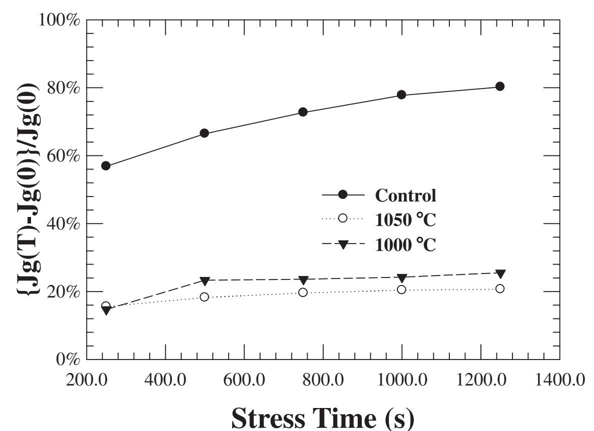


Fig. 6. SILC characteristics of TaN/HfAlO/chemical SiO_2/Si(100). SILC is defined as the increase in leakage current after stress [$J(T) - J(0)$] divided by leakage current of a fresh device [$J(0)$].

microscope (TEM) pictures of TaN/HfAlO/chemical SiO_2/Si(100) samples were analyzed. Figures 3 shows TEM pictures for interfacial layer (a) before and after spike anneal (b) 1000 and (c) 1050 °C in nitrogen ambient. It is worth noting that the splits with spike anneal, irrespective of the temperature (i.e., 1000 or 1050 °C), show a thinner physical thickness of 7 Å, compared with 10 Å for the split without the spike anneal. This indicates that HNO_3 chemical oxide could be effectively reduced by high temperature spike anneal. Figures 4 shows C–V and hysteresis curves for the TaN/HfAlO/chemical SiO_2/Si samples with and without spike anneal at 1050 °C. It can be seen that there is almost no hystersis difference for HNO_3 splits with or without high temperature spike anneal. Therefore, the threshold voltage instability could be ignored. Figure 5 shows gate leakage current characteristics. The splits with high temperature spike anneal show higher gate current due to its thinner interfacial oxide thickness. However, the leakage current is suppressed at 0 V gate voltage. We believe this is because the interface states are suppressed after spike anneal. Figure 6 shows stress induced leakage current (SILC) characteristics of TaN/HfAlO/chemical SiO_2/Si sample. SILC is defined as the increase in leakage current after stress [$J(T) - J(0)$] divided by the fresh leakage current, where $J(T)$ is leakage current density after stress, and T is stressing time. $J(0)$ is leakage current of a fresh. Note that SILC is also suppressed for the splits with high temperature spike anneal. It is due to the reduction of interface traps after spiking anneal, as shown in Fig. 5.

4. Conclusions

Chemical oxidation grown on silicon by different chemicals is investigated in view of its application to gate oxides. HNO_3–oxide depicts the thinnest thickness and the lowest leakage current among all chemical oxide splits. Furthermore, a high temperature spike anneal not only reduces the thickness of HNO_3 chemical oxide, but also suppresses the gate leakage current and SILC owing to reduced donor-like interface traps.

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