

Extraction of Eleven Model Parameters for Consistent Reproduction of Lateral Bipolar Snapback High-Current $I-V$ Characteristics in NMOS Devices

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Abstract—A series of literature models originally devoted to the second breakdown trigger current I_{t2} in a grounded-gate nMOS transistor can further find promising potential in handling high-current $I-V$ due to lateral bipolar snapback. This is achieved primarily by building significant linkage between bipolar current-gain β -related parameters: 1) the collector-to-base junction voltage dependencies A_1 and A_2 of the medium-level injection β roll-off factor; 2) the high-level β roll-off factor A_3 ; and 3) the collector-to-base junction voltage dependencies A_4 and A_5 of the collector corner current at the onset of high-level β roll-off. The new parameters A_1 to A_5 enable a consistent $I-V$ solution along with other existing six model parameters such as the substrate resistance R_{sub} and its conductivity modulation factor A_r , the impact ionization coefficients K_1 and K_2 , and the emitter series resistance R_e and collector series resistance R_c . Parameter extraction except R_c is thoroughly performed using only the parametric analyzer, and opposed to the traditional procedure, impact ionization coefficients and current gains are all assessed without entering the snapback regime. Remarkably, not only excellent agreements are gotten, but also bipolar snapback $I-V$ measured under the current pulsing condition can be separated into two distinct parts: medium- and high-level injection region. This is quite effective under $R_e = R_c$. Series resistance, although having very low value, is not to be absent under the high-level injection conditions. Experimental evidences from test structures with different epitaxial layer thicknesses strongly confirm the validity of the assumptions such as $R_e = R_c$. In light of the epitaxial layer thickness dependencies of the model parameters, the epitaxial layer thickness effect is addressed as well.

Index Terms—Bipolar, electrostatic discharge (ESD), MOS, second breakdown, snapback.

I. INTRODUCTION

THE grounded-gate nMOS transistor is one of the widely utilized input/output (I/O) devices [1] since it can be snapped back into the lateral bipolar high-current conduction state in an electrostatic discharge (ESD) event. In case of ESD Human-Body-Mode, the current discharging waveform

can adequately be approximated by a pulse with width in the order of several hundreds of nanoseconds [2]; and under such current pulsing or transmission-line-pulsing (TLP) condition, the measured lateral bipolar snapback high-current $I-V$ characteristics can provide information about ESD transient energy the device is carrying away [2]. This is valid until the second breakdown trigger current I_{t2} is encountered. Thus, characterization and modeling of high-current $I-V$ due to lateral bipolar snapback is essential. There exist a series of models in the literature originally devoted to I_{t2} :

- 1) a substrate current model [3], [4], with the substrate resistance R_{sub} , and the conductivity modulation factor A_r , as parameters;
- 2) an avalanche generation model [3]–[5] with the impact ionization coefficients K_1 and K_2 as parameters for the multiplication factor M ;
- 3) a lateral bipolar high-level injection current-gain β model [4], [6], with the roll-off factor A_o as the primary parameter. R_{sub} , M , and β , all extracted from a single nMOS transistor in terms of dc drain current versus drain voltage curve containing a snapback regime [3], [7], were shown to be well related to I_{t2} [4], [7].

This indicates the potential of a wafer-level process monitor [4], [7] in tracing ESD robustness capability to process tuning or device redesign, greatly reducing the load of the destructive characterization equipment like current pulse generator, high-voltage generator, switcher, and oscilloscope. Despite these striking achievements, the models themselves indeed fail to stand up in producing $I-V$ of interest due to the lacking in the linkage between parameters.

The goal of the work is to highlight another promising potential of the aforementioned models in handling lateral bipolar snapback high-current $I-V$. This is achieved by recovering the linkage between parameters. First of all, A_o is replaced by five ones: the collector-to-base junction voltage dependencies A_1 and A_2 of the bipolar medium-level injection β roll-off factor, the high-level β roll-off factor A_3 , the collector-to-base junction voltage dependencies A_4 and A_5 of the collector corner current at the onset of high-level β roll-off. The new parameters A_1 to A_5 enable a consistent solution of $I-V$ characteristic along with other existing six model parameters such as R_{sub} , A_r , K_1 , K_2 , and the series resistance [8]–[11] R_e in emitter and R_c in collector. Parameter extraction except R_c is thoroughly performed using only the parametric analyzer, and opposed to the traditional procedure [3], [7], impact ionization coefficients

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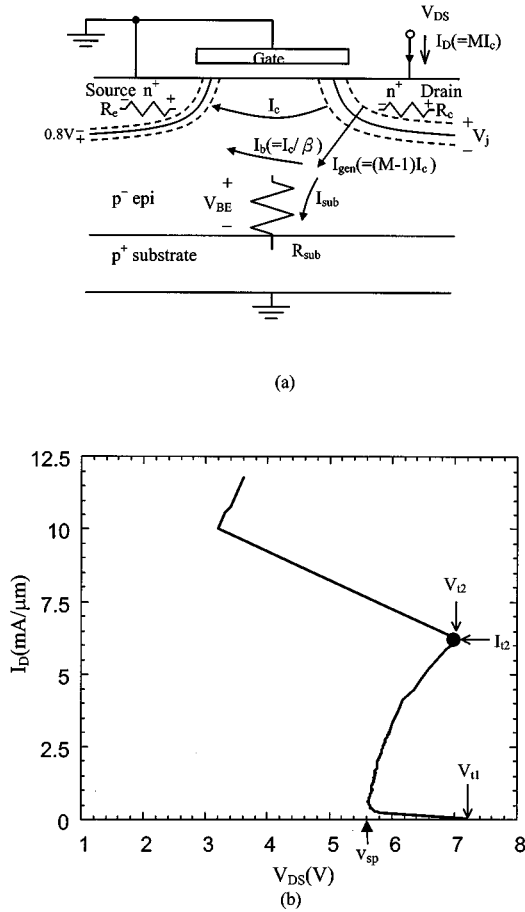


Fig. 1. (a) Schematic cross section of a grounded-gate nMOS transistor. The distinct current components and paths after snapback takes place are denoted. The potential drops are labeled as well. (b) Experimental I - V characteristic curve illustrating the avalanche voltage V_{t1} , the snapback voltage V_{sp} , the second breakdown triggering voltage V_{t2} and current I_{t2} , and the second breakdown regime.

and current gains are all assessed without entering the snapback regime. Moreover, traditionally applying an external forward bias was reported to be weak in measuring real β [5], [12]; however, in this paper, we alternatively characterize β as a function of the drain-to-substrate junction voltage and reasonably extract the impact ionization induced generation current in a consistent manner. As a result, remarkably excellent agreements are gotten while comparing lateral bipolar snapback I - V measured under the current pulsing condition. Series resistance, although having very low value, is not to be absent under the high-level injection conditions. Experimental evidences from test structures with different epitaxial layer thicknesses furnish strong supports to the assumptions behind the models. The epitaxial layer thickness effect is also addressed in light of the epitaxial layer thickness dependencies of the model parameters.

II. MODEL CITATION

Fig. 1 schematically shows the cross-sectional view of a grounded-gate nMOS device. Also attached is the experimental I - V characteristic curve including second breakdown regime, as explained in later sections. For device initially in off-state, increasing drain voltage to approach the avalanche voltage V_{t1}

can produce a significant substrate current I_{sub} via avalanche generation, which in turn develops a potential drop across the substrate resistance R_{sub} . As the substrate potential drop forward biasing the substrate-to-source junction rises to a certain criterion V_{BE} , the parasitic lateral bipolar turns on, and the drain voltage has to be lowered to around the snapback voltage V_{sp} such as to sustain the subsequent drain current. Then, the device enters into the so-called self-biased mode, that is, as depicted in Fig. 1(a), the bipolar electron current I_c collected at the edge of the substrate-to-drain junction is amplified by a multiplication factor M to constitute the drain electron current $I_D (= MI_c)$, and the substrate hole current $I_{sub} (= (M-1)I_c - I_c/\beta)$ and the base hole current $I_b (= I_c/\beta)$ both are provided by the generated hole current $I_{gen} (= (M-1)I_c)$. Such relation mathematically leads to [4]

$$M = \frac{(\beta + 1)}{\beta \left(1 - \frac{I_{sub}}{I_D}\right)}. \quad (1)$$

There exists a compact model relating the drain-to-substrate junction voltage V_j to M [4]

$$V_j = \frac{K_2}{\ln \left(\frac{K_1}{1 - \frac{1}{M}} \right)}. \quad (2)$$

I_{sub} can readily be calculated using a substrate current model [3], [4], but with parameter redefined for including R_e : $I_{sub} = A_r I_D + V_{BE}/R_{sub}$ where $V_{BE} = 0.8V + (1 + 1/\beta)R_e I_D/M$. As a result, $I_{sub} = (A_r + (\beta + 1)R_e/\beta M R_{sub})I_D + 0.8V/R_{sub}$. The parasitic lateral bipolar current-gain β roll-off was usually approximated by a simple form $\beta = A_o/I_C$ [4], [6]; as demonstrated later, however, such formulation is far away from the reality due to lacking of the linkage to junction voltage, making a consistent I - V solution improbable. To further cover the medium- and high-level regimes, a set of five parameters instead of single A_o is subsequently introduced. As a result of parameter expansion, V_j can be consistently solved from (1) and (2). Thus, summing all known or calculated potential drops from drain to substrate terminal for given I_D creates a model for the lateral bipolar snapback I - V under investigation

$$V_{DS} = I_D R_e + V_j + V_{BE}. \quad (3)$$

III. CHARACTERIZATIONS AND PARAMETER EXTRACTION

The nMOS test transistors were formed on a p-type epitaxial layer on p+ substrate. The gate oxide was grown to a thickness of 70 Å. Phosphorous ($6.0 \times 10^{12} \text{ cm}^{-2}$, 30 KeV) and then Arsenic ($4.0 \times 10^{13} \text{ cm}^{-2}$, 45 KeV) were implanted to form the low-doped source/drain, followed by Arsenic implant ($4.4 \times 10^{15} \text{ cm}^{-2}$, 40 KeV) for the highly doped n+ source/drain. Three different epitaxial layer thicknesses of 2, 4, and 5 μm were presented. The corresponding thickness values were measured after the processing by a spreading resistance probe. The gate width to length ratio selected in this work was 20 μm/0.3 μm for the threefold goals:

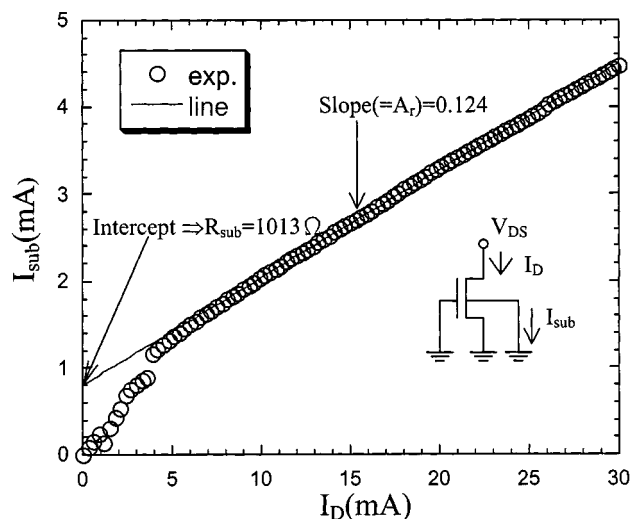


Fig. 2. Scatter plot between measured substrate current and drain current. A straight line fitting data points for $I_D > 4$ mA is drawn. The inset depicts the test configuration.

- 1) wafer-level parameter extraction using a parametric analyzer;
- 2) wafer-level measurement of bipolar snapback $I-V$ curve down to off-state using the same parametric analyzer with the equipment limit of 100 mA;
- 3) wafer-level measurement of bipolar snapback high-current $I-V$ curve and extension up to second breakdown regime using a current pulse generator with the equipment limit of 1 A. Unless stated otherwise, the 4- μ m thick epitaxial layer structure is first concentrated.

The parametric analyzer Keithley 236 was used to perform characterizations and parameter extraction on the same sample. First of all, the biasing condition for R_{sub} and A_r was tying source, gate, and substrate to ground. The drain current and substrate current were measured against drain voltage, and their correlation is plotted in Fig. 2. It can be seen that almost all data points for $4 \text{ mA} < I_D < 30 \text{ mA}$ fall exactly on a straight line. The slope and intercept of that line represent A_r and $0.8 \text{ V}/R_{sub}$, respectively. Note that within the current range illustrated in Fig. 2, $A_r \gg (\beta + 1)R_e/\beta MR_{sub}$, as evaluated using the quantities later. To extract K_1 and K_2 , the test device was biased in above threshold and the measured drain current versus drain voltage for different gate voltages is depicted in Fig. 3(a). The multiplication factor M in the avalanche region can be characterized by [5], [11]

$$M = \frac{1}{1 - K_1 \exp\left(\frac{-K_2}{V_{DS} - V_{DS,SAT}}\right)} \quad (4)$$

where $V_{DS,SAT}$ is the drain saturation voltage at the pinchoff point. The $V_{DS,SAT}$ value can be readily gotten by transforming the $I-V$ curves ($0 < V_{DS} < 1.5 \text{ V}$ in Fig. 3(a), for instance) free of avalanche generation to another function G according to [13]–[15]

$$G = g_{DS} \frac{\partial}{\partial V_{DS}} \left(\frac{1}{g_{DS}} \right) \quad (5)$$

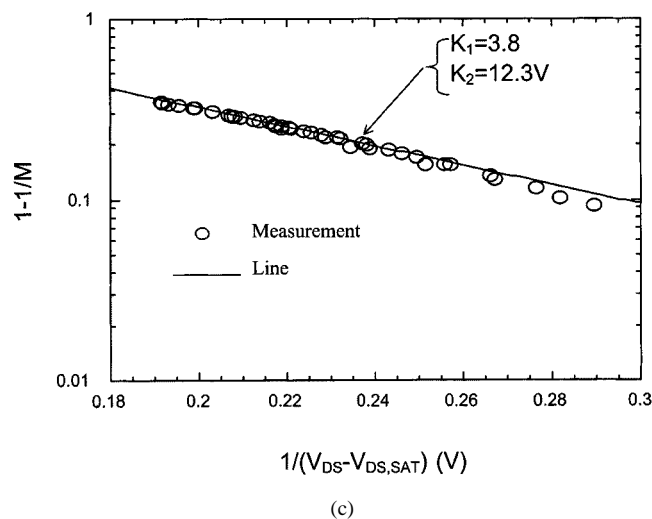
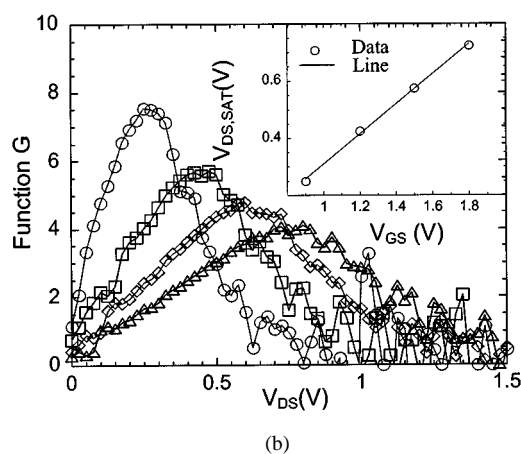
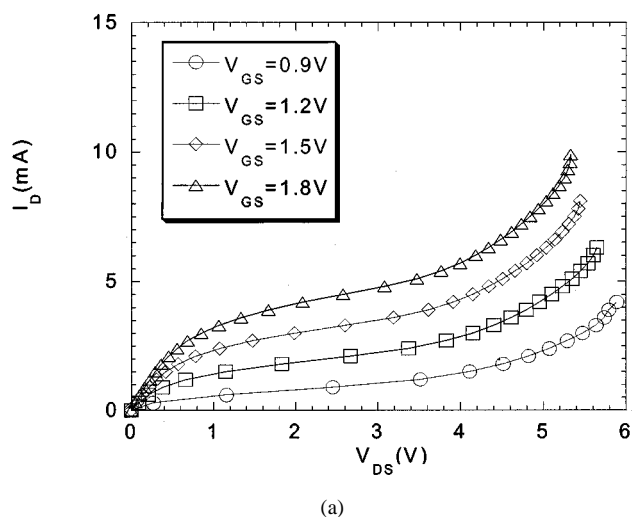


Fig. 3. (a) Measured nMOS transistor output $I-V$ characteristics for gate voltages over threshold voltage. (b) Transformed G versus V_{DS} for different V_{GS} . The inset depicts the extracted $V_{DS,SAT}$ versus gate voltage. (c) Extracted $(1 - 1/M)$ versus $1/(V_{DS} - V_{DS,SAT})$ along with a straight line for determination of K_1 and K_2 .

where $g_{DS} = \partial I_{DS}/\partial V_{DS}$ is the conductance of the device. The resulting G versus V_{DS} is depicted in Fig. 3(b), where a peak G takes place at $V_{DS,SAT}$. The extracted $V_{DS,SAT}$ versus V_{GS} is plotted in the inset of Fig. 3(b), suggesting a linear relationship between the two. Then the $I-V$ part in the avalanche

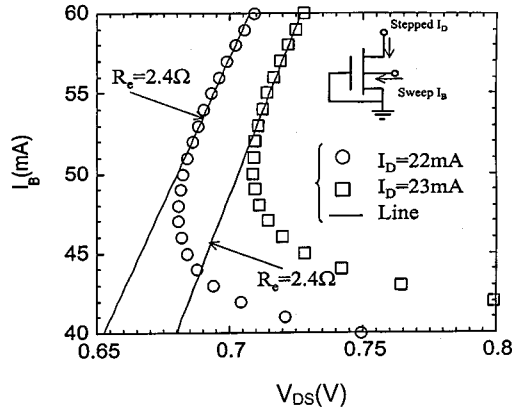
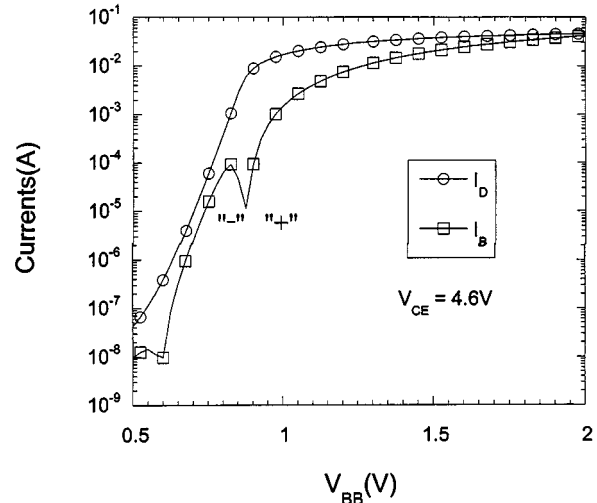


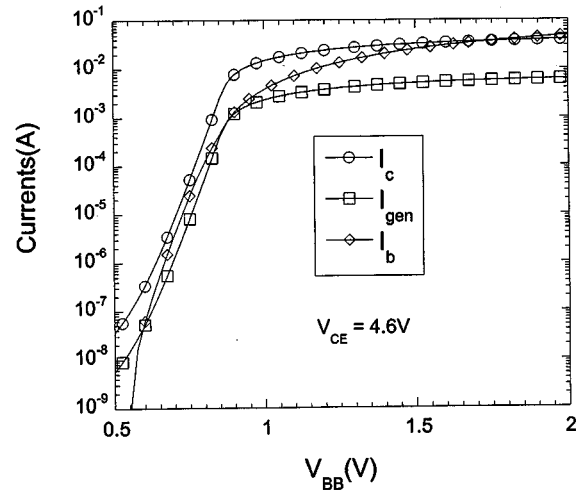
Fig. 4. Set-up of extracting the emitter series resistance as well as the measurement results.

regimes (not entering the snapback) in Fig. 3(a) were transformed to $(1 - 1/M)$ in log scale versus $1/(V_{DS} - V_{DS,SAT})$ in Fig. 3(c), from which a straight line is drawn along with extracted K_1 and K_2 . The technique of extracting the emitter resistance R_e is well defined in a bipolar transistor [6]: sweeping I_B for fixed I_D while monitoring V_{DS} , as shown in the inset of Fig. 4. The devices burn out if I_B exceeds about 70 mA. The measurement results for $I_B < 60$ mA are shown in Fig. 4, where the inverse of the slope near the knee of I_B versus V_D is around 2.4Ω . In spite of distinct bias modes in two junctions, to facilitate the analysis we made first order approximation of $R_c = R_e$ based on the symmetry of the n^+ diffusion regions. This also implies that the series resistance involved is located in certain part of diffusion regions where injection is insignificant. Strong experimental evidences supporting this assumption is presented later.

The biasing condition for bipolar current-gains is that, with grounded source and gate, an external forward bias V_{BB} was applied to the substrate while a reverse bias of V_{CE} was connected to the drain. Fig. 5(a) shows the measured drain terminal current I_D and bulk terminal current I_B versus V_{BB} at $V_{CE} = 4.6$ V. It can be seen that a bulk current reversal phenomenon like that in [16] (e.g., the avalanche generation bulk component exceeds the traditional base current component for recombination in the base and injection into the emitter) occurs for $V_{BB} < 0.9$ V. Both I_D and I_B can be transformed to I_c and I_b , respectively, according to the formula: $I_D = I_c M$; $I_{gen} = (M - 1)I_c$; and $|I_B| = I_{gen} - I_b$ for $V_{BB} < 0.9$ V and $I_B = I_b - I_{gen}$ for $V_{BB} > 0.9$ V. The resulting current components are depicted in Fig. 5(b) for clarification. Fig. 6 displays the resultant current gains versus collector current with V_{CE} as a parameter. First of all, the traditional $\beta_1 = A_o/I_c$ is found to dominate the medium-level current regime as fitted in Fig. 6(a). The extracted A_o versus V_j is given in Fig. 7(a), where a fitting line of $A_o = A_1(V_j - A_2)$ is drawn. One plausible explanation for such V_j dependencies is that, due to Early effect, an increase in V_j narrows the base width and thus increases current gain. Note that V_j was transferred from V_{CE} using the potential drop relation $V_{CE} = V_j + 0.8V + (I_E R_e + I_D R_c)$, and again to simplify the analysis, the average value of $I_E R_e + I_D R_c$ was roughly 0.2 V for the current range of interest in Fig. 5, namely,



(a)



(b)

Fig. 5. (a) Measured drain terminal current and bulk terminal current and (b) the extracted collector current, base current, and generation current, all versus external forward bias V_{BB} at $V_{CE} = 4.6$ V.

10 to 70 mA. Returning back to Fig. 6(a), one can see that 1) as V_{CE} increases, the deviation of β_1 is more pronounced in the high-level injection regime and 2) for $V_{CE} > 4.9$ V, current gain seems to shift toward the direction of increasing collector current as characterized by an increase in the collector corner current I_{co} at the onset of β roll-off [10]. Thus, we adopt the other form as cited in [10] for the high-level current gain β_2

$$\beta_2 = 1/A_3(I_c - I_{co}). \quad (6)$$

The fitting lines of (6) are drawn in Fig. 6(b), yielding $A_3 = 30 \text{ A}^{-1}$; and the extracted I_{co} is plotted in Fig. 7(b) versus V_j . Similarly, I_{co} can be empirically related to V_j through $I_{co} = A_4(V_j - A_5)$

IV. CURRENT PULSING $I-V$ MEASUREMENT AND REPRODUCTION

Equipment HP8114A with the upper limit of 1 A generated out a 400-ns wide current pulse to force entering the drain of

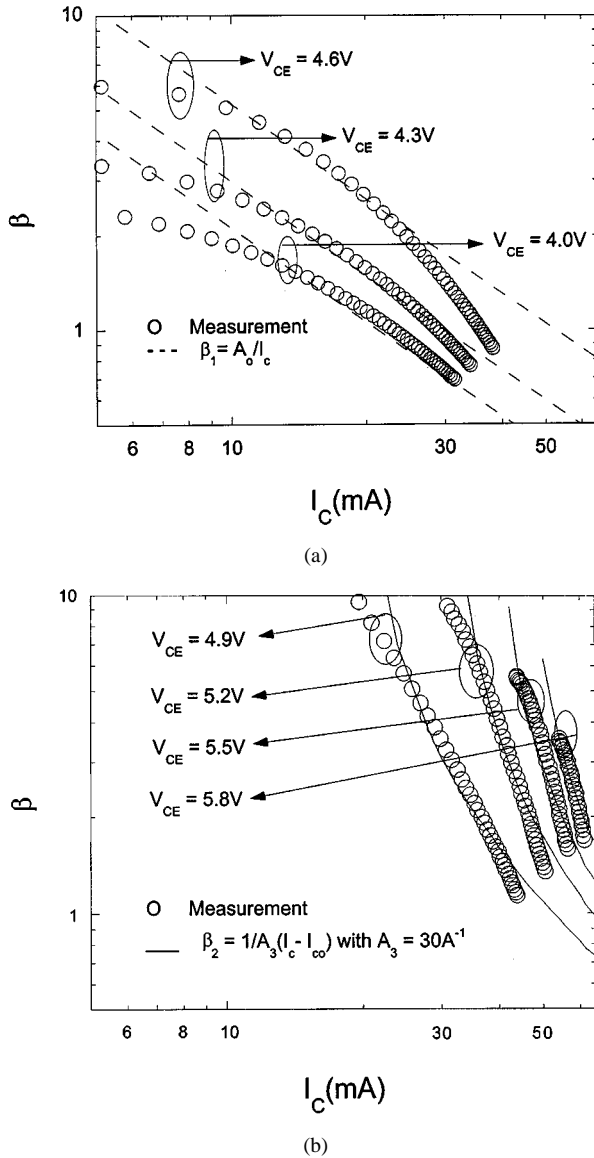


Fig. 6. Extracted current gains versus collector current for (a) V_{CE} of 4.0 to 4.6 V and (b) V_{CE} of 4.9 to 5.8 V. The fitting lines are shown for extraction of A_o , A_3 , and I_{co} .

the sample with gate grounded. A digital oscilloscope Tek744A recorded the transient waveforms of the drain current (via a CT-1 current probe) and drain voltage. Fig. 8(a)–(c) displays the measured waveforms for three increasing pulse heights corresponding, respectively, to the self-biased point, the second breakdown trigger point, and the second breakdown quasi-stable point. It can be observed that initially the device experiences the dynamic process starting from off-state through the avalanche point to the negative resistance regime, and eventually it enters the steady state in the remaining pulse width. In particular, in Fig. 8(b), a sudden drop in V_{DS} accompanying a rise in I_D during the subsequent decay is noticeable, evidencing the second breakdown trigger point. The corresponding steady-state $I-V$ is plotted in Fig. 1(b). It is worth noticing that between the second breakdown trigger point and the snapback point, there exists a critical point separating the $I-V$ into two distinct parts. The product of the second breakdown trigger voltage V_{t2} and I_{t2} herein is 45 mW/um, quite close to those reported with the same

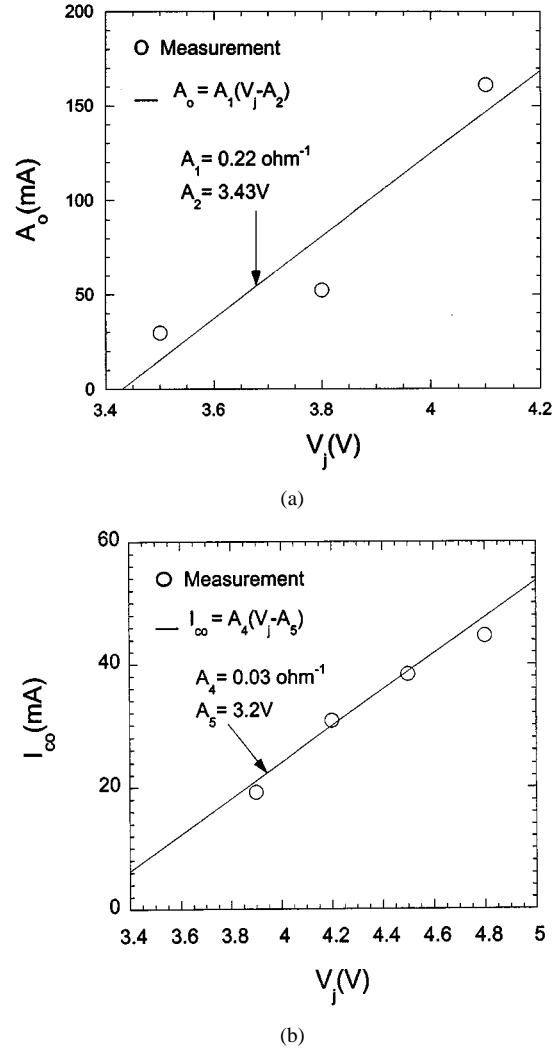


Fig. 7. (a) Extracted A_o versus V_j . A straight line is drawn for assessment of A_1 and A_2 . (b) Extracted I_{co} versus V_j . A straight line is drawn for assessment of A_4 and A_5 .

pulse width [4]. Additional equipment Keithley 236 with a maximum allowable current limit of 100 mA was also used to characterize the other samples (different locations on the same wafer) and the resulting $I-V$ down to off-state is together plotted in Fig. 1(b) for comparison. It can be seen that both have consistent overlap. This rather confirms the validity of the present current pulsing measurement technique. It is also noteworthy that since Keithley 236 has a much longer pulse width during the measurement, a catastrophic failure is easily produced in samples for currents exceeding only around 70 mA.

Substituting extracted parameters into the models, two $I-V$ curves were created for medium-level β_1 and high-level β_2 , as shown in Fig. 9 along with experimental $I-V$. Strikingly, excellent reproductions are obtained. This is rigorously achieved without adjusting any parameters. Obviously, the mentioned separation of experimental $I-V$ in Fig. 1(b) into two distinct parts can be adequately attributed to the two different operating regions, namely, the medium-level injection region and the high-level injection region. This suggests that an adequate tradeoff can be made between medium- and high-level current

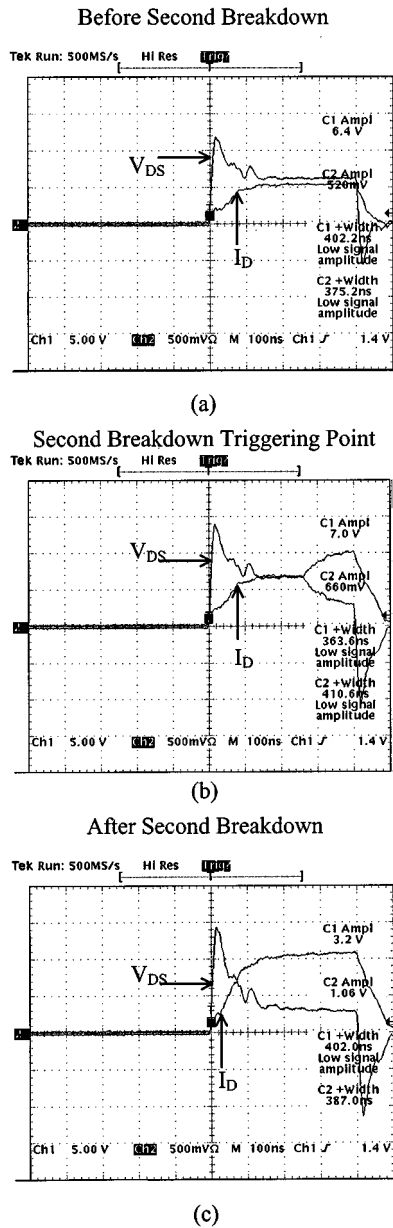


Fig. 8. Measured waveforms of drain current and drain voltage corresponding to current pulse heights of (a) 100 mA; (b) 130 mA; and (c) 210 mA.

regimes: $1/\beta = 1/\beta_1 + 1/\beta_2$. Also plotted in Fig. 9 is an extra calculation in high-level injection for $R_e = 0$ and $R_c = 0$. Surprisingly, ignoring series resistance indeed produces a serious deviation of the real $I-V$ curve. Thus, series resistance, although very low value as that in our study, is not to be absent under the high-level injection conditions, confirming the role of R_e and/or R_c reported elsewhere [8]–[11].

In the presence of excellent reproduction demonstrated above, however, some issues associated with the eleven-parameters-based models must be addressed. First, the reproduction is apparently effective under $R_e = R_c$. Second, the gate width is utilized for calculation, indicating the current distribution uniformity along the gate width or peripheral direction. The final problem rises in nature: the parameters extracted and measured in dc parametric analyzer could be suitable for

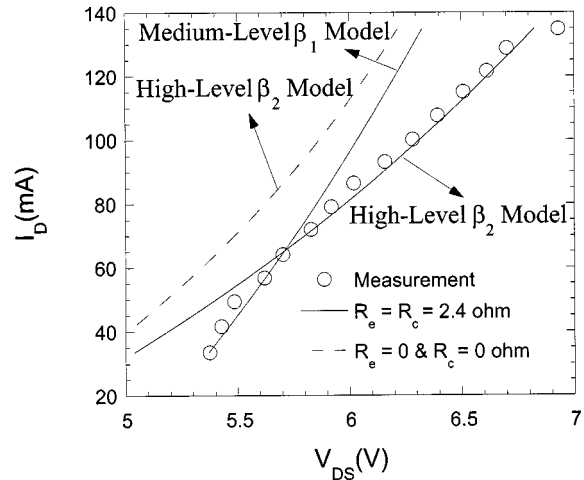


Fig. 9. Experimental $I-V$ characteristics and calculated results for two current-gain injection models. $R_e = R_c = 2.4 \Omega$. Also plotted is the high-level injection calculation for $R_e = 0$ and $R_c = 0$.

reproducing $I-V$ measured via current pulsing technique. Prior to answering these problems, it must be recognized that what we are faced with is a highly challenging area where very complex, sophisticated phenomena occur in an ESD event and each may play significant roles in terms of electrical-thermal coupling, three-dimensional distributing current and potential, and current filament formation. Even self-heating may considerably participate during extracting dc parameters. With this in mind, if any noticeable deviations would occur, one could trace back deviations to certain assumption and/or could evaluate the degree of deviations produced and relate them to that assumption. Strictly speaking, only more experimental evidences can be useful in this matter. This is presented below in terms of the epitaxial layer thickness effect.

V. EPITAXIAL LAYER THICKNESS EFFECT

Again, following the same procedure of device characterization and parameter extraction for the other structures having epitaxial layer thicknesses of 2 and 5 μm , comparable results do turn out, as depicted in Fig. 10. This is achieved again without any parameter adjustment. Thus, it is concluded that the assumptions behind the models are quite adequate and reasonable. Note that some serious deviations appear in the vicinity of the second breakdown trigger point, which may be attributed to current filament formation or others. Comparing both Figs. 9 and 10, one can see that $I-V$ curve shifts toward the increasing drain voltage with decreasing epitaxial layer thickness. Now we explain such effect in terms of the epitaxial-layer-thickness dependent model parameters. Fig. 11 depicts the measured $I-V$ of extracting R_e for epitaxial layer thicknesses of 2 and 5 μm . Again, comparing Figs. 4 and 11, it is argued that R_e increases with decreasing epitaxial layer thickness. This tendency is arisen from out-diffusion extension from underlying p^+ heavily doped substrate as supported by measured doping profile, which in turn narrows the quasi-neutral diffusion region. Under the same influence, due to structure symmetry another series resistance should show the same

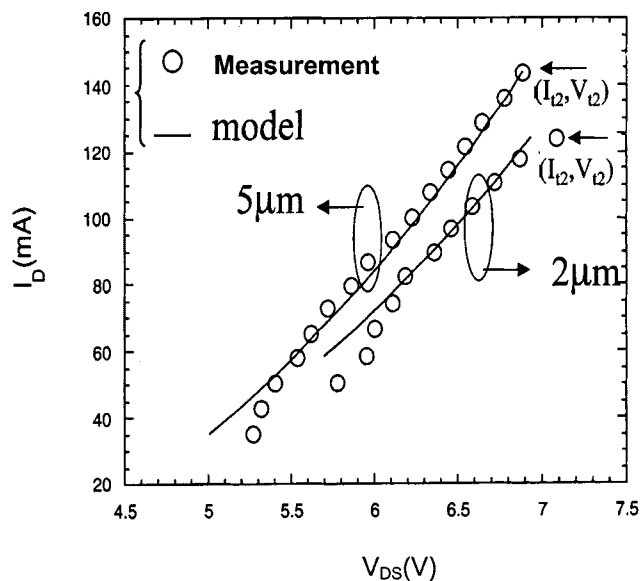


Fig. 10. Experimental $I-V$ characteristics and calculated results for high-level injection current gain model. $R_e = R_c = 3.1 \Omega$ for epitaxial layer thickness of $2 \mu\text{m}$ and $R_e = R_c = 2.1 \Omega$ for $5 \mu\text{m}$.

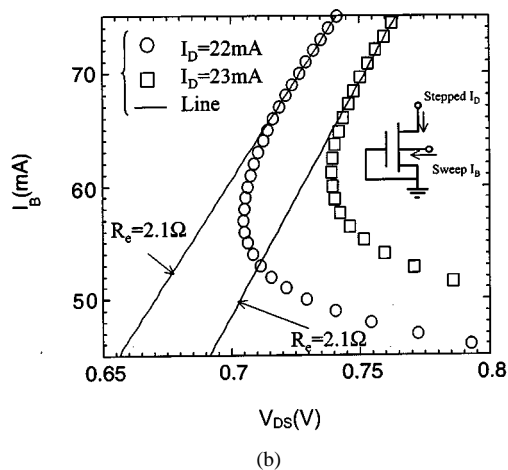
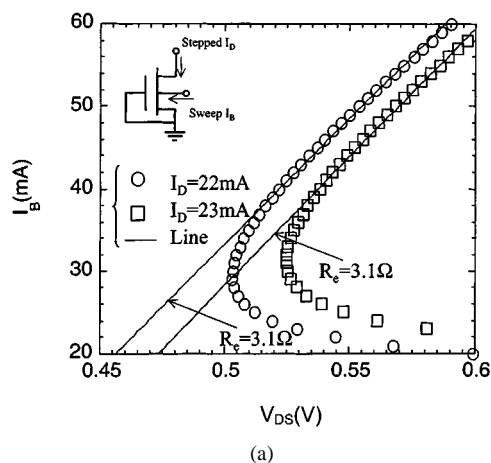


Fig. 11. $I-V$ of extracting the emitter series resistance for structures having epitaxial layer thickness of (a) $2 \mu\text{m}$ and (b) $5 \mu\text{m}$.

behavior. This naturally serve as a strong evidence of $R_e = R_c$ as employed in our work.

TABLE I
THE EXTRACTED PARAMETER VALUES FOR THREE DIFFERENT EPITAXIAL LAYER THICKNESSES. CURRENT-GAIN PARAMETERS ONLY IN THE HIGH-LEVEL INJECTION REGION ARE LISTED

Epitaxial Layer Thickness	R_{sub}	A_r	K_1	K_2	A_3	A_4	A_5	R_e
2 μm	987 Ω	0.158	3.8	12.3	18 A^{-1}	0.021 Ω^{-1}	2.70 V	3.1 Ω
4 μm	1013 Ω	0.124	3.8	12.3	30 A^{-1}	0.030 Ω^{-1}	3.20 V	2.4 Ω
5 μm	1065 Ω	0.103	3.8	12.3	40 A^{-1}	0.031 Ω^{-1}	3.22 V	2.1 Ω

Table I lists in part the extracted parameter values for different epitaxial layer thicknesses. This table reveals some dependencies of relevance. First, impact ionization coefficients are intact, indicating that the mentioned out-diffusion does not extend significantly to the surface beneath the gate, or its range is quite limited to around the bottom n^+ diffusion to p-type epitaxial layer junction. Second, the substrate resistance decreases with decreasing epitaxial layer thickness, as expected. According to the models, either increasing series resistance or decreasing substrate resistance can shift the $I-V$ toward positive drain voltage. This is because the former can increase the potential drop across the series resistance, while a bipolar current increase is accompanied with the latter to maintain the same substrate potential drop, which in turn increases the potential drop from drain to source. Relative to other parameters, an analysis simply judges out the series resistance and substrate resistance both as primary contributing factors to the above epitaxial layer thickness effect.

VI. CONCLUSION

We have demonstrated in detail one promising potential of the well-recognized literature models in dealing with the lateral bipolar snapback high-current $I-V$ of a grounded-gate NMOS transistor. This is achieved by building significant linkage between parameters such as to enable a consistent solution of a snapback $I-V$ curve. Experimental evidences from structures with different epitaxial layer thicknesses give strong supports to the assumptions used. The epitaxial layer thickness effect is also addressed in light of the epitaxial layer thickness dependencies of the model parameters.

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