Physical and Electrical Characteristics of F- and C-Doped Low Dielectric Constant Chemical Vapor Deposited Oxides

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This work compares the physical and electrical properties of two species of inorganic low dielectric constant (low-*k*) chemical vapor deposited (CVD) oxides, F-doped fluorinated silicate glass (FSG, $k = 3.5$) and C-doped organosilicate glass (OSG, $k = 2.9$). Experimental results indicate that FSG has a higher thermal stability ($>600°C$) than OSG ($500°C$), based on the results of thermal annealing for 30 min in an N_2 ambient. The degradation of the low-*k* property in OSG is mainly due to the thermal decomposition of methyl ($-CH_3$) groups at temperatures above $500°C$. For the Cu gated oxide-sandwiched low-*k* dielectric metal-insulator-semiconductor (MIS) capacitors, Cu penetration was observed in both FSG and OSG after the MIS capacitors were bias-temperature stressed at 250 and $150°C$, respectively, with an effective applied field of 0.8 MV/cm. Specifically, Cu appeared to drift more readily in OSG than in FSG, presumably because OSG has a more porous and less dense structure than FSG. The Cu permeation can be impeded by a thin nitride (SiN) barrier layer.

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As the feature size of the device shrinks to below 0.18 μm with multilevel interconnections, using low dielectric constant (low-*k*) materials as intermetal dielectrics to ameliorate the significant increase of parasitic capacitance, crosstalk interference and dynamic power consumption becomes inevitable.[1] Although replacing Al alloys with Cu offers the potential for devices that are 30% faster, and have fewer metal levels and are cheaper to produce, attaining high device yields on chips with Cu interconnects remains a great challenge, making low-*k* the vital factor in achieving high performance ultralarge-scale integrated circuits.[2] Low-*k* ($k < 3.0$) dielectrics are currently being extensively developed on both organic (carbon-based) and inorganic (SiO_2-based) materials using both spin-on (SO) and chemical vapor deposition (CVD) techniques.[1-10] Although spin-on is the most widely used method, low-*k* films grown by CVD are recently receiving widespread attention for potential back-end-of-line applications. Remarkably, CVD techniques offer several key advantages, such as superior gap-filling capability and extremely uniform coating of large areas, which is crucial to future 300 mm wafers.[11] Moreover, the CVD methods are dry processes and generally require fewer processing steps and lower processing costs than do the spin-on methods.[2,4,11] These features make the CVD process easier for equipment manufacturers to integrate with other key processes.

Among various low-*k* CVD films, SiO_2-based dielectrics have attracted immense interest because of their physical rigidity, superior mechanical strength, and process extendibility, which together reduce the risks and costs of integration. Previous studies have demonstrated the benefits of incorporating fluorinated silicate glass (FSG, $k = 3.5$-3.7) into multilevel interconnect applications, as opposed to using the conventional undoped silicate glass (USG, $k = 3.9$-4.1).[9,12-13] However, when Cu interconnects are further scaled down to the 0.15/0.13 μm node, requirement is expected for dielectrics with even lower *k* values. C-doped low-*k* CVD organosilicate glasses (OSGs) become viable candidates due to their lower *k* values (<3.0) than that of FSG. Before successfully integrating low-*k* CVD OSGs into on-chip interconnect structures, fundamental properties such as chemical bonding, thermal stability, and electrical reliability must be explored. This work presents a comparative study of the thermal stability and electrical reliability of FSG and OSG films, with respect to integration with Cu metallization.

Experimental

Electrical measurements were made on Cu and TaN gated oxide-sandwiched low-*k* dielectric metal-insulator-semiconductor (MIS) capacitors. Figure 1 schematically illustrates the cross section of the Cu and TaN gated capacitors. The TaN gated capacitors are used as control samples since TaN neither mixes with the silicon oxide layer nor oxidizes under the thermal conditions used in this study.[14] Samples were prepared by first growing a 18 nm thick thermal oxide on p-type Si (100) wafers at $1000°C$ in a dry oxygen atmosphere. This oxide layer is required to form a robust dielectric-to-substrate interface for well-behaved capacitance-voltage (C-V) characteristics. Two species of low-*k* dielectric inorganic CVD oxides were investigated; they were F-doped oxides, fluorinated silicate glass (FSG, Si_xOF_y), and C-doped oxides, organosilicate glass (OSG, α-SiCO:H), both of which were chemically vapor deposited over the thermal oxide to a thickness of 500 nm. The FSG films were deposited by an inductively coupled high density plasma CVD (HDPCVD) system operating at 13.56 MHz with the following deposition conditions: substrate temperature $400°C$, total gas pressure 1-10 mTorr, and $SiF_4/SiH_4/O_2/Ar$ flow rate ratio of 6/1/11/26. The OSG films were grown by a parallel plate plasma-enhanced CVD (PECVD) system operating at 13.56 MHz with the following deposition conditions: substrate temperature $17°C$, total gas pressure 1-10 Torr, and $(CH_3)SiH_3/N_2O$ flow rate ratio of 2/5. A 50 nm thick PECVD undoped silicate glass (USG, $k = 4.2$) was then deposited on the low-*k* CVD dielectrics. The USG films were deposited in a parallel plate reactor operating at 13.56 MHz at the following conditions: substrate temperature $400°C$, total gas pressure 1-5 Torr, and $SiH_4/N_2/N_2O$ flow rate ratio of 3/16/95. This oxide cap may be required to act as a chemical mechanical polishing (CMP) hard mask in the Cu damascene architecture and a barrier to minimize the uptake of moisture in the low-*k* films. Another split of samples with a 75 nm thick PECVD nitride (SiN, $k = 7$-9) barrier replacing this oxide cap layer were also prepared to examine the SiN barrier effectiveness against Cu permeation. The SiN barrier was deposited in a parallel plate reactor operating at 13.56 MHz at the following conditions: substrate temperature $400°C$, total gas pressure 1-5 Torr, and SiH_4/NH_3 flow rate ratio of 1/8. The samples underwent a degas bake at $400°C$ for 30 min in an N_2 ambient to remove absorbed moisture in the dielectric stack before the metal electrode deposition. A Cu film of 200 nm thickness was then sputter deposited using a dc magnetron sputtering system with a base pressure of 1-2×10^{-6} Torr and no intentional substrate heating. The Cu surface was further covered with a 50 nm thick TaN overlayer, which
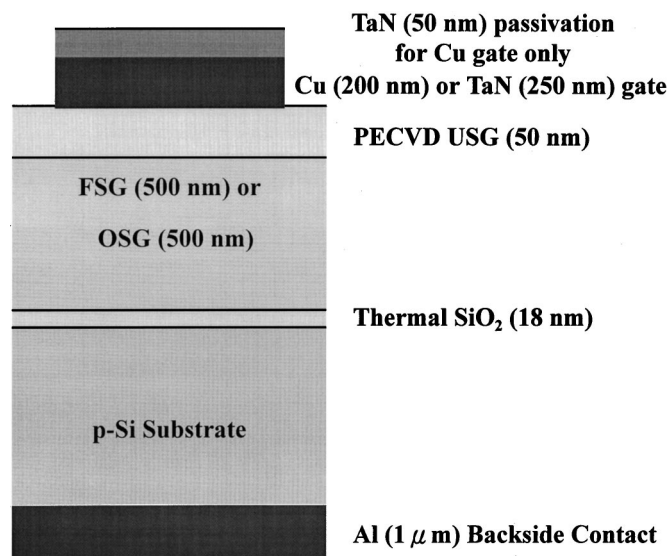
Figure 1. Schematic cross section of Cu and TaN gated oxide-sandwiched FSG and OSG MIS capacitors studied in this work.

Figure 2. Temperature dependence of (a) and (b) film thickness and (c) and (d) refractive index for FSG and OSG films.

was reactively sputtered in the same sputtering system without breaking the vacuum, using a Ta target in a gas mixture of Ar and N_2 with Ar/N_2 flow rates of 24/6 standard cubic centimeters per minute. The TaN overlayer prevents oxidation of the Cu layer in the subsequent high temperature process. For the TaN gated control samples, a 250 nm thick TaN layer was reactively sputter deposited directly on the USG layer. A lift-off process, instead of a chemical wet etching of the vulnerable low-*k* dielectric stack, was used to define gate electrodes in a circular area of 0.8 mm diam. A 1 μm thick Al layer was thermally evaporated on the back side of the Si substrates for all samples, for a better contact in electrical measurements.

The completed Cu and TaN gated MIS capacitors were thermally annealed at 400°C for 1 h in an N_2 ambient. This annealing step eradicates the plasma damage during gate electrode sputtering, and provides the driving force for Cu diffusion. The capacitors were then bias-temperature stressed (BTS) at 250 and 150°C, respectively, for the FSG and OSG MIS capacitors with an effective applied field of 0.8 MV/cm for 30 min, which is long enough for the mobile charges to drift across the stacked insulator layer. The bias during BTS was provided by an HP4145B semiconductor parameter analyzer, and the room temperature C-V characteristic was measured using a Keithley package 82 system. Notably, the MIS capacitors were first baked at 200°C on the thermal chuck for 1 h in the N_2 ambient to dehydrate the CVD dielectric stack prior to any BTS and/or electrical measurement and that all BTS measurements were conducted with a continuous N_2 purge to prevent the uptake of moisture in the CVD dielectrics throughout testing. High frequency C-V characteristics of the MIS capacitors, sweeping from inversion to accumulation, were measured at a frequency of 1 MHz.

Several techniques were employed for intrinsic physical property analysis. The *k* value of the films was evaluated from the maximum capacitance values obtained from the C-V measurement at 1 MHz using the Al gated MIS structure with the area correction of the Al gate electrodes made by optical microscopy (OM). Both the film thickness and the refractive index of the CVD dielectrics were measured using a well-calibrated N&K analyzer at 6328 Å wavelength. Fourier transform infrared spectroscopy (FTIR) and thermal desorption mass spectroscopy (TDS) were used to monitor the chemical bonding evolution and outgassing behavior of the CVD dielectrics during the thermal annealing process. Secondary ion mass spectroscopy (SIMS) was employed to probe the possible presence of Cu in the dielectric layers of the MIS capacitor.
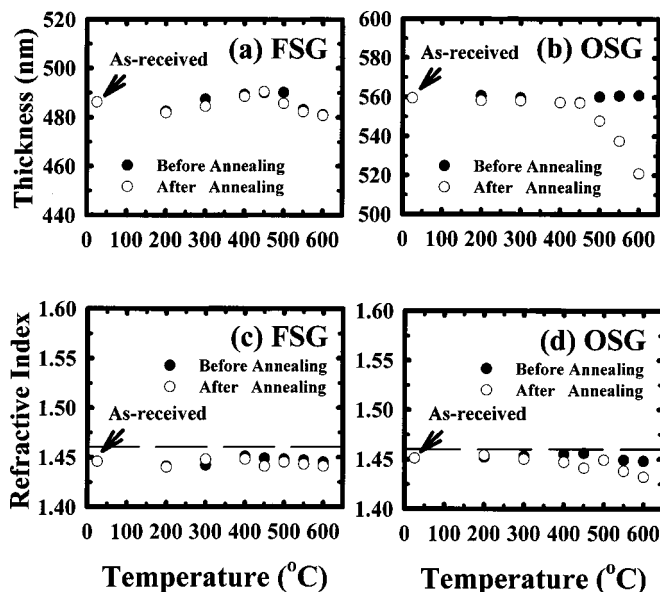
Results and Discussion

Physical properties and thermal stability of FSG and OSG dielectric films.—Figure 2 shows the variations of thickness and refractive index for FSG and OSG thermally annealed at various temperatures. Clearly, the film thickness and the refractive index of FSG remained nearly constant even at temperatures of up to 600°C, although the film thickness for OSG clearly shrank upon annealing at temperatures above 500°C, and the refractive index also exhibited a decreasing tendency, indicating changes in film composition and bonding structure in OSG. The reference value of 1.46 for the refractive index of the thermal oxides is indicated by a dashed line. Refractive indices below 1.46 were reported herein to be indicative of porous or less dense materials like FSG and OSG.[15] In fact, introducing fluorine leads to a less dense Si-O network in FSG, while a high density of nanometer-sized pores, with radii of only about 4-12 Å and total volume fraction of pores around 36%, are incorporated into the methyl-doped OSG films.[16-18] Such nanoporosity is closely related to the incorporation of CH_3 moieties into the films. Figure 3 illustrates the FTIR spectra for FSG and OSG thermally annealed at various temperatures. Several salient features exist in the evolution of the absorption peaks. First, the silanol peak (Si-OH) at about 3700 cm^{-1} was not present in the FTIR spectra for either FSG or OSG, implying that the FSG and OSG used herein were not prone to moisture uptake in the normal ambient. However, immersing the OSG film in boiling water for 30 min caused the Si-OH peak to appear in the FTIR spectra, whereas it remained stable for the FSG film even after immersion in boiling water for 2 h. Since OSG is more porous and less dense than FSG, moisture uptake in OSG should be easier due to its effective larger surface area, despite the presumption that adding CH_3 groups to the Si-O matrix could cause OSG to become hydrophobic.[1-3,6,19-21] Such a susceptibility to moisture may adversely impact the electrical reliability of OSG in its integration with Cu metallization. Second, OSG is a hybrid material whose infrared spectrum comprises both organic and inorganic absorption peaks. The organic Si-CH_3 bonds reduce the density and polarizability of OSG films, while the inorganic Si-O stretch peak contains a shoulder at higher wavenumbers, indicating that the open chain and caged Si-O structural configuration coexist in this bond. Third, the peak height ratio of Si-F (927 cm^{-1}) to Si-O (1095 cm^{-1}) in FSG remained constant at about 8-9% at temperatures of up to 600°C, while the Si-CH_3 (1273 cm^{-1}) to Si-O
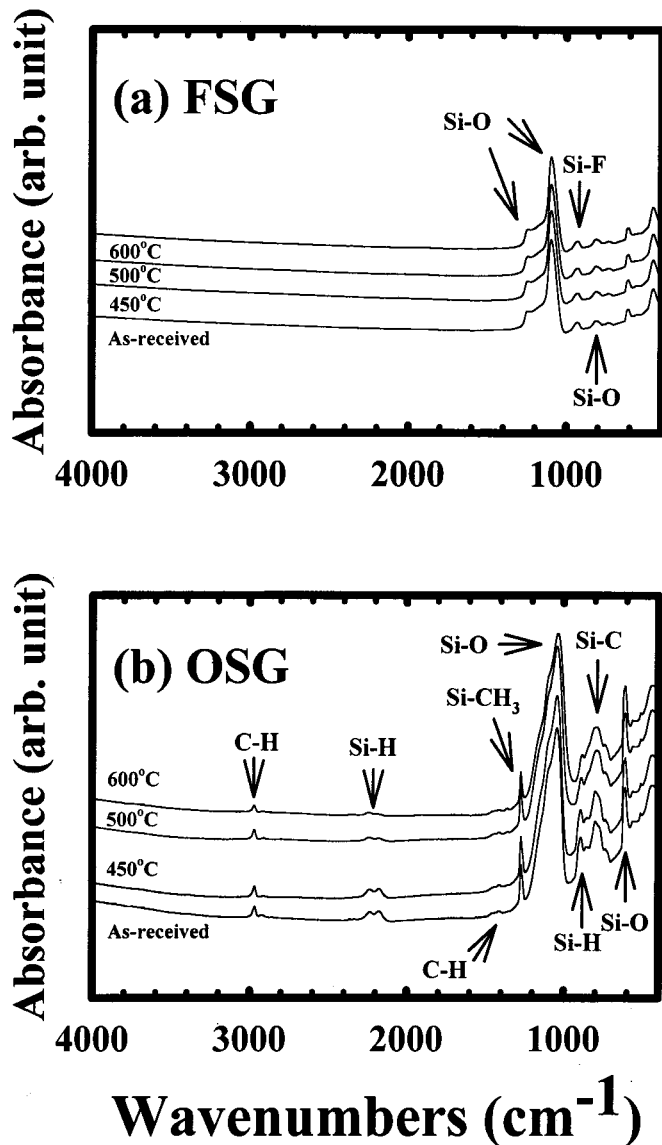
Figure 3. FTIR absorption spectra of (a) FSG and (b) OSG films annealed at various temperatures for 30 min in an N_2 ambient.
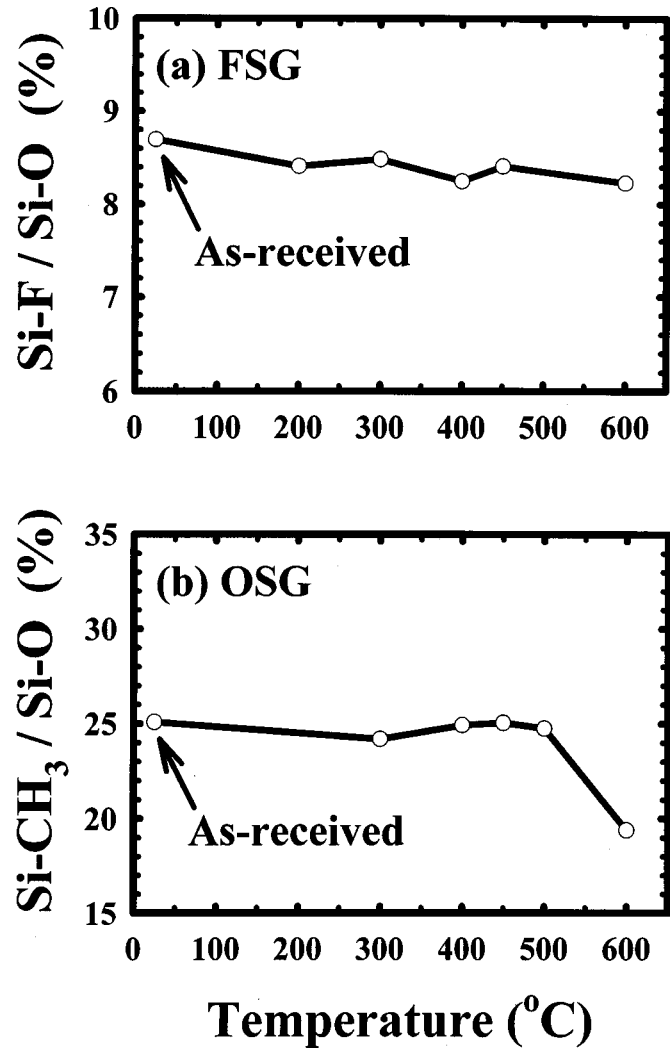

Figure 4. Temperature dependence of peak height ratios of (a) Si-F/Si-O for FSG and (b) Si-CH$_3$/Si-O for OSG films as determined from FTIR spectra.
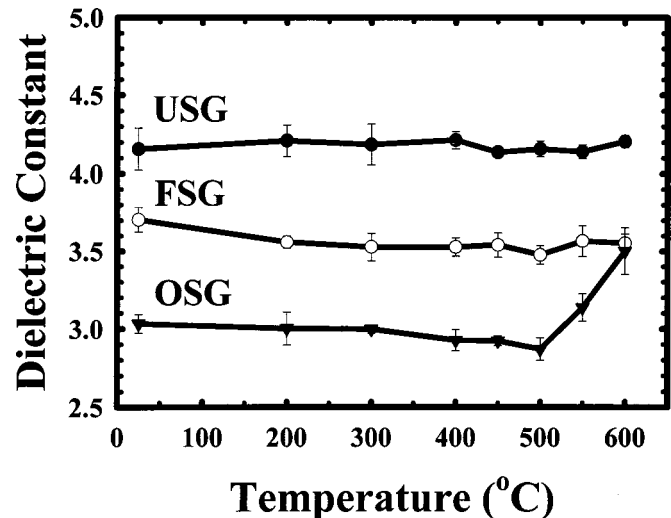
(1042 cm^{-1}) peak ratio in OSG remained nearly 25% at temperatures of up to 500°C, but dropped sharply at temperatures above 500°C, as shown in Fig. 4. Thus, deterioration of the low-k property of OSG, especially the k value, can be expected at temperatures above 500°C. Figure 5 shows the dielectric constants of FSG and OSG thermally annealed at various temperatures, with the data of USG included for comparison. The dielectric constants remained stable for USG (4.1-4.2) and FSG (3.5-3.7) at temperatures of up to 600°C, but for OSG, the dielectric constant increased markedly when temperatures exceeded 500°C. Apparently, the k value in OSG degraded mainly because of the partial removal of the methyl groups (CH$_3$), making the film prone to moisture uptake, and to appearing hydrophilic at localized areas on its surface. This result is further confirmed from the measured TDS spectra (not shown), wherein the desorption of CH$_3$ increased significantly at temperatures above 500°C. In summary, the thermal stability of FSG was found to exceed 600°C, while that of OSG was about 500°C, both higher than that of organic aromatic PAE-2.[22]

　　　Electrical characteristics of oxide-sandwiched FSG and OSG capacitors.—Figure 6 shows C-V curves of the Cu as well as TaN

Figure 5. Dielectric constant *vs.* annealing temperature for USG, FSG, and OSG films.
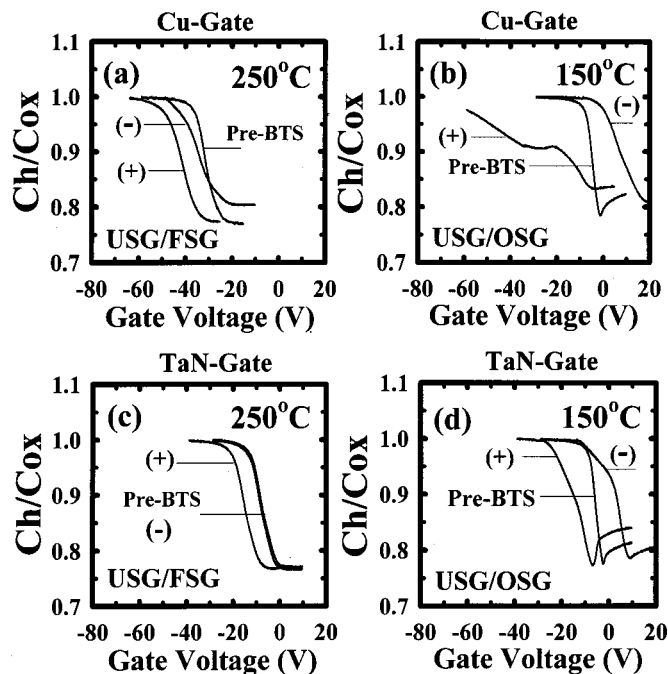
Figure 6. C-V characteristics of Cu and TaN gated oxide-sandwiched FSG and OSG MIS capacitors before and after BTS at 250 and 150°C, respectively, with an effective applied field of 0.8 MV/cm for 30 min. The positive (+) bias was applied first, followed by the negative (−) bias at the same conditions.

gated oxide-sandwiched FSG and OSG MIS capacitors before and after BTS at 250 and 150°C, respectively. The BTS was first applied with a positive bias (on the gate electrode) corresponding to an effective field of 0.8 MV/cm for 30 min, and followed by application with a negative bias under the same conditions. Notably, the BTS at 150°C produced negligible change of C-V curve for the Cu and TaN gated FSG capacitors, and thus, BTS was applied on FSG capacitors at 250°C. For both of the FSG and OSG capacitors, the negative flatband voltage shift (ΔV_{FB}) of the Cu gated capacitor resulting from the positive BTS was evidently larger than that of the TaN gated capacitor, implying the presence of positively charged mobile Cu ions in both Cu gated FSG and OSG films with BTS at 250 and 150°C, respectively. Moreover, Cu ions clearly drift more readily in OSG than in FSG, presumably owing to the porous structure of OSG, which contains high density nanometer-sized pores. The smaller negative ΔV_{FB} associated with the TaN gated FSG and OSG capacitors was caused by the contaminated ionic charges, such as the alkali or hydrogen-related impurity in the upper USG cap
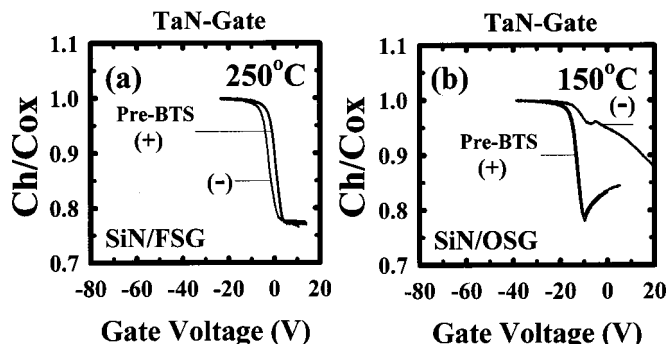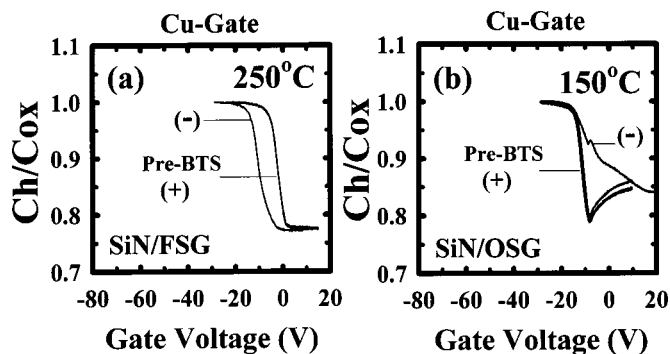

Figure 8. C-V characteristics of Cu gated and SiN capped (a) FSG and (b) OSG MIS capacitors before and after BTS. The conditions of BTS are the same as those of Fig. 6.

layer.[23] This relationship can be verified by the fact that replacing the USG cap layer with a SiN cap layer resulted in negligible ΔV_{FB}'s, as shown in Fig. 7. On the other hand, the large positive ΔV_{FB} and marked distortion in C-V resulting from the negative BTS on the Cu and TaN gated OSG capacitors may be associated with natural dielectric wear out, and is not related to Cu ion drift. In contrast to the more oxide-like FSG, such a dielectric wearout of OSG is presumably related to its intrinsic porous film structure. The anomalous small negative ΔV_{FB} resulting from the negative BTS on the TaN-gated and SiN capped FSG capacitors (Fig. 7a) cannot be attributed to Cu ions. Rather, this negative bias-temperature instability is presumably related to the film nature of FSG deposited by HDPCVD, since such an instability was not observed in FSG grown by PECVD.[24] Figure 8 shows the C-V characteristics of the Cu gated FSG and OSG capacitors with a 75 nm thick SiN cap layer before and after BTS at 250 and 150°C, respectively. The figure reveals that the C-V characteristics remained intact at the same position, indicating the barrier effectiveness of the SiN layer against Cu diffusion. Meanwhile, Fig. 9 shows the SIMS depth profiles of the positive BTS stressed Cu gated FSG capacitor with a 75 nm thick SiN cap layer, as well as the corresponding Cu gated USG capped FSG capacitor. The SiN cap layer achieves significant improvements in the FSG and OSG films, both in the absence of negative ΔV_{FB} with respect to the positive BTS, and in the absence of Cu permeation. Therefore, the large negative ΔV_{FB} in the Cu gated oxide-sandwiched FSG and OSG MIS capacitors was induced by the presence of Cu ions following the positive BTS, and the 75 nm thick SiN cap layer served as an effective dielectric barrier against Cu penetration.
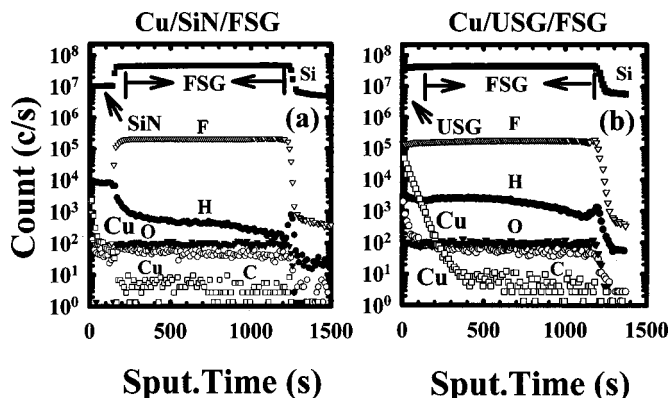

Figure 7. C-V characteristics of TaN gated and SiN capped (a) FSG and (b) OSG MIS capacitors before and after BTS. The conditions of BTS are the same as those of Fig. 6.

Figure 9. SIMS depth profiles of Cu gated (a) SiN and (b) USG capped FSG MIS capacitors after a positive BTS at 250°C. The Cu gate was removed prior to the SIMS measurements.

Combining the C-V and SIMS results, this study showed that Cu did penetrate into FSG and OSG, and that Cu appeared to drift faster in OSG than in FSG. The distinct difference between the observed Cu drift behavior in FSG and OSG results from the inherent porous structure of OSG, in which the CVD deposition of OSG films incorporates high density nanometer-sized pores. These nanopores act as fast diffusion paths via which Cu can drift rapidly in porous OSG. Meanwhile, the relatively dense structure of FSG hindered the Cu drift because of the miniature free volume in the FSG Si-O network.[25,26] Moreover, it was also reported that water vapor in the ambient markedly compounded the penetration of Cu in the oxide network, either by causing deep level electron traps,[26,27] or by hydration energy.[28] Therefore, even with continuous N_2 purging during BTS measurements, Cu drift in OSG may also be enhanced by the uptake of a trace of H_2O, due to the susceptibility to moisture that differentiates OSG from FSG.

Conclusion

Two species of inorganic low-*k* F- and C-doped CVD oxide-based dielectrics (FSG and OSG) were evaluated for their thermal stability and electrical reliability with respect to integration with Cu metallization. The thermal stability temperature of FSG was found to exceed 600°C, while that of OSG was about 500°C. Although Cu penetration was observed in both dielectrics, Cu appeared to drift more readily in OSG than in FSG, presumably because OSG has a porous and less dense structure. Moreover, the nitride film (75 nm) was confirmed to be an effective dielectric barrier against Cu permeation.

Acknowledgments

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