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One-Step Cleaning Solution to Replace the Conventional RCA Two-Step Cleaning Recipe for Pregate Oxide Cleaning

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This work proposes an advanced wet chemical one-step cleaning process which omits the hydrochloric acid/hydrogen peroxide/water mixture (HPM) step in RCA. A novel one-step cleaning solution had been developed for pregate oxide cleaning to replace the conventional RCA two-step cleaning recipe, which used ammonia/hydrogen peroxide (or SC-1) and HPM (or SC-2) step. Tetramethylammonium hydroxide (TMAH) and ethylenediaminetetraacetic acid (EDTA) were added into the RCA SC-1 cleaning solution to enhance cleaning efficiency. From the experimental results, the particles and metallic contamination on the bare Si wafer surface could be removed significantly by applying this one-step cleaning solution. The effectiveness of various cleaning recipes and their interaction mechanism with silicon surfaces were studied. The surface adsorption and double layer models could explain the surface behavior of TMAH solutions. Based on the model, the particle, surface roughness and metallic contaminants can be realized. It was observed that the electrical properties of metal oxide semiconductor capacitors after cleaning with this novel solution were better than those after the conventional RCA cleaning. Besides, the cleaning method combining NH_4OH, tetramethylammonium hydroxide, ethylenediaminetetraacetic acid, and H_2O_2, at 80°C for 3 min showed high performance on particle removal, metal cleaning, surface smoothness, and electrical properties. Hence, this one-step cleaning process is very promising for future large sized silicon wafer cleaning due to the advantages of time-saving, low cost, and high performance.
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An efficient wet cleaning process in semiconductor manufacturing is essential to the removal of residual contaminants on silicon wafer surfaces as the device size scales down to the deep-submicrometer scale era.[1] The thickness of the gate oxide decreases from 70 to 25 Å as the device dimension decreases from 0.35 to 0.1 μm.[2] Gate oxide integrity (GOI) is closely related to the lifetime of the device.[3] It has been reported that GOI depends strongly on wafer cleanliness before oxidation.[4] Different contaminants have different effects on device reliability.[5] Particles on the silicon surface result in a low breakdown field and low yield, while the organic contamination decreases the rate of oxidation and the quality of the oxide.[6] Furthermore, metal contamination will cause a low breakdown field and a high junction leakage current, an increased oxide trap, which results in a reduced minority carrier lifetime, a shifted threshold voltage, and a resulting hot carrier degradation. The RCA cleaning process was developed in 1970 by Kern and Puotinen,[7] which is still employed around the world as a wet cleaning technology to remove contaminants on the wafer surface. The conventional RCA two-step cleaning recipe including SC-1 of NH_4OH:H_2O_2:H_2O, 1:1:5, 70°C, 10 min, and SC-2 of HCl:H_2O_2:H_2O, 1:1:6, 70°C, 10 min, has been used for over 30 years. Solution of a high pH value (*i.e.*, SC-1) is used to remove organic contamination and particles. Solution of a low pH value (*i.e.*, SC-2) is used to remove most metallic contamination by acid competition.

Recently, many modifications of the conventional RCA two-step cleaning have been proposed to meet stringent requirement in the preparation of ultrathin oxide.[4,8] The concept of reducing the cleaning step process cost and cycle time has been proposed in these studies. This concept demonstrates the following benefits: (*i*) to meet the international guidance and requirements developed in environmental management, (*ii*) to reduce the use of chemicals and waste handling, (*iii*) to save processing time, increase throughput, and reduce cost, and (*iv*) to improve the goals of Safety, Health, and Environment (SHE).[9] For example, Ohmi[4] proposed a new and advanced wet chemical cleaning process which omitted SC-2 step in RCA cleaning when highly purified HF solution was used. Heyns *et al.* (IMEC)[8] proposed a cleaning process without NH_4OH or HCl. Akiya *et al.*[6] added chelating agents into the SC-1 solution to reduce metallic contamination. On the other hand, Morinaga *et al.*[10] found that ammonia/hydrogen peroxide mixture (APM) cleaning, together with megasonic irradiation and a chelating agent, showed better removal of particles and metallic impurities. However, they have not investigated the influence of surface roughness, residual particles, and metals on the electrical characteristics of ultrathin oxide film for using these cleaning solutions.

In this paper, a one-step cleaning solution containing NH_4OH and H_2O_2, and/or tetramethylammonium hydroxide (TMAH) and ethylenediaminetetraacetic acid (EDTA) were explored for their influence on the roughness and etching rate of silicon surface. The interaction mechanism of the TMAH solution and the silicon surface was discussed. Furthermore, the particle, organic, and metallic impurities were analyzed for evaluating the cleaning efficiency. The electrical characteristic of gate oxide after cleaning with this novel cleaning solution was also evaluated.

Experimental

Cleaning solutions and capacitor fabrication process.—All reagents used with high purity were of electronic or higher grade from Merck (Darmstadt, Germany). Table I lists the various recipes of different alkali cleaning solutions which are tested to find the best

Table I. Cleaning recipes used in pregate oxide cleaning study.

Solution	NH_4OH (%)	TMAH (2.38%, Mw = 91): NH_4OH	EDTA (Mw = 292)	pH
A	29	0	0	12.38
B	29	1:100	0	12.65
C	29	0	100 ppm	12.40
D	29	1:100	100 ppm	12.75

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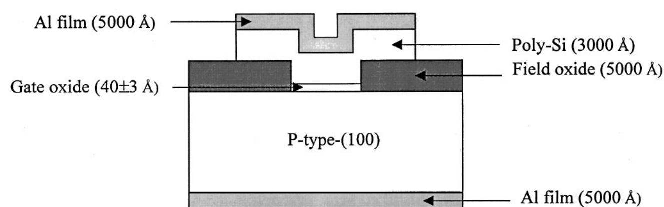

- RCA clean
- A field oxide with a 5000 Å thickness
- Defined active region and etched oxide
- *Cleaned wafers by using RCA and one-step cleaning step*
- The gate oxide with 40±3 Å thickness thermally grown at 900℃
- Poly-Si film with a 3000 Å thickness and doped with $POCl_3$ at 950℃ for 30 min
- Deposited a 5000 Å Al film on the wafer
- Defined MOS capacitor and etched Al and poly-Si film
- Deposited a 5000 Å Al film on the backside of wafer
- Sintered at 400℃ for 30 min

Figure 1. The capacitor structure and manufacturing steps of the MOS capacitors.

cleaning efficiency for silicon surface. The TMAH and EDTA are used in the cleaning solutions. The EDTA has four p*K*a values of 1.99, 2.67, 6.16, and 10.26.[11]

Figure 1 describes the fabrication process for capacitor and the cleaning procedure. Metal-oxide-semiconductor (MOS) capacitors were fabricated on a 4 in. diam, (100)-oriented p-type wafers with a resistivity of 14-21 Ω cm. All wafers were first cleaned by a standard RCA two-step cleaning method. A 5000 Å field oxide was thermally grown at 1050°C for 1 h in a pyrogenic gas as an isolation layer. The active region was defined with lithography and etching. All wafers were cleaned by sulfuric acid/hydrogen peroxide mixture (SPM) (H_2SO_4/H_2O_2) and diluted HF, then followed by various cleaning solutions and various methods (Table II). Immediately, a gate oxide with 40 ± 3 Å thickness was thermally grown at 900°C. The oxide thickness was determined from spectroscopic ellipsometry. After oxidation, a 3000 Å poly-Si film was deposited at 620°C in a low-pressure chemical vapor deposition (LPCVD) system. The poly-Si film was then doped with $POCl_3$ at 900°C for 30 min, which resulted in a resistivity of 30-40 Ω/□. A 5000 Å Al film was deposited on the wafer using a thermal coater. The gate of MOS capacitor was defined by lithography, and then Al and poly-Si films were etched by wet etching solutions. The back of the wafer was also

Table II. Different cleaning methods for this study.

Method	
RCA	Standard RCA (SC-1 and SC-2) cleaning
TM	Solution B:H_2O_2:H_2O (1/4:1:5) at 70°C for 10 min
ED	Solution C:H_2O_2:H_2O (1/4:1:5) at 70°C for 10 min
TE	Solution D:H_2O_2:H_2O (1/4:1:5) at 70°C for 10 min
TE1	Solution D:H_2O_2:H_2O (1/4:1:5) at 70°C for 5 min
TE2	Solution D:H_2O_2:H_2O (1/4:1:5) at 80°C for 3 min

deposited with 5000 Å Al film using evaporation method. Finally, all the samples were sintered at 400°C for 30 min in an N_2 ambient to form a good ohmic contact.

Instrumental analysis and electrical characterization.—Wafers were then exposed to environment air (outside) to create particle-contaminated wafers (particle counting indicated 4000-5000 pieces on wafer surface). These contaminated wafers were subsequently cleaned with different cleaning solutions, finishing with a deionized water immersion for 10 min, and determined the efficiency of particle removal. The particle number for various cleaning recipes was counted by the Tencor Surfscan model 4500 system. A particle count for sizes greater than 0.2 μm was detected. The surface roughness of the silicon wafer was measured by atomic force microscopy (AFM). The residual organic on the poly-Si surface was determined with the Hitachi thermal desorption system (TDS) (model UG-21) and atmospheric pressure ionization mass spectrometer (APIMS) (model UG-400P). The desorption temperature of the TDS-APIMS ramped from room temperature to 600°C at 10°C/min. The surface outgassing was analyzed at m/z 16, 30, 44, and 58. In order to measure the cleaning efficiency for metal, wafers were first dipped in solutions containing Fe, Na, Ca, Cu, Mn, and Al (pH 6-7, room temperature). The surface metal after cleaning was determined using Rigaku model 3700 total reflection X-ray fluorescence spectrometer (TXRF). The incident X-ray angle was 0.07°. The detection limit of TXRF is near 5×10^9 atoms/cm^2. The gate area of the MOS capacitor was 10^{-4} cm^2. The electrical properties of the MOS capacitors, the current density *vs.* electric field, and time dependent dielectric breakdown (TDDB) characteristics, were measured by using the Hewlett-Packard (HP) 4145B semiconductor parameter analyzer. The flatband voltage was obtained by using a Keithley capacitance-voltage (C-V) system.

Results and Discussion

The physical and chemical properties of pregate oxide cleaning.—The surface adsorption and double layer model can explain the behavior of TMAH according to our previous report.[12] The tetramethylammonium cations are first adsorbed in the primary layer due to van der Waals attraction on the silicon surface. As Fig. 2

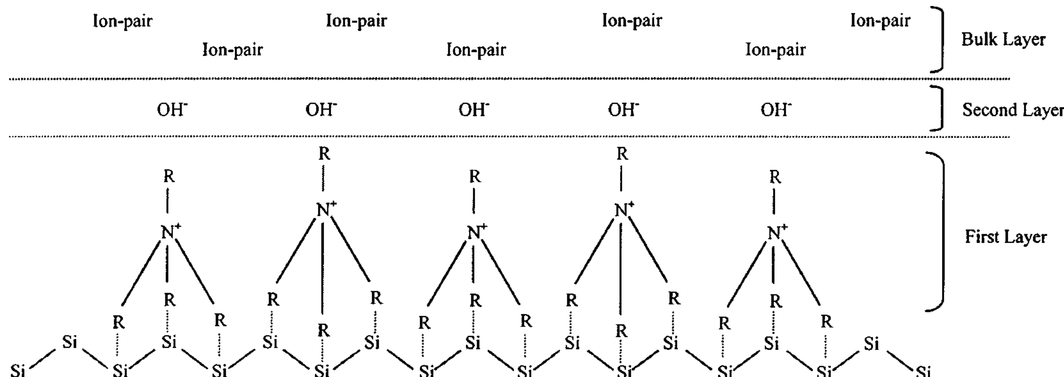

Figure 2. The surface adsorption and double layer models.

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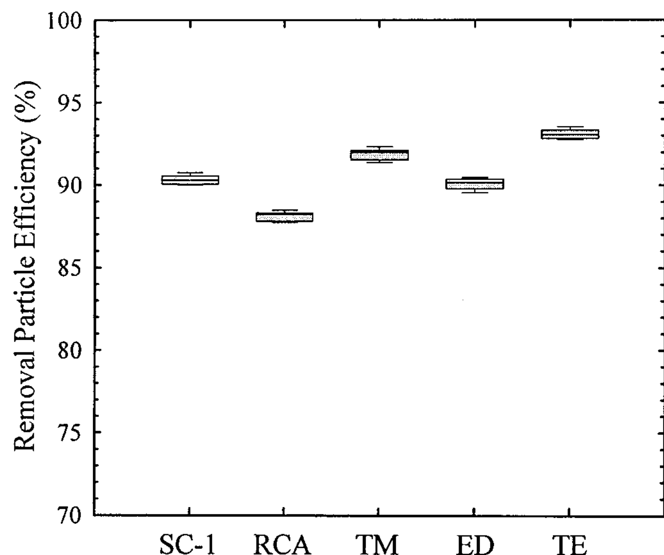

Figure 3. The particles removal efficiency on the surface for different cleaning methods.

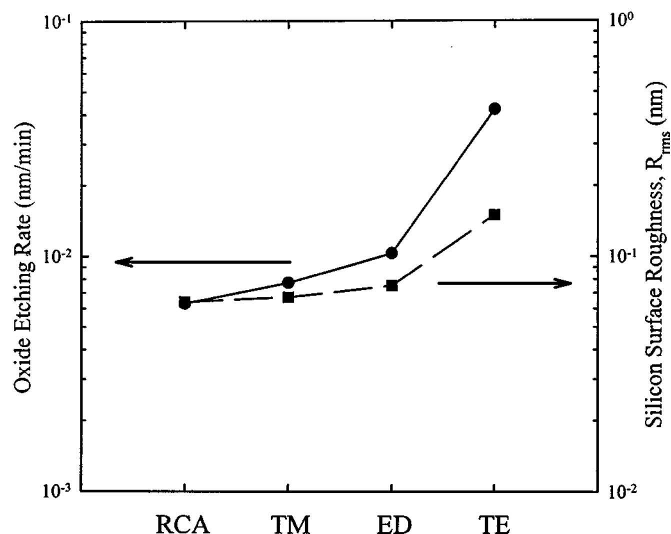

Figure 5. The etching rate of oxide and the roughness of silicon surface after different cleaning methods.

illustrates, this layer is positively charged. The second layer is negatively charged with anion (*e.g.*, hydroxide). The formation of ion pairs (*i.e.*, TMAH) can be seen in the bulk layer. In the next section, the model can be used to explain the origin of surface roughness for each cleaning solution. It is inevitable to use the interaction model in Fig. 2 for examining the surface particle. Figure 3 shows the particle removal efficiency on the surface of wafers cleaned with different methods. The one-step method improves the removal efficiency significantly. The tetraethylene (TE) method depicts the highest removal efficiency among these four solutions. However, the particle removal efficiency of the RCA method (SC-1 and SC-2) is not satisfactory because a lot of particles may adsorb on the wafer surface during SC-2 treatment. Figure 4 illustrates the surface behavior of two types of particles, *i.e.*, hydrophilic and hydrophobic. The type-I hydrophilic particle has a weaker interaction with silicon surface, while the type-II hydrophobic particle shows stronger interaction. Based on Tardif's report,[13] the zeta potentials of particles and the silicon surface are both negative at pH higher than 12. For the type-I particle, the effect of the solution composition is not significant due to weak attraction of the particle to the silicon surface. However, for the type-II particle, the composition of cleaning solution is very important in separation of the particle with higher surface attraction force. In the one-step method with cleaning solutions B and D, the tetramethylammonium can penetrate into the interfacial region of particles and silicon. Then, the particle surface and silicon surface can be gradually adsorbed by tetramethylammonium ions. The surface adsorption of tetramethylammonium ions facilitates the particle removal from the silicon surface due to the reduction of interfacial attraction. On the contrary, the RCA and ethylene diamine (ED) (containing only EDTA) methods with solutions A and C cannot easily penetrate the interfacial region of silicon and hydrophobic particle due to the hydrophilic character of NH_4OH. Despite the fact that solutions containing tetramethylammonium have good behaviors on particle removal, the contamination effect of surface adsorption organic in cleaning solution needs further evaluation.

Tardif *et al.*[14] have reported that the electrical properties of capacitors increase with the HF dipping time. However as the dipping time is too long, the electrical properties gradually decrease. This uprising tendency of charge-to-breakdown is due to surface hydrophilicity, while the degrading tendency is due to surface roughness. The surface roughness of silicon wafers and the oxide etching rate of oxide were measured and shown in Fig. 5. The RCA method has the smoothest surface, while the TE method shows the roughest silicon surface among these four cleaning recipes. In addition to the roughness, it is obvious that the TE method also exhibits the fastest oxide etching rate than the other solutions. This figure also indicates that the cleaning solution containing TMAH and EDTA has an appreciably high surface roughness. This tendency can be attributed to two reasons. First, the solution is more basic due to spiking TMAH (see Table I). The more basic condition leads to a higher oxide etching rate and surface roughness. Second, the EDTA anion can appear in the second layer of Fig. 2. The surface TMA^+ in the first layer can be removed by the formation of $(TMA)_4EDTA$. The vacancy can be easily attacked by the hydroxide from the second layer.

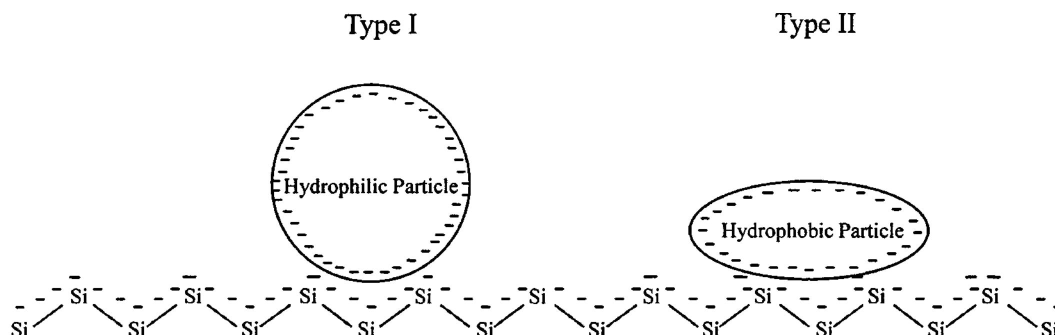

Figure 4. The adsorption of hydrophobic and hydrophilic particles on the silicon surface.

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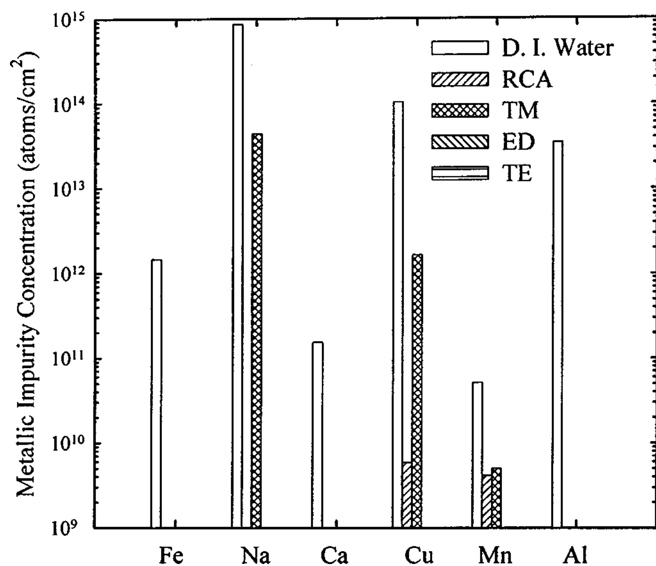

Figure 6. The metallic impurities contamination on the surface for different cleaning methods.

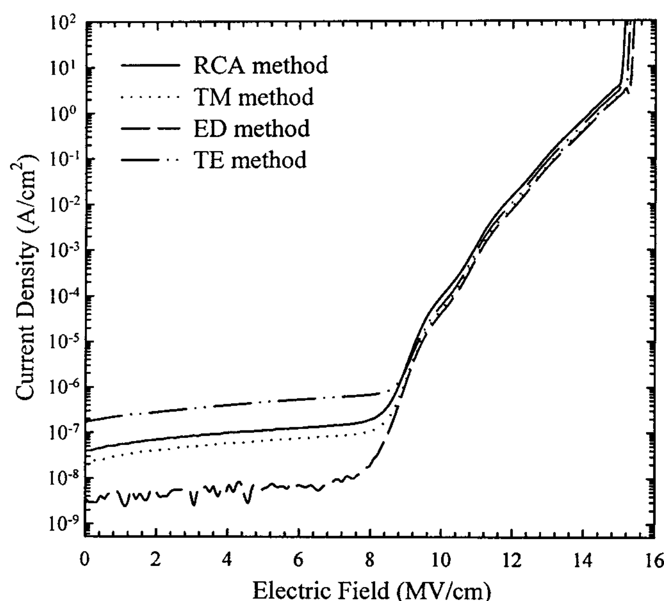

Figure 7. The current density *vs.* voltage characteristic of MOS capacitors with oxide thickness of 4.5 nm after cleaning with different cleaning methods.

The intensity of surface organic is determined by TDS-APIMS measurement. The weak peak intensity of CH_4, C_2H_6, C_3H_8, and C_4H_{10} for the one-step method with cleaning solutions B and D are in the same range with solution A. The latter electrical result demonstrates the level of residual organic has no deteriorating effect. Another important indicator to check the cleaning efficiency is the metallic contamination. The 1999 International Technology Roadmap for Semiconductors (ITRS) indicates that the control limit of surface metal is about 10^4-fold more critical than that of the organic component. Figure 6 shows the metallic impurity concentration measured by TXRF. It is clear that the metallic contaminants are removed significantly by using the one-step method. Solution B (containing only TMAH) does not easily remove metallic impurities on the wafer surface. This result follows with our previous publication[12] that few amounts of spiking EDTA (100 ppm) in cleaning solutions can enhance metal removal. In the alkaline condition ($pH > 12$), the hydrogen ion on the EDTA can be fully removed owing to their p*K*a values. Then, the solution EDTA has hexadentate coordination capability with the metals ions. Hence, the surface metal is efficiently removed with the EDTA from the solution. In using the one-step method with containing tetramethylammonium solutions, the most concerning problem is the interaction of metallic ion and the silicon surface. Interestingly, it is found that the metal cation and the surface adsorption tetramethylammonium cation are of the same charge type. The consideration of electrostatic interaction between metal ions and the wafer surface can be neglected. For the metal oxide (*e.g.*, chromium oxide, iron oxide), the effect of tetramethylammonium-containing solutions needs further consideration. Similar with the type-II particle in Fig. 4, metal oxide may be taken away from the surface by the adsorption of tetramethylammonium ions.

Electrical properties for various cleaning methods.—In Fig. 7, the current density *vs.* electric field characteristic (J-E characteristic) of the MOS capacitor cleaned by four solutions are shown. The MOS capacitor using the ED method demonstrates the lowest leakage current density among these four samples. On the other hand, the MOS capacitor using the TE method depicts the largest leakage current density and the lowest breakdown field. The variation in leakage current density and breakdown field strength is attributed to the rough silicon surface resulting from the TE cleaning solution. Figure 8 shows the cumulative distribution (in percentage) of leakage current density measured at -3.3 V. It is clear that the ED method has the lowest distribution among these four solutions, and TE method exhibits the highest leakage current density distribution. The breakdown field is shown in Fig. 9. It is obvious that the TE method exhibits the lowest breakdown electric field in the distribution.

A constant current stressing is used to determine the GOI reliability. In this measurement, an electron current is injected by tunneling through the oxide. The gate voltage of the MOS capacitor is measured when the Si substrate is positively biased in accumulation mode. Hence, for p-type Si substrate, electrons are injected from the interface of poly-Si/SiO_2 to the SiO_2/Si interface. For ultrathin gate oxide, it has been found that the charge-to-breakdown (Q_{bd}) value is lower for electrons injection from gate than that from substrate

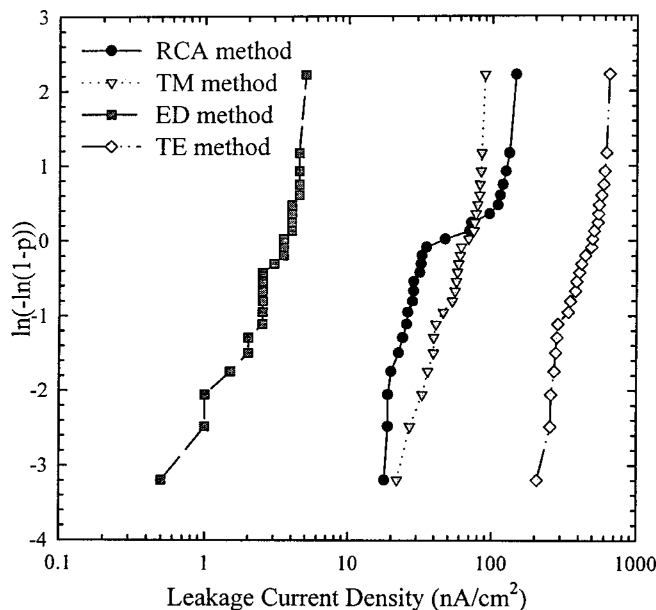

Figure 8. The cumulative distribution of leakage current density of MOS capacitors after cleaning with different cleaning methods.

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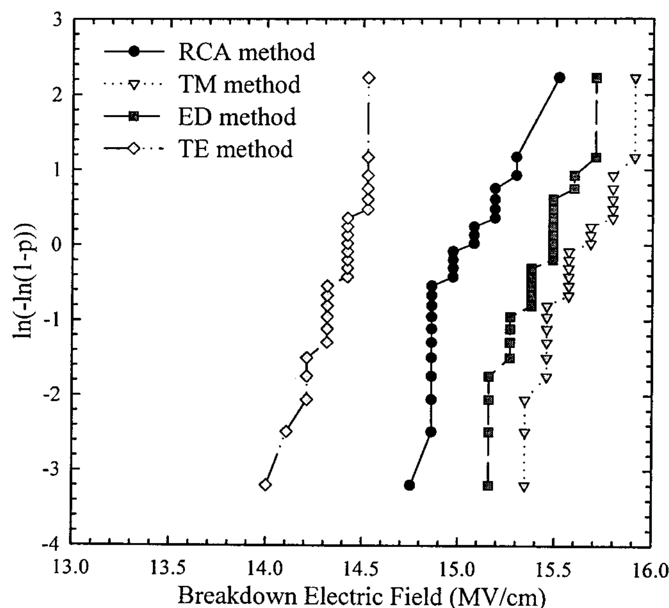


Figure 9. Statistical distribution of the electric breakdown field of MOS capacitors with oxide thickness of 4.5 nm after cleaning with different cleaning methods.

injection.[15,16] It is known that the mechanisms of breakdown can be summarized due to the hole trapping model,[3] the electron trapping model,[17] the interface softening model,[18] the physical damage model,[19] and the modified hole trapping model.[20] The breakdown model of our sample is consistent to the hole-trapping model that a negative gate voltage shift is found under constant current stressing. The resultant Q_{bd} under a constant -0.1 A/cm^2 current stressing is shown in Fig. 10. The ED method shows a larger value of Q_{bd} than that of the others. To optimize the TE recipe, the cleaning time and the temperature should be adjusted to reduce the surface roughness. However, it should be noted that the efficiency may be reduced for insufficient time and temperature. An experiment was designed with

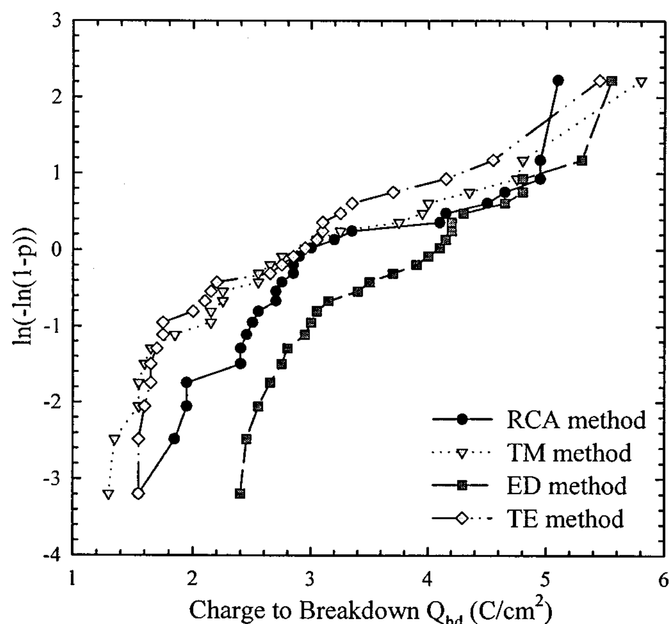
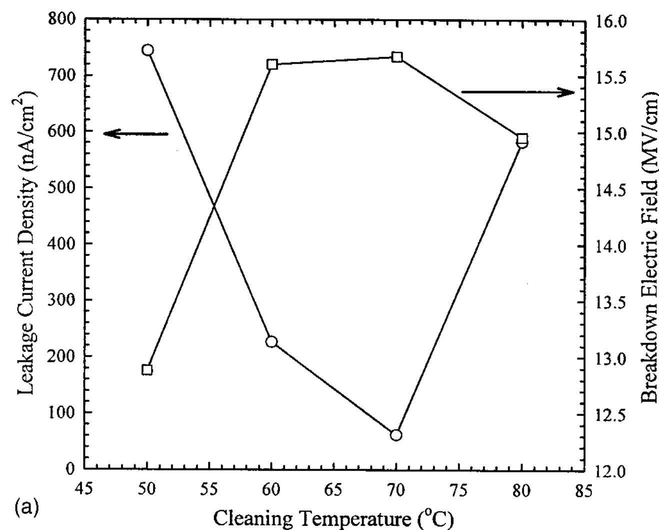


Figure 10. The charge-to-breakdown of MOS capacitors after cleaning with different cleaning methods. The thickness of oxide is 4.5 nm.



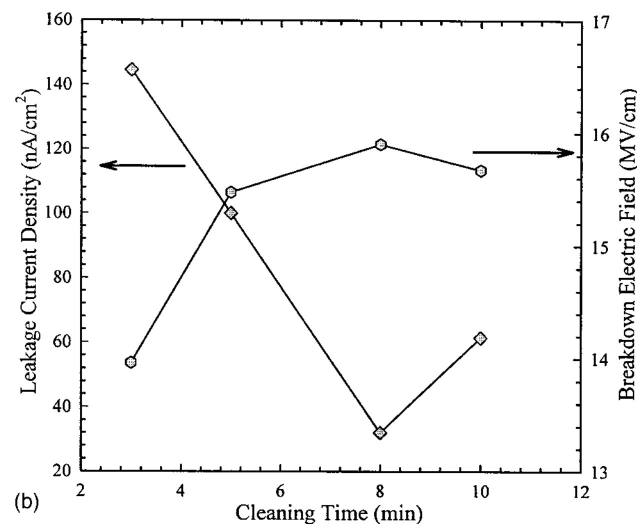


Figure 11. Leakage current density and electric breakdown field after (a) cleaning for 10 min by using different cleaning temperatures and (b) cleaning at 70°C by using different cleaning times, respectively.

various processing time and temperatures. The resultant leakage current density and electric breakdown field of the MOS capacitor with cleaning time of 10 min are shown in Fig. 11a. It is observed that cleaning temperature at 70°C exhibits a lower leakage current density and higher electric breakdown field than the other temperatures. The resultant leakage current density and electric breakdown field of the MOS capacitor with cleaning temperature at 70°C are shown in Fig. 11b. The cleaning time of 3 min demonstrates a higher leakage current density and smaller electric breakdown field than do the other times. This is due to the insufficient cleaning time and temperature. Consequently, the metallic and particle contaminants on the silicon wafer surface cannot be removed completely.

In another experiment, the cleaning efficiency of the one-step solution at higher temperature and short cleaning time was conducted. Experimental conditions are divided into six groups and shown in Table II. Figure 12 shows the cumulative distribution (in percentage) of the leakage current density. From the result, it is found that the TE2 method (EDTA + TMAH, at 80°C for 3 min) has the lowest leakage current among these methods. They show a significant improvement compared with RCA method. The breakdown field distribution is shown in Fig. 13. The TE2 method has the largest value of breakdown field. This result depicts that the one-step solution of SC-1 with both TMAH and EDTA is even better

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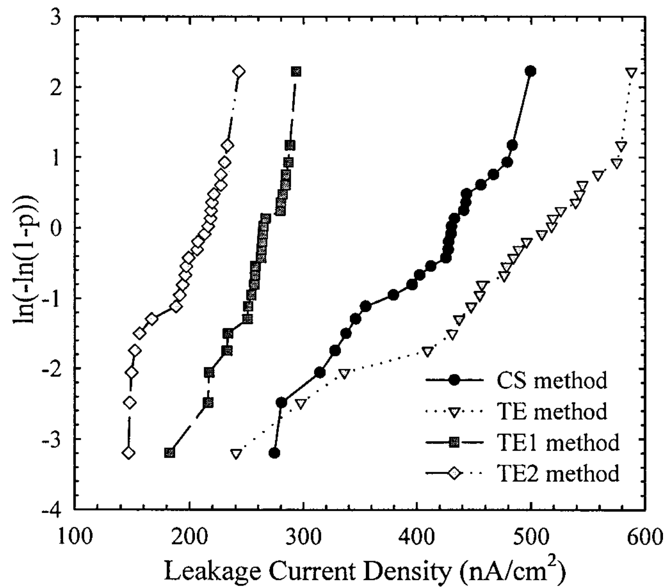

Figure 12. The cumulative distribution of leakage current density of MOS capacitors after cleaning with different cleaning methods. The oxide thickness is 3.7 nm.

than the already effective solution with EDTA the only additive provided that a higher temperature (80°C) and a shorter time (3 min) is used. This is because the TE2 method produces a smooth silicon surface ($R_{\mathrm{rms}} = 0.06$ nm) and excellent particle and metal removal performance (particle removal efficiency = 92.2-93.5%, metal removal is below the detection limit for all metals investigated). The one-step cleaning solution with EDTA and TMAH can be effectively used to replace the conventional two-step RCA cleaning process. Hence, the use of chemical, handling of waste, and time of processing can all be significantly reduced.

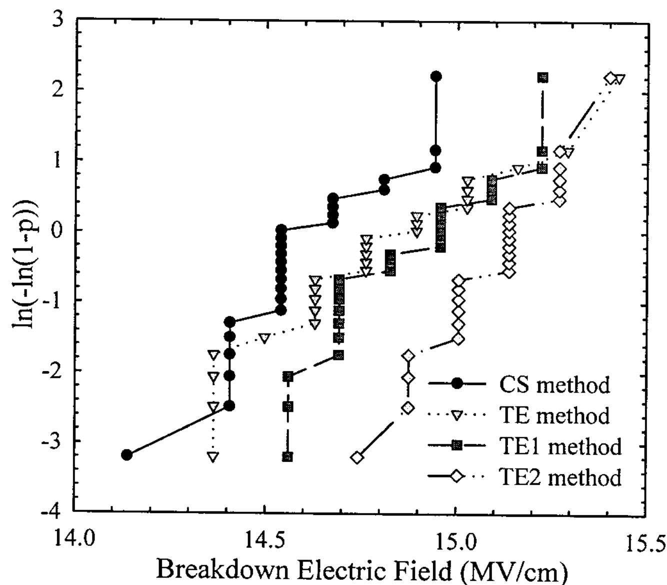

Figure 13. The breakdown field of MOS capacitor after cleaning with different cleaning methods. The oxide thickness is 3.7 nm.

Conclusions

The conventional wet cleaning process of semiconductor manufacturing process can be simplified if the SC-2 cleaning step is omitted by introducing a one-step cleaning solution, which added TMAH and/or EDTA into the SC-1. The tetramethylammonium cations of TMAH were explored for their effect on surface roughness, etching rate, and electrical characteristics of ultrathin oxide film. This finding can be explained with the surface adsorption and double layer behaviors of the tetramethylammonium ions of TMAH. Effect of silicon surface roughness, particle and metal on electrical properties of MOS capacitors, such as leakage current, electric breakdown field and charge-to-breakdown, were investigated to evaluate cleanliness of wafer surface. The SC-1 cleaning with TMAH is an effective way for particle removal, however, metal contamination is still found. The spiking of EDTA into the SC-1 solution demonstrates the effective performance for preventing metallic contamination. In addition, the one-step cleaning with the TE2 method (EDTA + TMAH, at 80°C for 3 min) exhibits better electrical properties than the conventional RCA two-step method because it is capable of removing particle and metallic impurity and has excellent surface smoothness. Hence, this one-step cleaning process is very promising for future large silicon wafer-size processing because it has the advantages of time-saving, low cost, and high performance.

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