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Analysis of Field Emission of Fabricated Nanogap in Pd Strips for Surface Conduction Electron-Emitter Displays

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We study the field emission (FE) property of a nanometer-scale gap structure in a palladium strip, which was fabricated by hydrogen absorption under high-pressure treatment. A vigorous cracking process could be accompanied by extensive atomic migration during the hydrogen treatment. A three-dimensional finite-difference time-domain particle-in-cell method is adopted to simulate the electron emission in a surface-conduction electron-emitter display (SED) device. Examinations of conducting characteristics, FE efficiency, the local field around the emitter, and the current density on the anode plate with one FE emitter are conducted. The image of a light spot is successfully produced on a phosphor plate, which implies that the explored electrode with nanometer separation possesses a potential SED application. Experimental observation and numerical simulation show that the proposed structure can be used as a surface conduction electron emitter and has a high FE efficiency with low turn-on voltage and a different electron emission mechanism. This study benefits the advanced SED design for a new type of electron source. [DOI: 10.1143/JJAP.47.2972]

KEYWORDS: nanometer-scale gap, high-pressure hydrogen absorption treatment, three-dimensional finite-difference timedomain particle-in-cell method, surface conduction electron-emitter display, conducting characteristics, field emission efficiency, current density distribution

1. Introduction

Nanometer-scale gaps are promising for electrodes in molecular electronics,^{1,2)} biosensors,³⁾ and vacuum microelectronics.⁴⁾ However, most relevant research on nanogaps are only in their infancy because of the complexity and unreliability of nanogap fabrication and the manipulation of nanosized constituents. One of the up-to-date applications of nanogaps is the surface conduction electron emitter (SCE) for flat panel displays (FPDs), which have attracted considerable attention since reported by Sakai *et al.*⁵⁾ The surfaceconduction electron-emitter display (SED) is a new type of FPD based upon SCEs. The potentiality of SCEs as field emission (FE) sources is superior to that of conventional cathodes in many respects. These SEDs possess the ability to obtain high-quality images, a high resolution, a quick response time, and low-power consumption,^{5,6)} where the FE efficiency is determined by the shape and material of the SCE. The key to the SCEs at the heart of the SED is an extremely narrow fissure made from an ultrafine-particle film between the two electrodes. Electrons are emitted from one side of the slit under a low driving voltage. Some of these electrons are scattered at the other side of the slit and accelerated by the high voltage applied between the anode and cathode, and they collide with the fluorescent coated glass plate, causing light to be emitted. The FE efficiency is determined by the topology and material of the SCE, but theoretical results of the FE property are not clearly understood yet.

In this work, we experimentally and theoretically explore the conducting characteristics, electron trajectories, current density distribution on an anode plate, and electron emission efficiency in the proposed SCE structure. The structure is a palladium (Pd) SCE fabricated by hydrogen absorption under high-pressure treatment⁷⁾ with a separation of about 90 nm width. A three-dimensional (3D) finite-difference time-domain particle-in-cell (FDTD-PIC) simulation for a self-consistent solution of the electromagnetic fields and charged particles is performed. Even though the multiple scattering model of the electron emission mechanism of the SCE has been proposed,⁸⁾ no simulation that includes full 3D fields and charged particles has been considered for the electron emission of SED yet. Consequently, a simulation technique that calibrates the theoretical model with the experimental data is developed to evaluate the characteristics of this SCE structure.

This paper is organized as follows. In §2, we briefly state the experimental procedure of the nanogap. In §3, the FDTD-PIC simulation method is described. In §4, both the measured and calculated results are discussed. Finally, we draw conclusions and suggest future work.

2. Experimental Procedure

Figure 1 schematically shows the structure of the SCE device. A p-type (100) silicon (Si) wafer was used as the substrate. A 150-nm-thick SiO₂ layer was first thermally grown on the Si substrate. The titanium (Ti) layer with 5-nm-thick was electron-beam-evaporation (e-beam) deposited on the oxide as an adhesion layer for the subsequently e-beam deposited platinum (Pt) thin film with a thickness of 10 nm. The pattering of the Pt/Ti line electrodes with a width of 80 μ m was photolithographically performed using a lift-off method. The Pd thin film of 30 nm thickness was then e-beam deposited on the Pt/Ti bottom electrode and the lift-off method was also used to pattern the Pd electrode line of 50 μ m length and 3 μ m width. A nanogap with a separation of 90 nm on the Pd strip was then produced by hydrogen absorption under high-pressure treatment.

It is known that for a system under tensile stress, the defects are often near singular strain points, such as step edge or crack tips. Therefore, we designed a Pd thin-film strip with a height difference to create a step edge, and then used high-pressure hydrogen treatment to form the nanometer-scale gaps. Once Pd is exposed to hydrogen gas,

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Fig. 1. (Color online) Schematic plot of SED structure and cross section of surface conduction electron emitter in x-z plane. The thicknesses of this device is shown in the bottom-right corner.



Fig. 2. SEM image of nanogap formed on Pd strip at 300 °C in SCE device. The width of the nanogap is approximately 90 nm.

adsorbed hydrogen atoms can quickly diffuse into the Pd lattice and occupy the interstitial site.⁹⁾ Therefore, crack initiation in the Pd thin film in the step region due to a high degree of stress concentration can result in the rupture of the Pd strip along the step edge via the process of stress relaxation through atomic diffusion driven by the stress gradient. On the microscopic scale, fracture proceeds in a ductile manner and occurs more reactively at higher temperatures. Hence, the degree of separation and edge roughness of the nanogap increase with temperature. Figure 2 shows plane-view scanning electron microscopy (SEM) images of the nanogap formed on a Pd electrode. The nanogap formed at 300 °C is approximately 90 nm in width. Notice that the width of the nanogap is very controllable at a given temperature. (It shows about 10% variation among nine samples with a 90 nm nanogap.) The electrical characteristics of the SCE were studied by measuring the conducting current between the two sides of the nanogap using a DC voltage power supply. The measurement was carried out under a vacuum condition of 1.0×10^{-6} Torr.

3. Numerical Simulation

We first formulate a calibration model with the experimental data using the numerical simulation. The FDTD-PIC codes are used in the numerical simulation, where the computational flowchart is shown in Fig. 3. The fundamentals of PIC are briefly described^{10–12)} as follows: starting from a specified initial state, we simulate electrostatic fields as its evolution in time. We then perform a time integration of Faraday's law, Ampere's law, and the relativistic Lorentz equation. The full set of Maxwell equations is simultaneously solved to obtain electromagnetic fields. Similarly, the Lorentz force equation is solved to obtain the relativistic particle trajectories. In addition, the electromagnetic fields are advanced in time at each time step. The charged particles are moved according to the Lorentz equation using the fields advanced in each time step. The weighted charge and current density at the grids are subsequently calculated. The obtained charge and current densities are successively used as sources in the 3D Maxwell equations for advancing the electromagnetic fields. These steps are repeated for each time step until the specified number of time steps is reached. In addition, the FDTD-PIC method allows the statistical representation of general distribution functions in phase space. The use of fundamental equations often contains the full nonlinear effects, and space charge and other collective effects¹³⁾ can be included self-consistently by coupling charged particles to the field equations via source terms. The particle treatment permits the incorporation of relativistic effects. In general, the PIC method employs fundamental equations without much approximation, allowing it to retain most of the physics. This 3D FDTD-PIC method thus approaches a self-consistent simulation of the electromagnetic fields and charged particles.

In the FE process, the electron emission is modeled using the Fowler–Nordheim (F–N) equation:¹⁴⁾

$$J = \frac{AE^2}{\phi t^2} \exp\left(\frac{-Bv(y)\phi^{3/2}}{E}\right),\tag{1}$$

where *A* and *B* are fitting parameters to be calibrated with the measured data, *E* is the normal component of the electric field at the emitter surface, ϕ is the work function of the emission material, t^2 is approximately equal to 1.1, and $v(y) = 0.95 - y^2$ with $y = 3.79 \times 10^{-5} \times E^{1/2}/\phi$ in International System of Units. The emission current density is determined by eq. (1) according to the local electric field, the work function of the emitter material, and geometric factors. We notice that all the dimensions of the physical quantities are the same with the experimental settings and the surfaces in the SCE are assumed to be smooth on the cell level in the entire simulation.

4. Results and Discussion

According to the calibrated model¹⁵⁾ and the experimentally measured data, Fig. 4(a) shows the measured and simulated current–voltage (I-V) characteristics for the sample with a 90 nm nanogap, where the V_g varies from 10 to 300 V and V_a is 0 V. The solid lines indicate the experimental data and the symbols are the simulation results. Also, the corresponding F–N plot of the FE of a Pd surface conduction electron emitter, shown in the inset of Fig. 4(b),



Fig. 3. (a) Computational scheme and (b) flowchart of PIC procedure for 3D simulation. Note that **E** and **B** are the electric and magnetic fields, **P** and **x** are the momentum and position of charge particles, and **J** and ρ are the current density and the charge density resulting from charge particles, respectively.



Fig. 4. (Color online) (a) *I–V* characteristics of SCE device with approximate 90 nm nanogap. (b) Corresponding F–N plot. The solid lines are measured data and the symbols are the simulated results obtained using the calibrated model.

is further calculated. Assuming a ϕ of 5.12 eV for Pd, the linear relationship indicates that the electron conduction followed the F–N FE mechanism. Two different turn-on voltages near 90 and 185 V are observed in the 90 nm nanogap, where the turn-on voltage is defined as the gate voltage at which the F–N plot begins to show linear



Fig. 5. (Color online) The simulated contour plot of electric fields in 90 nm nanogap, where V_g and V_a are equal to 60 V and 3 kV, respectively. The electric fields concentrate on the emitter apex and the electrons have energies sufficient to be tunneled from the metal to vacuum.

behavior, as marked by the circle and square in Fig. 4. This phenomenon is caused by the fact that the Pd–H system reacts vigorously when the temperature is higher such that the degree of separation and edge roughness of the nanogap increase. We can see that the edge of the nanogap in Fig. 2 is indeed very rugged. Hence, when the applied voltage is up to 90 V, the first turn-on voltage (circle) is found owing to the conducting of the nanogap with the part of shorter separations, and then the full region will turn on until the applied voltage attains a higher value, which is near 185 V (square) in this case.

Figure 5 shows the contour plot of electric fields near the nanogap, where V_a is 3 kV and V_g is 60 V. We found that the electric fields concentrate on the emitter apex and at the same time the electrons have energies sufficient to be tunneled from the metal to vacuum. The electron trajectory calculated by the 3D FDTD-PIC method is shown in Fig. 6. We clearly observe that electrons tunnel to the fissure region; some of the electrons are scattered at the right electrode and emitted into vacuum. The scattered electrons



Fig. 6. (Color online) (a) Electron beam ejected from SCE in x-z plane with V_g of 60 V and V_a of 3 kV. (b) Zoom-in plot around emitter. The electrons travel upwards to the phosphor plate when they escape from the fields generated by the gate electrode.

travel in the electric field, and some of the electrons falling onto the film are scattered again and go upwards to the phosphor plate owing to the high anode voltage. Hence, the motions of emitted electrons arriving at the anode are scattered on the film again and again until the electrons escape from the fields generated by gate electrode. The zoom-in plot of Fig. 6(a), around the emitter, is shown in Fig. 6(b), which more clearly shows the electron emission mechanism.

In addition, we calculated the dependence of electron emission efficiency on anode voltage and gate voltage using our simulation method. The electron emission efficiency (η) is defined as the current collected by the anode (I_a) divided by the emission current (I_e) ,

$$\eta \equiv I_{\rm a}/I_{\rm e}.\tag{2}$$

The power consumption and luminous efficiency of the SEDs are dominated by this parameter. Figure 7(a) shows the relationship between the currents (I_a and I_e) and anode voltage (V_a) with a fixed gate voltage of 80 V. The plot of electron emission efficiency versus anode voltage is shown in Fig. 7(b). It was found that the higher anode voltage increases the emission current. The calculated electron emission efficiency thus has the tendency towards a saturate region and attains a maximum of 50% in the 90 nm gap. This



Fig. 7. (Color online) (a) *I–V* curves of SED device with different anode voltages. (b) Dependence of electron emission efficiency on anode voltage.



Fig. 8. (Color online) Dependence of electron emission efficiency on gate voltage calculated using 3D FDTD-PIC technique.

is a very high efficiency compared with that of a prior report.⁸⁾ In the wider nanogap, more electrons are scattered at the right electrode and emitted into vacuum. The scattered electrons travel in the electric fields and travel directly upwards to the phosphor plate owing to the high anode voltage. This results in fewer electrons falling into the film. Therefore, the electron emission efficiency of the SCE with a 90 nm nanogap is higher than the SCEs with narrower nanogaps. Figure 8 shows the electron emission efficiency at





(b)

Fig. 9. (Color online) (a) Simulated current density distribution on anode plate. (b) The image of a light spot was produced on a phosphor plate, where V_g and V_a are 60 V and 3 kV, respectively.

a different gate voltage (V_g) and a constant anode voltage of 2 kV. We found that the efficiency is very low when V_g is increased. When the V_g becomes larger, it produces a very high electric field near the gate electrode. The high electric field narrows the potential barrier at the metal-vacuum interface sufficiently for the electrons to have a chance to tunnel from the solid into vacuum. Because the motions of the emitted electrons arriving at the anode are scattered on the film again and again until the electrons escape from the fields generated by the gate electrode, the electrons cannot go upwards to the phosphor plate if the fields generated by the gate electrode are too high. Therefore, this causes the electron emission efficiency to be lower at high V_g .

Figure 9(a) shows the simulated current density distribution on the anode plate at a V_g of 60 V and a V_a of 3 kV. The collected current is approximately 5 μ A, which was evaluated by integrating the current density over the area, and its value is large enough to allow for phosphor luminance. To illustrate the potential of the proposed SCE structure for display applications, the light spot, which is produced on the phosphor plate with a spacer 500 μ m away from the emitter, is shown in Fig. 9(b), where $V_a = 3 \text{ kV}$ and $V_g = 60 \text{ V}$. The SCEs occupying a total area of $160 \times 300 \,\mu\text{m}^2$ can produce a clear light spot with a diameter of 1 mm. It is worthwhile to note that electrons can actually be emitted toward the driver side from any part of the sidewall of the heightened cathode and move upwards to the phosphor plate owing the collection of anode voltage. The achieved performance coincides with the suppositions in refs. 5 and 6 and has significant potential applications for electron sources in FE displays.

5. Conclusions

We have fabricated a single nanogap in the Pd strip electrode with a SCE structure and developed a 3D simulation scheme for the electron emission in SED applications. Thus, the electron emission properties, the electron trajectories, the current density distribution on the anode plate, and the high emission efficiency of 50% have been investigated. The image of a light spot was successfully demonstrated on a phosphor plate, illustrating the potential of the proposed SCE structure for display technology. They promise the advantage of the SED design, and advanced applications using nanogap structure are now under consideration, including molecular devices and chemical sensors.

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