Electrical properties of shallow p + -n junction using boron-doped Si 1x Ge x layer deposited by ultrahigh vacuum chemical molecular epitaxy

Hsiang-Jen Huang, Kun-Ming Chen, Chun-Yen Chang, Tien-Sheng Chao, and Tiao Yuan Huang

Citation: Journal of Applied Physics **89**, 5133 (2001); doi: 10.1063/1.1321022
View online: http://dx.doi.org/10.1063/1.1321022
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/89/9?ver=pdfcov
Published by the AIP Publishing

Electrical properties of shallow p^+-n junction using boron-doped $Si_{1-x}Ge_x$ layer deposited by ultrahigh vacuum chemical molecular epitaxy

Hsiang-Jen Huang, Kun-Ming Chen, Chun-Yen Chang,[a] Tien-Sheng Chao, and Tiao Yuan Huang
Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 30050, Taiwan, Republic of China

(Received 16 March 2000; accepted for publication 5 September 2000)

Strained boron-doped $Si_{1-x}Ge_x$ layers with different Ge mole fractions were selectively deposited by ultrahigh vacuum chemical molecular epitaxy to form shallow p^+-n junction suitable for raised source/drain metal–oxide–semiconductor field effect transistor applications. Detailed electrical characterizations were performed. Our results show that the reverse leakage current could be optimized by a rapid thermal annealing at 950 °C for 20 s, and a near perfect forward ideality factor (i.e., <1.01) is obtained for the p^+-n $Si_{1-x}Ge_x$/Si junction. By analyzing the periphery and area leakage current components of p^+-n $Si_{1-x}Ge_x$/Si junctions with various perimeter lengths and areas, the degree of misfit dislocations and undercut effect were studied. The specific contact resistance was found to decrease as Ge mole fraction increases. Junction depth measurements also show that the junction depth decreases monotonically with increasing Ge mole fraction. The reduced B diffusion constant is attributed to the increasing Ge gradient in the transition region. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1321022]

I. INTRODUCTION

Heterojunction bipolar transistors with $Si_{1-x}Ge_x$ bases have been extensively studied in order to overcome the conflicting requirements between base-resistance and transit-time limitation inherent in the conventional bipolar transistors.[1–3] In addition, the SiGe layer has also been proposed for forming the raised source/drain regions of metal–oxide–semiconductor (MOS) field-effect transistors, as well as for optical device applications.[4,5] With a recent surge in research interest of the sub-0.1 μm complementary MOS technologies, the issue of forming a shallow p^+ source/drain junction with low contact resistivity to minimize the short channel effects while maintaining the high current drivability has been highly researched. Unfortunately, the conventional ion implantation method has become increasingly difficult for forming the required shallow junction due to channeling and radiation damage. To overcome these problems, several methods have been proposed. Among them, the simplest and the most promising approach appears to be the use of an upper doped layer.[6–11]

The upper doped layer can be selectively deposited on the active region to form a shallow junction by several methods including rapid thermal chemical vapor deposition (RTCVD),[12] and ultrahigh vacuum chemical molecular epitaxy (UHVCME).[7] For ultralarge-scale-integration applications, however, it is crucial to minimize postdeposition dopant redistribution during subsequent thermal processes. Although this can be accomplished by reducing the subsequent thermal budget, it usually places severe constraint on the subsequent process flexibility. Therefore, it would be advantageous to achieve minimum dopant redistribution by reducing the dopant diffusion constant. Previously, it has been pointed out that B diffusion from SiGe to Si is reduced in the SiGe/Si system due to the stress compensation effect.[9,10] In addition, misfit dislocation density is lowered by using selective epitaxial growth, compared to that of other large area deposition methods.[13,14] The selective epitaxial growth (SEG) feature is also advantageous in reducing the undesirable parasitic capacitance that often limits the transistor performance. Previously, the physical and electrical characteristics of selective SEG SiGe/Si diodes using RTCVD has been studied.[15,16] The propagation of misfit dislocations was discussed. Diodes fabricated in small deposited regions were shown to demonstrate more ideal forward characteristics than those fabricated in large regions. However, the effects of Ge ratio on the physical and electrical characteristics was not investigated.

The present article examines the structural and electrical properties of SEG $Si_{1-x}Ge_x$/Si p^+-n heterojunction diodes by using UHVCME-deposited $Si_{1-x}Ge_x$ layers with different Ge mole fractions x on wafers containing oxide patterns. Besides being a low temperature process, UHVCME is also known to be advantageous in minimizing the impurity contamination due to its low base pressure. The electrical characteristics and dislocations caused by undercut effects and misfit at $Si_{1-x}Ge_x$/Si interface were studied in detail by measuring diodes with various perimeter lengths and areas. A relative lower contact resistance is obtained with higher Ge composition in the $Si_{1-x}Ge_x$ layer. Finally, the junction depth reduction as a result of reduced B diffusion coefficient with increasing Ge composition is also discussed.

[a]Author to whom correspondence should be addressed; electronic mail: cyc@cc.nctu.edu.tw

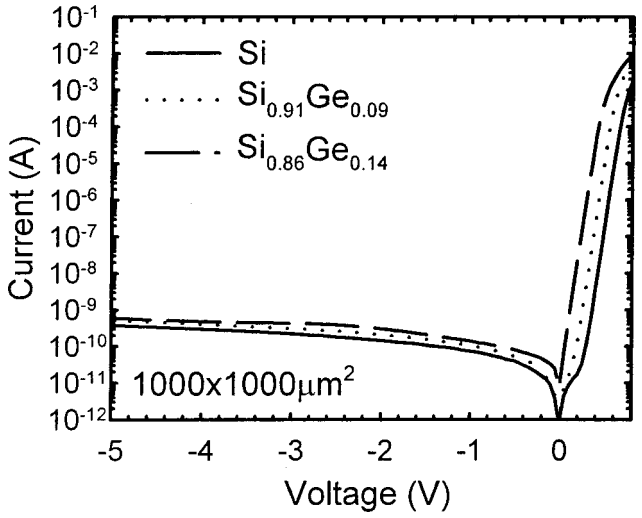

FIG. 1. The forward and reverse characteristics for SiGe/Si p^+-n junction with annealing at 950 °C for 20 s. The size of the diode area is 1000 $\times 1000\ \mu m^2$. The pure Si p^+-n junction was made for comparison. The epitaxial thickness of the SEG diodes is 100 nm.

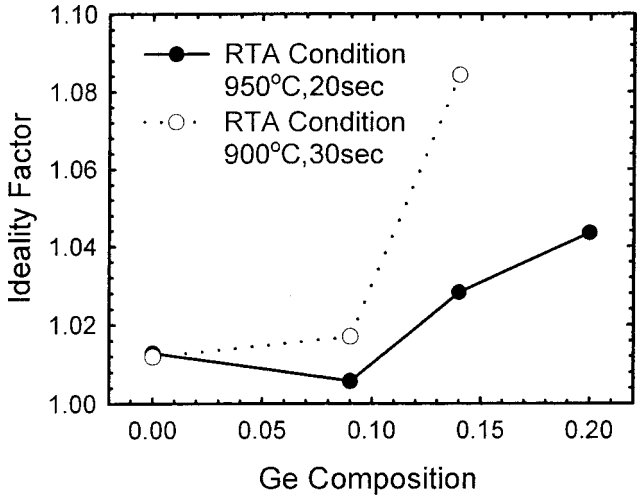

FIG. 2. Forward ideality factor vs Ge composition with different RTA conditions. Solid line denotes RTA temperature at 950 °C for 20 s and dotted line RTA temperature at 900 °C for 30 s.

II. EXPERIMENTS

n-type 6 in. (100) silicon wafers of 10–15 Ω cm resistivity were used as the starting Si substrates. A 300 nm isolation oxide was first formed to define the active areas with various periphery and area ratios (P/A). Then, following a standard RCA clean and a 1:50 HF:H_2O dip, a 100 nm B-doped $Si_{1-x}Ge_x$ ($x=0.09$, 0.14, and 0.2) layer was selectively deposited using the UHVCME system described previously.[7] Briefly, the growth chamber was pumped with a 1000 l/s turbomolecular pump to a standby base pressure of 2×10^{-10} Torr. Wafers were first loaded into the loading chamber, and immediately transferred to the growth chamber for selective epitaxial growth. A base pressure of 1×10^{-9} Torr was routinely established within 1 min after the wafer transfer process. Next, wafers were heated to the final deposition temperature of 550 °C at a ramp rate of ~150 °C/min. For growing the *in situ* B-doped $Si_{1-x}Ge_x$ layer, pure Si_2H_6, GeH_4, and B_2H_6 were introduced into the growth chamber. The chamber pressure was maintained below 1×10^{-3} Torr during epitaxial growth by the turbomolecular pump. Then, a 200 nm tetraethylorthosilicate passivation oxide was deposited, which was followed by a rapid thermal anneal (RTA) at various temperatures for dopant activation and outdiffusion. After contact opening, the TiN/Al–4%Cu/TiN/Ti four-layer metal was then sputtered and patterned to form the metal interconnect. Finally, wafers were sintered in N_2/H_2 at 400 °C before measurements.

The electrical characteristics were measured by a HP4145B semiconductor parameter analyzer. The sheet resistance was extracted using both the transmission length method (TLM)[17] and cross-bridge resistor method, while the contact resistance was measured by both TLM and Kevin cross structures. Finally, the diffusion profile was measured by using secondary ion mass spectroscopy (SIMS) in a Cameca IMS5f apparatus. To obtain better accuracy, boron and oxygen profiles were obtained by using O_2^+ and Cs^+, respectively, as the primary ion beams.

III. RESULTS AND DISCUSSION

A. Electrical characteristics

Figure 1 shows the forward and reverse current–voltage characteristics of $Si_{1-x}Ge_x$ diodes with different Ge compositions. All samples were annealed at 950 °C for 20 s. It can be seen that the reverse leakage current increases only slightly with increasing Ge composition. However, the saturation current increases dramatically with increasing Ge ratio, i.e., the saturation current density J_S is 63.8, 90.6, and 108.0 nA/cm^2 for Si control, $Si_{0.91}Ge_{0.09}$, and $Si_{0.86}Ge_{0.14}$SEG diodes, respectively. A larger J_S for the SiGe diodes with higher Ge composition is believed to be due to the increasing misfit dislocations caused by Ge atoms. In addition, at high current level, the $Si_{0.86}Ge_{0.14}$ diode also depicts the highest forward current among the splits, indicating a low contact resistance between metal and semiconductor junction and therefore a lower effective series resistance.

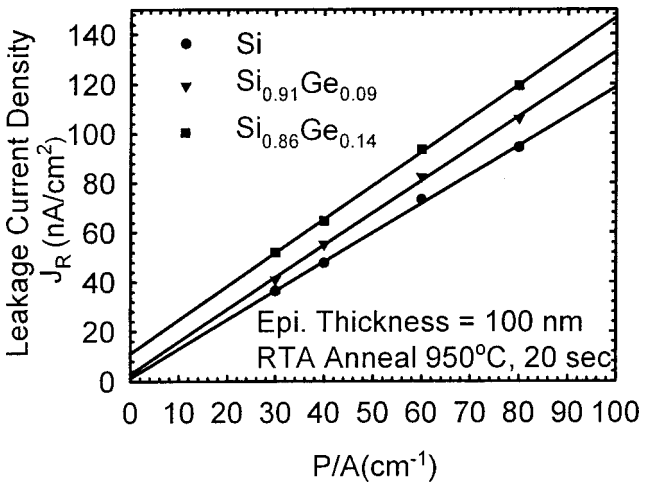

FIG. 3. The leakage current density J_R vs P/A ratio of SEG $Si_{1-x}Ge_x$ diodes which were annealed at 950 °C for 20 s. J_R is the reverse leakage current density of the p^+-n junction at −5 V.

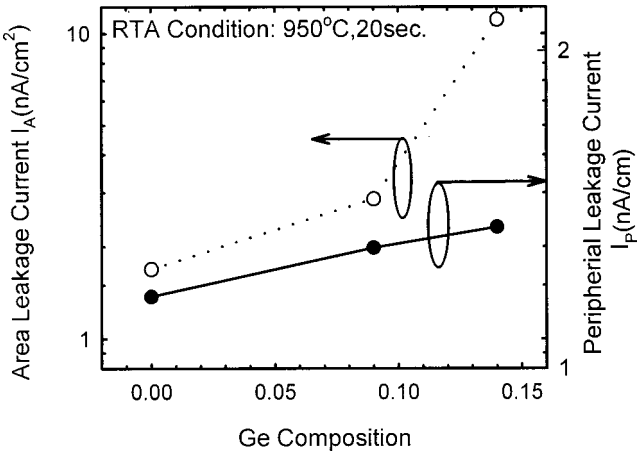

FIG. 4. The calculated value of peripherial component of leakage current J_P and areal component J_A vs Ge composition for SEG diodes after annealing at 950 °C for 20 s. The solid line is J_A, and dotted line is denoted J_P.

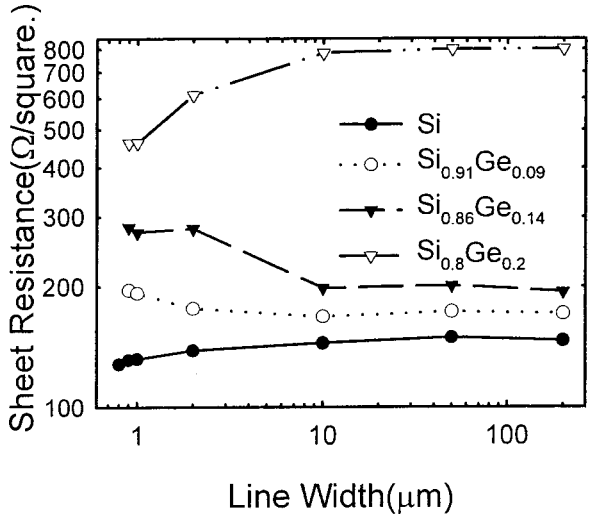

FIG. 6. Sheet resistance value vs linewidth of crossbridge resistors with different Ge mole fraction of $Si_{1-x}Ge_x$ layer deposited on the resistors.

It is also worth noting here that the $Si_{0.91}Ge_{0.09}$SEG diode depicts an ideality factor of better than 1.01 for over 7 decades.

The forward ideality factors versus Ge composition for different RTA conditions are plotted in Fig. 2. As Ge composition increases, generally the ideality factor increases due to the increasing amount of misfit dislocations associated with more Ge atoms. For a sufficient RTA thermal budget (e.g., 950 °C, 20 s), the measured junction depth is deeper than 50 nm, and a near-perfect ideality factor is obtained. However, as the junction depth becomes shallower, such as the case for samples receiving RTA at 900 °C for 30 s with a junction depth of about 44 nm, the ideality factor increases slightly from 1.028 to 1.084 for the $Si_{0.86}Ge_{0.14}$ diode. This is because with a shallower junction, more Ge atoms would increase the amount of defects lying within the depletion region, giving nonideal behavior.

Figure 3 shows the plots of reverse leakage current density J_R versus the the P/A ratio for diodes with different Ge compositions. All samples were annealed at the optimum RTA condition of 950 °C for 20 s. The reverse leakage current density was measured at -5 V. By separating the reverse leakage current density J_R into the area component J_A (nA/cm^2) and the periphery component J_P (nA/cm), and by using the equation

$$J_R = J_A + (P/A)J_P, \tag{1}$$

J_A can be found by the intersection of the straight line with the vertical axis, while J_P can be found by the slope of the straight line. The resultant J_A and J_P derived from these curves are summarized in Fig. 4. It can be seen that J_P values in a diode with a square or wide rectangular area are in general small and exhibit little change as Ge composition changes, suggesting the undercut effects along the isolation oxide edge during SEG process is reasonably small. In contrast, J_A values are relatively large and also increase with increasing Ge composition. This is believed to be due to the

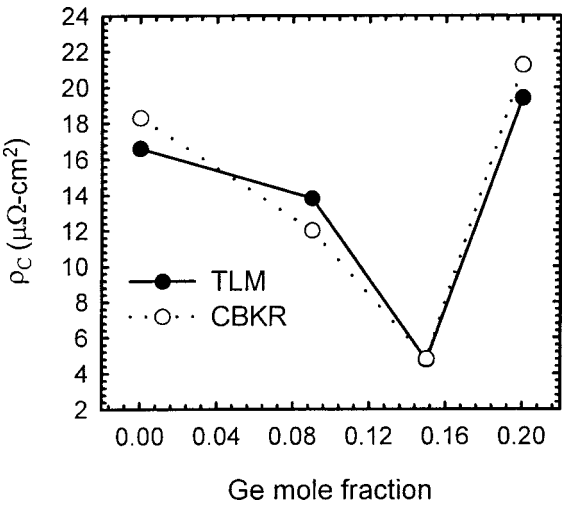

FIG. 5. The calculated specific contact resistivity using both the TLM method and Kelvin resistor (CBKR) method as a function of Ge mole fraction.

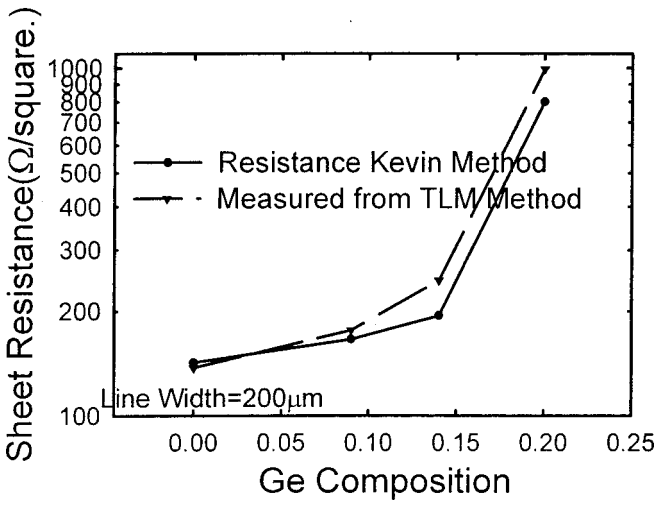

FIG. 7. The sheet resistance value measured from both the TLM method and crossbridge resistors. The crossbridge resistors used here are 200 μm in linewidth.

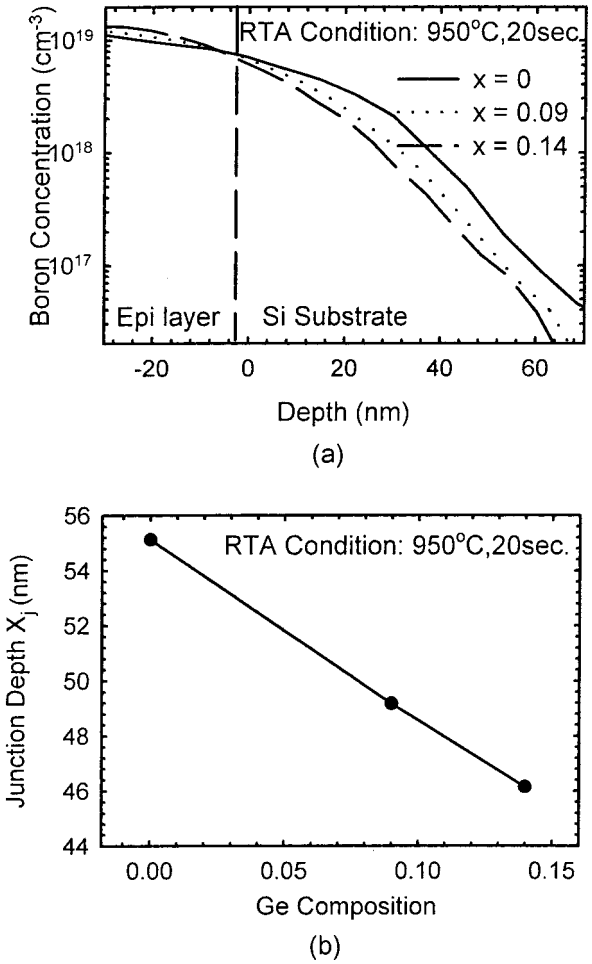

FIG. 8. (a) SIMS boron profiles and (b) junction depth vs Ge composition for strained SEG Si and $Si_{1-x}Ge_x$ layer on Si substrate with annealing at 950 °C for 20 s.

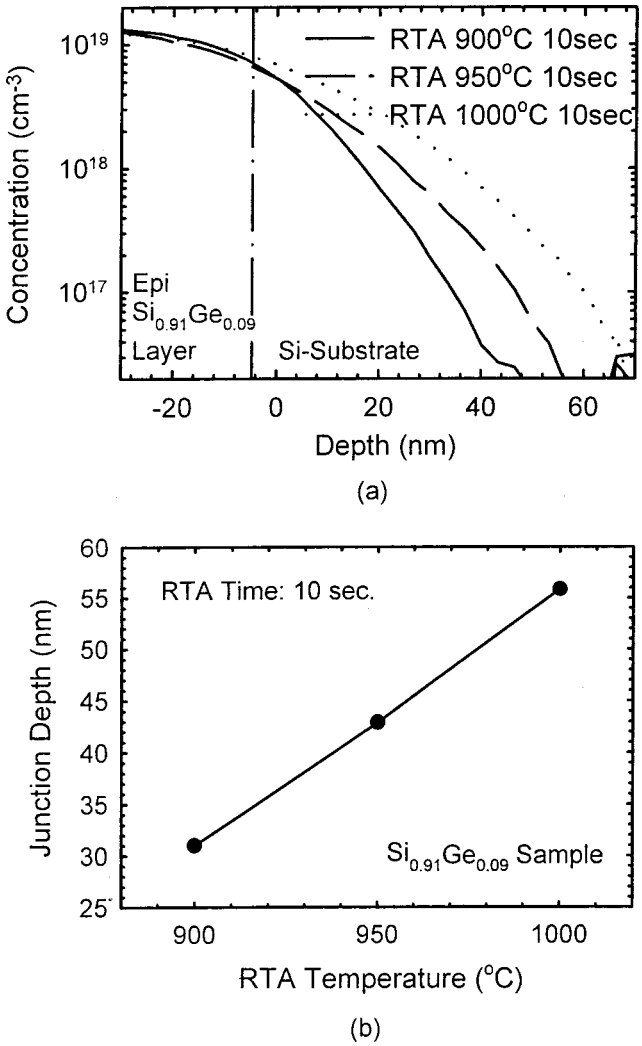

FIG. 9. (a) SIMS boron profiles and (b) junction depth as a function of anneal temperatures for strained $Si_{0.91}Ge_{0.09}$ layer on Si substrate with annealing at various temperatures for 10 s.

severe extension of misfit dislocations formed at the $Si_{1-x}Ge_x$/Si interface.[15] As a result, the areal leakage current constitutes a significant portion of the total leakage current, and degrades the reverse leakage performance. With increasing Ge composition, both the area and periphery leakage currents increase. Increased Ge content atoms result in more severe misfit dislocations and defects along the interface region, and thus worsen the leakage current.

Measurement of specific contact resistivity ρ_C was performed using both the TLM[17] and cross bridge Kelvin resistors. The results are summarized in Fig. 5. Only a small difference in specific contact resistivity ρ_C can be observed between the two methods. Theoretically, the barrier height φ_{BP} formed at the metal/semiconductor interface is known to be a critical factor in determining the contact resistivity ρ_C. It is known that the energy-band gap E_g of $Si_{1-x}Ge_x$ changes from 1.12 to 0.66 eV with increasing Ge mole fraction, and the conduction band edges are almost at the same level in metallurgical Si and SiGe junctions. However, the potential difference of the valence band will cause the lowering of the Schottky barrier height (SBH) in metal/$p^+Si_{1-x}Ge_x$ junction.[18] For the pseudomorphic p-$Si_{0.86}Ge_{0.14}$ layer, the SBH is expected to be lower than that of metal/p^+Si by 0.07 eV, which effectively reduces the specific contact resistivity ρ_C. From Fig. 5, the specific contact resistivity indeed decreases as the Ge relative ratio changes from 0 to 0.14, as predicted. A minimum ρ_C value of 4.8 $\mu\Omega\,cm^2$ is observed for the $Si_{0.86}Ge_{0.14}$ sample with low level *in situ* boron concentration of $1\times10^{19}\,cm^{-3}$ in the p^+ region. However, the ρ_C value jumps to a high value for a higher Ge ratio of 0.2. This is believed to be due to severe dislocations at the $Si_{0.8}Ge_{0.2}$/Si interface.

To study misfit dislocations and dislocations formed by undercut effects in detail, the sheet resistance ρ_S of each sample was measured by crossbridge Kevin resistors. The measured sheet resistance as a function of linewidth for various samples is plotted in Fig. 6. For the Si SEG control sample, sheet resistance decreases as the resistor linewidth decreases and reaches a minimum value of 123 Ω/□ for the Si control sample. This is because for a wider SEG area, the occurrence of dislocations and defects between the Si SEG region/Si substrate increases due to the propagation of misfit dislocation,[15] which leads to a higher sheet resistance value. On the contrary, for the $Si_{0.91}Ge_{0.09}$ and $Si_{0.86}Ge_{0.14}$ samples, the sheet resistance increases as the linewidth decreases, due

to dislocations caused by undercut around the field oxide edge. The undesirable undercut effect is believed to be formed during the prebake process which is used for oxide removal prior to the selective epitaxy growth.[16] The prebaking temperature was kept at 1000 °C for 10 s. The boundary between substrate and patterned oxide can be attacked by such a preclean process. During subsequent selective epitaxial deposition, the attacked region was partially refilled. Certain defects and dislocations were formed and nucleated at the edges of the oxide. This phenomenon is more apparent for the resistor with higher P/A ratio. Finally, for the $Si_{0.8}Ge_{0.2}$ sample, the sheet resistance decreases as the linewidth decreases. This is because for the sample with a high Ge ratio, the $Si_{0.8}Ge_{0.2}/Si$ interface misfit dislocations in the active region is much more severe than the undercut effects.

The effects of Ge composition on the sheet resistance value are shown in Fig. 7. The sheet resistance was measured by both TLM and crossbridge resistors. It can be seen that both methods yield the same trend that with more Ge mole fraction in the SEG region, the value of sheet resistance becomes higher, due to the increasing amount of misfit dislocations with more Ge atoms.

B. SIMS boron profiles and junction depth

Figure 8(a) shows the SIMS boron profiles of the SEG $Si_{1-x}Ge_x$ structure with different Ge compositions. All samples were annealed at 950 °C for 20 s. The B concentration in the underlying Si substrate becomes lower with increasing Ge composition in the SEG region. Furthermore, the depth of the p^+n junction is significantly reduced by using the $Si_{1-x}Ge_x/Si$ structure. In addition, all the B profiles, irrespective of Si or SiGe samples, are very similar to each other, indicating that the B diffusion constant in the SiGe layer is nearly identical to that in Si.[8–10] On the other hand, from the previous studies, the decrease of boron diffusion coefficient occurs only at the $Si_{1-x}Ge_x/Si$ interface region, which is the transition region from $Si_{1-x}Ge_x$ to Si. By increasing Ge composition in the SiGe layer, the Ge gradient in the transition region also increases, thus the effective B diffusion constant could be reduced. As a result, the reduction of boron junction depth is effective when the junction depth is located in the underlying Si substrate. By defining the junction depth as the depth when the B concentration equals $2\times10^{17}\,cm^{-3}$, the junction depth value for all the samples are summarized in Fig. 8(b). It can be seen clearly that the junction depth decreases monotonically as Ge composition increases. Figure 9(a) shows the boron SIMS profiles of the $Si_{0.91}Ge_{0.09}$ sample after annealing at various temperatures for 10 s. The calculated junction depths are plotted in Fig. 9(b). All the profiles are similar to each other. In addition, the incremental change of junction depth X_J is slower than that of the pure Si sample, i.e., for the Si sample with RTA at 1000 °C for 10 s, $X_J=62$ nm; however, for the $Si_{1-x}Ge_x$ sample at the same condition, X_J only equals 56 nm.

IV. CONCLUSION

The electrical characteristics of shallow p^+/n diodes fabricated by selective epitaxial growth of the boron-doped $Si_{1-x}Ge_x$ layer deposited by UHVCME were reported. It was found that the reverse leakage current could be optimized by a RTA at 950 °C for 20 s with near ideal forward characteristics for the $Si_{1-x}Ge_x$ diodes. The specific contact resistance is found to improve with increasing Ge mole fraction. In addition, the junction depth decreases with increasing Ge composition, due to reduced B diffusion constant as a result of increasing Ge gradient in the transition region. However, due to the severe undercut effects along the localized oxidation of silicon field oxide edge during the SEG process, the periphery leakage current constitutes a significant portion of the total leakage current, and degrades the reverse leakage performance. The generalized information in this study should be useful for novel solid phase diffusion process and MOS field effect transistor applications.

ACKNOWLEDGMENTS

The authors would like to thank Dr. W. F. Wu and Dr. H. C. Lin for experimental assistance. This work was supported in part by the National Science Council of the Republic of China through Contract No. NSC89-2215-E009-050.

[1] X. Xiao, C. Sturm, S. R. Parihar, S. A. Lyon, D. Meyerhofer, S. Palfery, and F. V. Shallcross, IEEE Electron Device Lett. **EDL-14**, 199 (1993).
[2] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbe, B. De Fresart, J. M. C. Stork, J. Y. C. Sun, D. L. Harame, and J. M. Burgatz, IEEE Electron Device Lett. **EDL-11**, 171 (1990).
[3] J. M. Stork, E. J. Prinz, and C. W. Magee, IEEE Electron Device Lett. **EDL-12**, 303 (1991).
[4] B. F. Levine, J. Appl. Phys. **74**, R1 (1993).
[5] J. S. Park, R. P. G. Karunasiri, and K. L. Wang, Appl. Phys. Lett. **61**, 681 (1992).
[6] T. F. Lei, T. P. Chen, H. C. Lin, and C. Y. Chang, IEEE Trans. Electron Devices **42**, 2104 (1995).
[7] L. P. Chen, C. T. Chou, G. W. Huang, and C. Y. Chang, Appl. Phys. Lett. **67**, 3001 (1995).
[8] S. M. Hu, Phys. Rev. Lett. **63**, 2492 (1989).
[9] S. M. Hu, D. C. Ahlgren, P. A. Ronsheim, and J. O. Chu, Phys. Rev. Lett. **67**, 1450 (1991).
[10] J. Sakano and S. Furukawa, Jpn. J. Appl. Phys., Part 1 **32**, 6163 (1993).
[11] P. Kuo, J. L. Hoyt, J. F. Gibbons, J. E. Turner, R. D. Jacowits, and T. I. Kanins, Appl. Phys. Lett. **62**, 612 (1993).
[12] D. T. Grider, M. C. Öztürk, S. P. Ashburn, J. J. Wortman, G. Harris, and D. Maher, J. Electron. Mater. **24**, 1369 (1995).
[13] D. B. Noble, J. L. Hoyt, C. A. King, J. F. Gibbons, T. I. Kamins, and M. P. Scott, Appl. Phys. Lett. **56**, 51 (1990).
[14] E. A. Fitzgerald, Y.-H. Xie, D. Brasen, M. L. Green, J. Michel, P. E. Freeland, and B. E. Wier, J. Electron. Mater. **19**, 949 (1990).
[15] T. I. Kamins, K. Nauka, R. D. Jacowitz, J. L. Hoyt, D. B. Noble, and J. F. Gibbons, IEEE Electron Device Lett. **EDL-13**, 177 (1992).
[16] T. I. Kamins, K. Nauka, R. D. Jacowitz, J. L. Hoyt, D. B. Noble, and J. F. Gibbons, J. Electron. Mater. **21**, 817 (1992).
[17] H. H. Berger, Solid-State Electron. **15**, 145 (1972).
[18] C. G. Van de Walle and R. Martin, Phys. Rev. B **34**, 5621 (1986).