Isolation on Si Wafers by MeV Proton Bombardment for RF Integrated Circuits

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***Abstract*—This paper studies issues related with using high energy protons to create local semi-insulating silicon regions on IC wafers for device isolation and realization of high-Q IC inductors. Topics on two approaches, i.e., one using Al as the radiation mask and the other using proton direct-write on wafers were studied. It was shown that Al can effectively mask the proton bombardment of 15 MeV up to the fluence of 10^{17} cm^{-2}. For the unmasking direct write of the proton bombardment, isolation in the silicon wafer can be achieved without damaging active devices if the proton fluence is kept below 1×10^{14} cm^{-2} with the substrate resistivity level chosen at 140 Ω-cm, or kept at 1×10^{15} cm^{-2} with the substrate resistivity level chosen at 15 Ω-cm. Under the above approaches, the 1 h-200 °C thermal treatment, which is necessary for device final packaging, still gives enough high resistivity for the semi-insulating regions while recovers somewhat the active device characteristics. For the integrated passive inductor fabricated on the surface of the silicon wafer, the proton radiation improves its Q value.**

***Index Terms*—Aluminum mask, annealing, flatband shift, proton bombardment, RF IC.**

I. Introduction

PLANAR on-chip inductors have been widely investigated for its integration to monolithic digital and RF integrated circuits [1]–[3]. However, inductors of high quality (Q) factors are hard to achieve on the silicon substrate for the lack of the technique to create effective insulating regions [2]. Recently, a method was proposed by Liao *et al.* [4] to create semi-insulating regions on IC wafers with high energy (10–30 MeV) proton bombardment prior to packaging. The technique raises the resistivity of the bombarded silicon substrate from 1–10 Ω-cm to 10^5∼10^6 Ω-cm. It is due to carrier removal by proton-created charge trappings [4]–[6] and the Coulomb scattering of the charged traps [4]. For this technique, the bombardment is performed after the wafer fabrication, making it compatible with the present micro-fabrication process. Hence, it is more attractive than other traditional approaches [7]–[11] to create isolation regions in IC.

To exploit further applicability of this technique to fabrication of high frequency IC, this paper studies in more details practical issues related with the technique. First, it studies the integration issue of masking for the proton bombardment. Then, to address the direct-write possibility without using mask, it studies the enhancement of resistivity with the proton fluence. The direct-write approach is based on the reasoning that a relatively low proton fluence can readily achieve regions of a very high resistivity on the substrate, which is originally of a relative high resistivity, for example, 140 Ω-cm, and at the same time only cause a slight, if any, degradation to nearby active devices even without masking. This may allow for the direct-write option to create high-Q RF components at relatively low cost and ease. It then includes thermal experiments to imitate packaging heat cycles to study the sustenance of the created semi-insulating regions to the thermal treatment. In addition, it includes a simple model to explain the improvement of Q factor for the irradiated integrated metal inductor.

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II. Experiments

In the conducted experiments, silicon wafers carrying MOS capacitors of n+ poly-Si gate, MOSFET's, resistors, and spiral inductors were used. On the wafers, MOS capacitors and MOSFET's were fabricated in the CMOS n-well region, which in turn were fabricated on p-type (100) 15 Ω-cm silicon substrates through implanting phosphorus at 100 keV for a dose of 1×10^{13} cm^{-2}. Resistors with four point ohmic contacts were fabricated in p-well regions which were formed by using a 50 KeV boron implant for a dose 1×10^{13} cm^{-2}. The gate oxide of MOSFET's of a thickness $\leq$60 Å was grown at 850 °C in dry O_2 followed by annealing in N_2 for 15 min. Then a layer of LPCVD α-Si of a 3000 Å thickness was deposited at 560 °C on the top of the gate oxide. Then, As of a dose of 5×10^{15} cm^{-2} was implanted at 50 keV into this poly-Si gate layer. After gate patterning and etching, BF_2 of a dose of 4×10^{15} cm^{-2}, and As of a dose of 5×10^{15} cm^{-2} were implanted into the substrate to form p+ and n+ ohmic contacts, respectively. After the BPSG deposition, Al contacts were formed, and sintered at 410 °C for 30 min. In addition, in order to study the effect of the initial substrate resistivity on the enhanced substrate resistivity under the 15 MeV proton bombardment, resistors were made separately on p-type (100) 15 Ω-cm and n-type (100) 2 Ω-cm substrates without extra underlying doping. Square spiral inductors of 2.5 turns were fabricated with an Al layer (2.8 μm thick, metal 2) patterned on the field oxide (1.65 μm thick) as shown in Fig. 1, where the metal width and space between adjacent turns were both 30 μm.

For the proton bombardment masking study, the proton beam irradiation setup is shown in Fig. 2. The proton fluence was set to

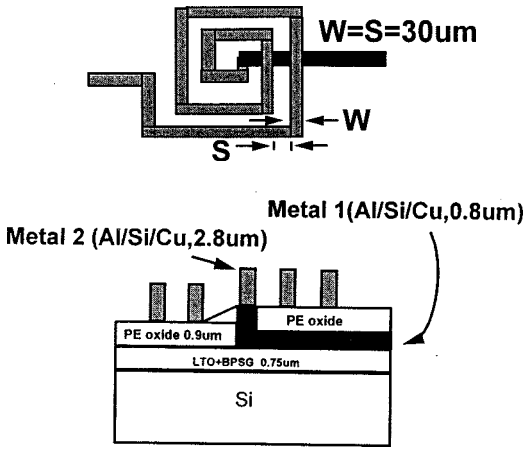

Fig. 1. Top view and cross-sectional view of the integrated spiral inductor.

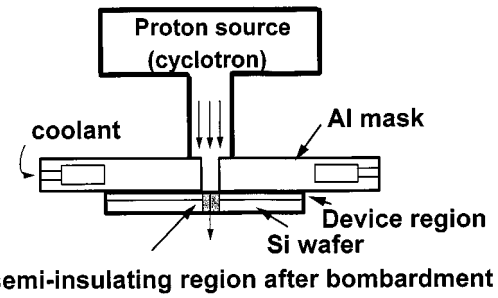

Fig. 2. Proton beam irradiation setup for patterning semi-insulating region on Si wafer.

10^{16}~10^{17} cm^{-2} at 15 MeV to simulate dose of the proton bombardment during the integration process. The projected range of the 15 MeV proton was approximately 1500 μm, which was much larger than the thickness of silicon wafers used in this experiment. The mask used was an Al mask due to its ease of fabrication and its relatively acceptable shielding capability [12]. The Al mask was of a thickness of 10 mm and had a hole of a square size of 13×13 mm^2, which was the size of fabricated chips. The diameter of the proton beam was 2 cm, which covered all the open hole of the mask during irradiation. Cooling water ran through the inner layer of the aluminum mask to maintain the mask at the room temperature. For the direct-write study, the proton fluence was chosen to be 10^{13}~10^{16} cm^{-2} and also at 15 MeV. No masks were used and wafers of resistivities of 15, 70, and 140 Ω-cm, which were relatively higher than the 3~5 Ω-cm resistivity of the conventional wafer, were used.

Following proton bombardments, I–V characteristics of MOSFET's were measured by using an HP-4145B device analyzer. Van der Pauw method [13] was employed to measure the substrate resistivity. The high frequency and quasistatic capacitances of capacitors, each of an area of 2.5×10^{-3} cm^{-2}, were measured by using a Keithley C–V analyzer. Hot plate heat treatment at 200 °C was imposed on the above IC wafers to study the isothermal annealing effect on the devices.

S-parameters of inductors were measured with an HP-8510B network analyzer. Before the measurement, a full two-port calibration was performed with the help of standard calibration substrate to extend the measurement port to the probe tip. In order to investigate the substrate loss effect of the inductor itself, the probe pad's effect were de-embedded by subtracting the Y parameters of the OPEN dummy pattern from the measured S-converted Y parameters [14]. This de-embedding procedure was re-done again after proton bombardment. The Q factor was determined by the ratio of the imaginary part to the real part of the one-port input impedance transformed from the measured de-embedded S-parameters.

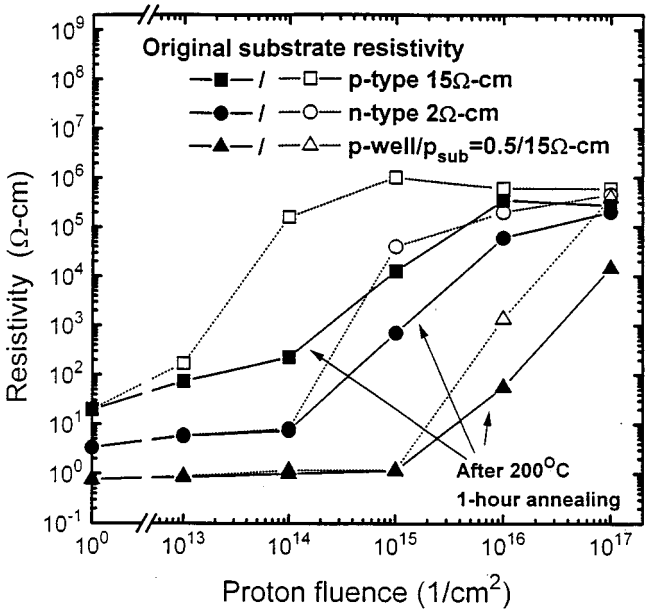

Fig. 3. Enhanced silicon resistivity as a function of proton fluence under various initial substrate resistivity before and after annealing. The annealing condition was 1 h 200 °C.

III. Results and Discussions

Fig. 3 shows the substrate resistivity as a function of proton fluence, before and after the thermal annealing, for substrates of various original resistivities. It can be seen that for each case the substrate resistivity increased with the bombarding proton fluence until it reached a final saturation level. For example, the resistivity of the sample with the original resistivity of 15 Ω-cm increased with the proton fluence and saturated at the value of about 5×10^5 Ω-cm at the proton fluence of about 1×10^{15} cm^{-2}. For a given proton fluence, the resistivity increase was more significant for samples of higher original resistivities. Moreover, it was noted that the resultant ultimate substrate resistivity for all cases was of almost the same value, i.e., approximately 5×10^5 Ω-cm, after receiving a proton fluence of 1×10^{17} cm^{-2}. After the 200 °C 1 h annealing, which simulated the packaging molding process of 200 °C 1 h thermal process, the resistivities of all samples decreased by one to two order, depending on the original starting resistivity and the bombarding proton fluence. For the 15 and 2 Ω-cm samples with 1×10^{15} cm^{-2} proton fluence, the resistivity decreased by one order.

For the masking study, Fig. 4 shows the reverse junction leakage distribution of p+/n diodes on the wafer before and after proton bombardment. The inset shows the mapping of test die sites. First, the die site#12 was exposed to 1×10^{16} cm^{-2} proton, while all other die sites were masked. The reverse junction leakage distribution of p+/n diode before bombardment

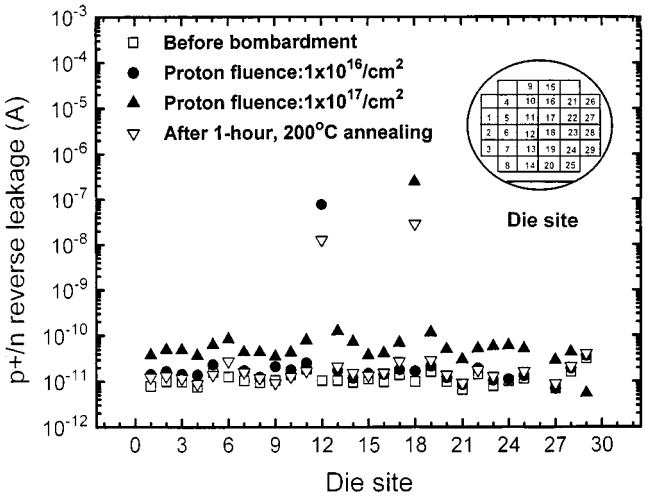

Fig. 4. The p+/n junction leakage distributions of masked and unmasked dies before and after proton bombardment and after 1-h, 200 °C annealing. Site#12 and site#18 were bombarded at 1×10^{16} cm^{-2} and 1×10^{17} cm^{-2} respectively with all other dies masked.

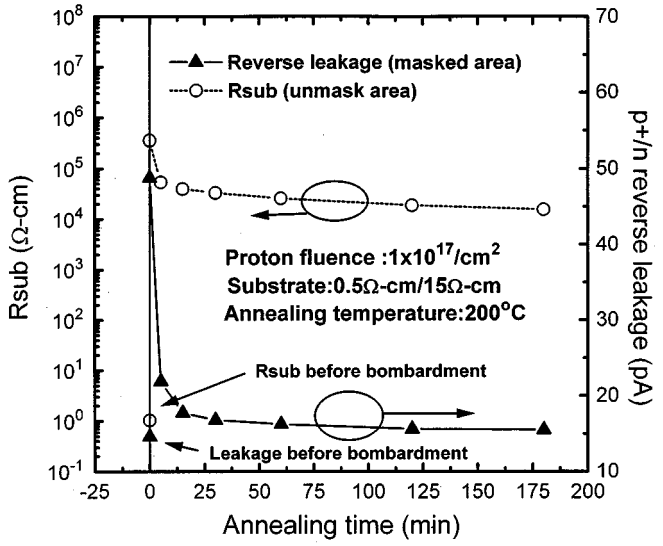

Fig. 5. Annealed characteristics of Rsub and the p+/n reverse junction leakage. The proton bombardment was at 1×10^{17} cm^{-2} and the annealing temperature was 200 °C.

were in the range of 8∼16 pA. After the 1×10^{16} cm^{-2} bombardment, the junction leakages of diodes of the masked area were almost not affected, approximately 12∼18 pA. However, the junction leakage of the diode of the unmasked area rose by a factor of $\sim 10^{3.5}$, which suggests that the defect density increased by the proton bombardment. Then, the site#18 was exposed to a 1×10^{17} cm^{-2} proton fluence while all other die sites were masked. The diode junction leakages of the masked area increased to 40∼110 pA, which indicates that the diodes of the masked area were affected by the proton bombardment. At the same time, the junction leakage of the diode in the unmasked area increased by a factor of $\sim 10^4$. After 200 °C annealing, the diode junction leakages of the masked area recovered to the range of 10∼20 pA, which was almost equal to the level before bombardment. That indicates the defects created by the high dose bombardment in the masked area can be annealed out by a 200 °C heat treatment.

Fig. 5 shows the p+/n junction leakage in the masked area and the Rsub, resistivity of the substrate, in the unmasked area after the 1×10^{17} cm^{-2} proton bombardment of Fig. 4 versus the annealing time for 200 °C annealing. It can be found that the Rsub increased from 1 Ω-cm to 4×10^5 Ω-cm after 1×10^{17} cm^{-2} proton bombardment. The reverse junction leakage of p+/n diode increased from 13 to 48 pA. The increase of Rsub by proton bombardment was due to the carrier removal mentioned previously. The Rsub and p+/n junction leakage of the bombarded sample reduced abruptly to a saturation level in the first 30 min of 200 °C annealing. The p+/n junction leakage recovered to its original level before bombardment, but Rsub maintained a level of 1×10^4 larger than its initial value. This suggests that the Al mask can be used to sustain a sufficiently high resistivity in the substrate for isolation purpose even after a 200 °C annealing thermal treatment is applied.

Fig. 6 shows the typical forward and reverse I–V curve of p+/n diodes in unmasked area. In the forward current region, the saturation current decreased with the proton dose, indicating the series resistance created by the proton bombardment. For

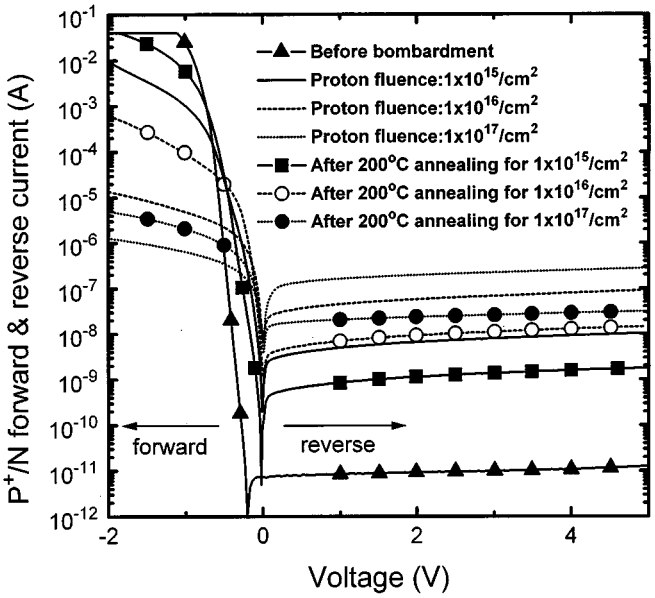

Fig. 6. Typical forward and reverse I–V curves of p+/n diodes in the unmasked area.

the reverse current, it was almost constant under reverse voltage bias, revealing that it was the generation current. It increased by a factor of approximately 2×10^4 for the proton dosage of 1×10^{17} cm^{-2} and a factor of approximately 1×10^3 for the proton dosage of 1×10^{15} cm^{-2}. After 1-h, 200 °C annealing, the forward saturation current increased and the reverse leakage current reduced, indicating the annealing of the defect density.

Fig. 7 shows the Arrhenius plots of J_R/T^3 versus $1/T$ for the diodes of the masked and unmasked areas respectively. The activation energy (Eg) deduced for the fresh sample (before bombardment) was 1.14 eV, which was approximately equal to the band-gap of Si, indicating that the reverse leakage current was due to the band-to-band generation [15]. For the samples after proton bombardment at the dose of 1×10^{16} cm^{-2}and 1×10^{17}

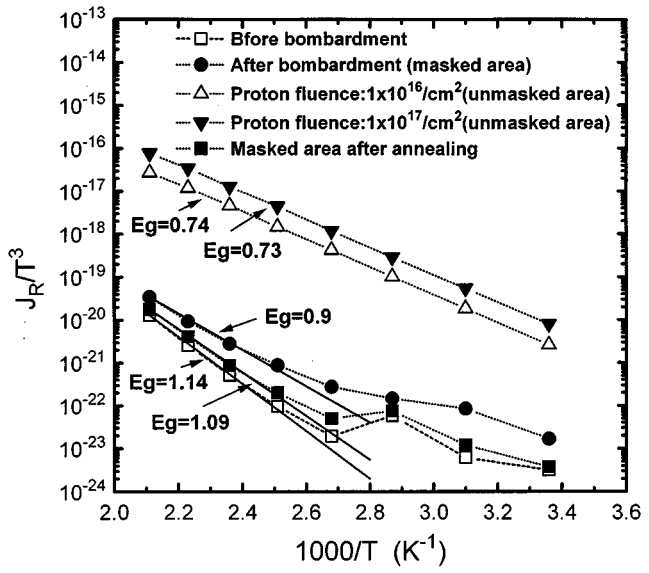

Fig. 7. Arrhenius plot of J_R/T^3 versus $1/T$ for the p+/n diodes of masked and unmasked areas respectively.

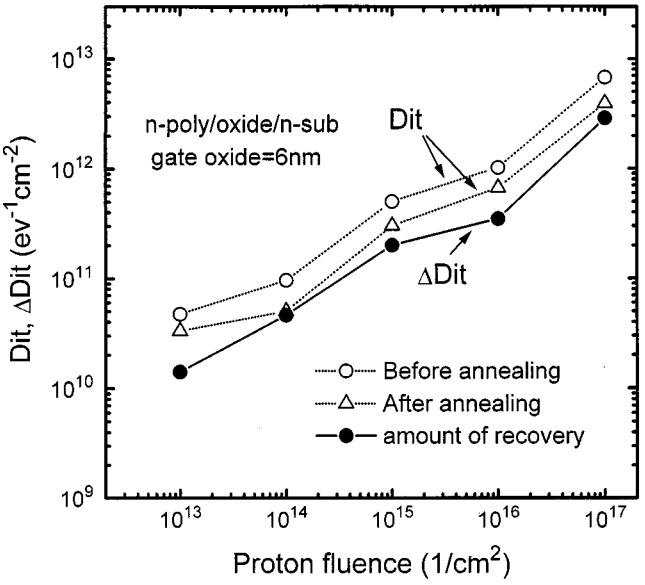

Fig. 9. Densities of interface states (Dit) under various fluences of the proton bombardment and the amount of recovery (Δ Dit) after 1-h, 200 °C annealing.

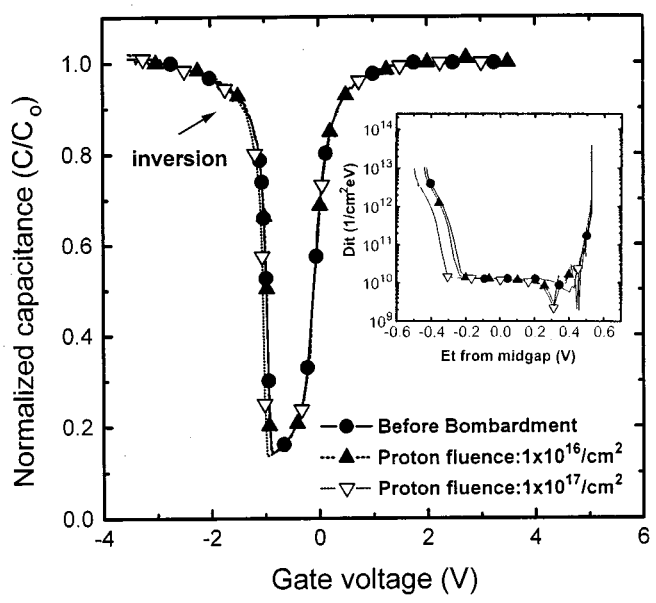

Fig. 8. Quasistatic C–V plots of n+ MOS capacitors in the masked area before and after proton bombardment at 1×10^{16} cm^{-2} and 1×10^{17}cm^{-2}, respectively. The insert shows the densities of interface states (Dit) as a function of he trap energy extracted from quasistatic and high frequency C–V curves.

cm^{-2}, Eg were approximately 0.74 and 0.73 eV respectively, indicating that the dominating recombination centers were located closed to the band center. In the masked area, Eg were approximately 0.94 eV after the proton bombardment at the dose of 1×10^{17} cm^{-2}, indicating that the leakage current of p+/n diodes was affected by this heavy dose of the proton bombardment. However, Eg recovered to approximately 1.09 eV after 1-h 200 °C annealing.

Fig. 8 show the quasistatic C–V for the n+ gate MOS capacitors in the masked area at die site #24, which was close to the bombarded die site, before and after proton bombardment. The gate oxide thickness was about 60 Å. It can be seen that all C–V curves were almost identical, indicating no increase in trapped charges or interface state densities after the bombardment. The insert shows the density of interface states (Dit) extracted for these samples. The Dit's were approximately 1×10^{10} cm^{-2}eV^{-1} in the midgap.

For the MOS capacitors without masking, the C–V curves became gradually distorted as the proton influence increased, For the proton influence less than 1×10^{14} cm^{-2}, the C–V curves only had slight distortion. As the influence increased to 1×10^{15} cm^{-2}, distortion became significant. The derived midgap interface state density (Dit) due to the proton bombardment, before and after 1 h-200 °C annealing, for different fluences are shown in Fig. 9. For the sample received the proton bombardment of the fluence of 1×10^{14} cm^{-2}, Dit increased to approximately 9×10^{10} cm^{-2}eV^{-1}, and for the 1×10^{15}cm^{-2} fluence, Dit increased to approximately 3.5×10^{11} cm^{-2}eV^{-1}. After 200 °C annealing, Dit recovered for various proton fluences. For example, for the 1×10^{14} cm^{-2}sample, Dit decreased to only 5×10^{10} cm^{-2}eV^{-1}. The amount of the recovery is also plotted in the figure, where, in general, Dit recovered more for the higher bombardment fluence.

Fig. 10 shows the subthreshold characteristics of pMOSFET's in the masked and unmasked areas respectively. The off- and the subthreshold characteristics were not affected by the proton bombardment of 1×10^{16} cm^{-2} and 1×10^{17} cm^{-2} in the masked area. They became worse for the devices of the unmasked area after the bombardment. However, for the proton fluence of 1×10^{16} cm^{-2}, the subthreshold increased from 70/dec to only 102/dec. Hence, it can be expected that it would increase less if the proton fluence was less than 1×10^{15} cm^{-2}.

Fig. 11 shows the Gm of pMOSFET's under various proton fluences. The Gm peak of pMOSFET's decreased as the proton fluence increased. The decrease of Gm can be attributed to the increase of interface states of the gate oxide and the defects created by the proton bombardment in the device channel. The degradation of the Gm peak was approximately 5% for the

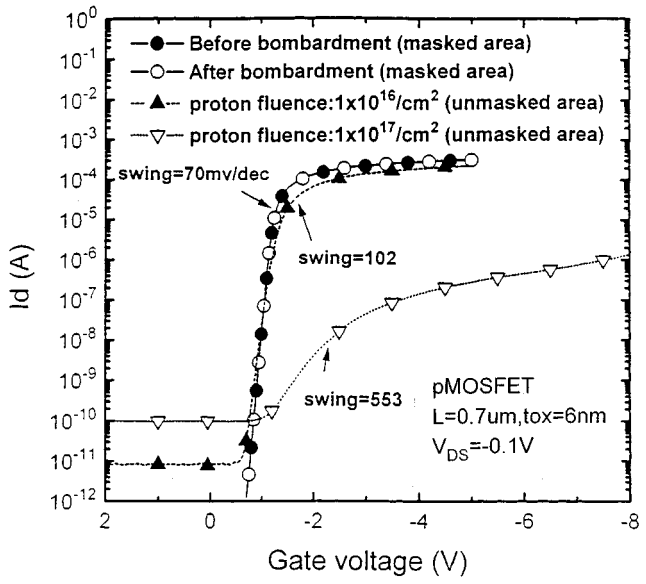

Fig. 10. Subthreshold characteristics of pMOSFET before and after the proton bombardment in the masked or unmasked areas.

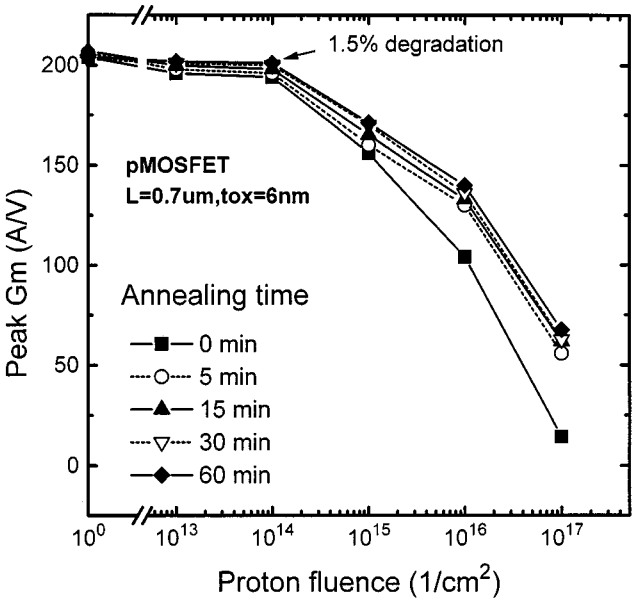

Fig. 12. Annealing effect on the peak Gm of pMOSFET under the various proton fluences. The annealing temperature was 200 °C.

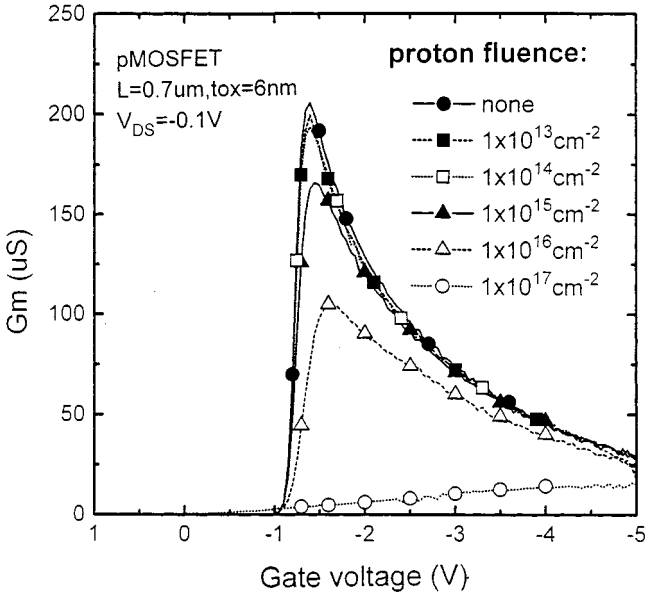

Fig. 11. Gm of pMOSFET under various fluences of the proton bombardment.

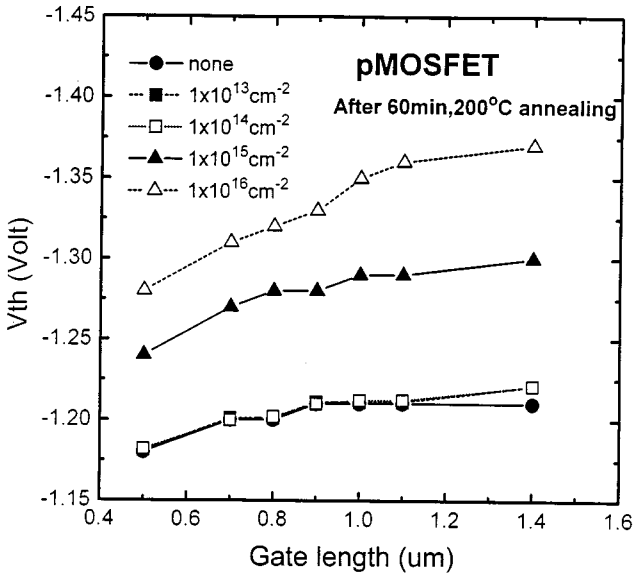

Fig. 13. Threshold voltage of pMOSFET as a function of the channel length under various fluences of the proton bombardment.

proton fluence of 1×10^{14} cm^{-2} and approximately 24% for the proton fluence of 1×10^{15} cm^{-2}. These degradations of Gm could be recovered by the 200 °C annealing. Fig. 12 shows the Gm peak recovery of devices under various proton fluences for different annealing time. The recovery rate was larger for samples of the higher fluence of the proton bombardment. The peak Gm degradation became approximately 1.5% for the proton fluence of 1×10^{14}cm^{-2} and 16% for the fluence of 1×10^{15} cm^{-2} after annealing.

Fig. 13 shows the Vth, the turn-on voltage of the devices, plotted in terms of the channel length, as a function of the bombardment fluence. The devices had received the 1-h, 200 °C annealing. Vth almost did not change for the proton fluence below 1×10^{14} cm^{-2}, and shifted to more negative values as the proton fluence increased to above 1×10^{15} cm^{-2}. This indicates that observable positive charges were created in the oxide for the proton bombardment above this value.

As a summary of the above data, it can be concluded that the interface state density, Gm, threshold voltage of a MOSFET is only slightly affected under the proton bombardment below 1×10^{14} cm^{-2} after a 1-h, 200 °C annealing. This implies that if a sufficiently high Rsub can be obtained at a low fluence proton bombarded (less than 1×10^{14} cm^{-2}) on the Si substrate, it is possible to get negligible degradation on active devices.

Fig. 14 shows the annealing effect on Rsub of p-type substrates of various resistivities under various fluences of the proton bombardment. For the 15 Ω-cm substrate, a proton bombardment above 1×10^{14} cm^{-2} raised Rsub of all substrates

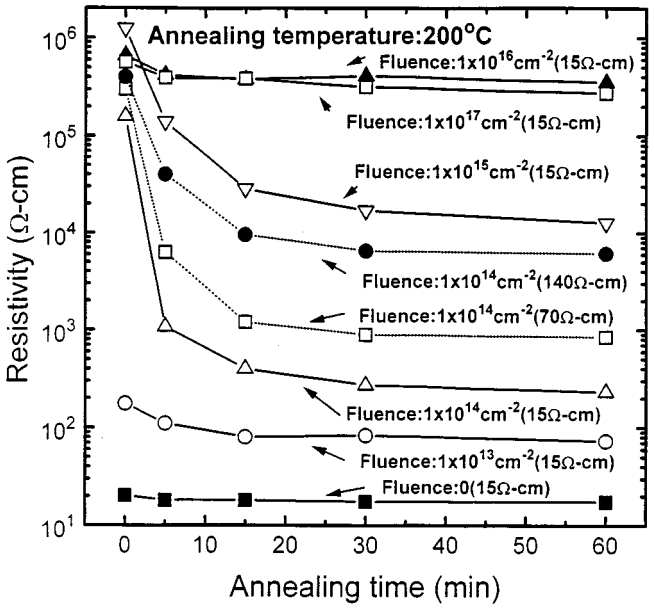

Fig. 14. Isothermal-annealed characteristics of Rsub for various fluences of the proton bombardment on the 15 Ω-cm substrate and for the 1×10^{14} cm^{-2} bombardment on substrates of various resistivities.

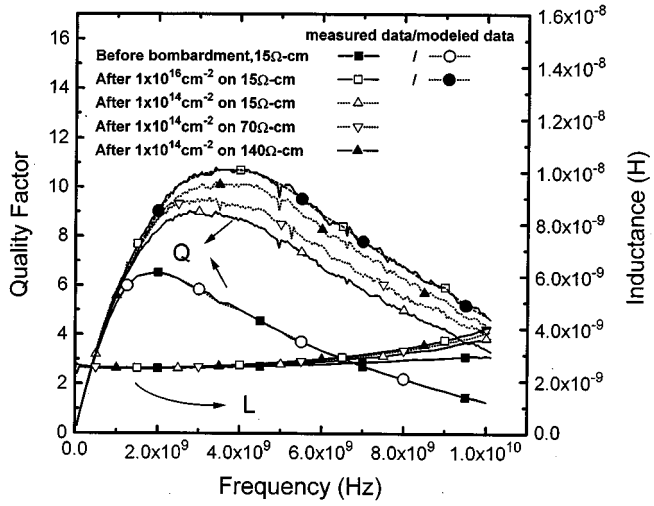

Fig. 15. Measured Q factor and inductance of the inductor as a function of frequency for the 1×10^{16} cm^{-2} proton bombardment on the 15 Ω-cm substrate and for the 1×10^{14} cm^{-2} bombardment on substrates of various resistivities after 1-h, 200 °C annealing. Simulated characteristics of the Q factors of inductors before and after the 1×10^{16} cm^{-2} bombardment are also shown.

to the level above 10^5 Ω-cm, but Rsub decreased rapidly to different levels, depending on the starting resistivity, in the first 30 min of annealing. After that, the decreasing rate became less in the succeeding annealing time. For the same proton level of 1×10^{14} cm^{-2}, the substrate with the higher starting resistivity had the higher the saturated value of Rsub. For the substrate of the original resistivity of 140 Ω-cm, Rsub could increase to $\sim 6 \times 10^3$ Ω-cm. It is noted that for the 15 Ω-cm sample, with a proton fluence of 1×10^{15} cm^{-2}, it could still achieve a Rsub of $\sim 1 \times 10^4$ Ω-cm after 1 h-200 °C annealing.

Fig. 15 depicts the Q factor of the previously mentioned 2.5-turn spiral inductor, before and after the proton bombardment followed by 1 h-200 °C annealing treatment, as a function of the measurement frequency. It is observed that as driving frequency increased, the typical Q factor first increased to maximum ($Q\max$) and then gradually decreased. This can be understood as that at low frequencies the Q factor is proportional to $\omega L_S/R_S$, while its suppression starts to cut in due to the degrading effects facilitated by the combined action of C_{SB}, C_{OX}, and R_{SB} [16], [17] at higher frequencies. In the above, C_{OX}, R_{SB}, L_S, and R_S, ω, represent the oxide capacitance, substrate resistance, inductance and resistance of the inductor, and the driving frequency, respectively. The increase of $Q\max$ after the proton bombardment is caused by the reduction of the substrate-rendered AC losses. A simple lumped-parameter model of Fig. 16 was used to analyze the above phenomenon. In Fig. 15, for the 15 Ω-cm sample, the Q factor curves before and after the 10^{16} cm^{-2} proton bombardment were simulated with the model of Fig. 16, where the substrate resistivity was increased from 15 Ω-cm to about 0.5 MΩ-cm (see Fig. 3). Model parameters were extracted by fitting the experimentally measured S-parameters, and a plausible solution was obtained and tabulated in Table I, where L_S, R_S, and C_P represent inductance, inductor metal resistance, and parasitic capacitance between metal lines, respectively.

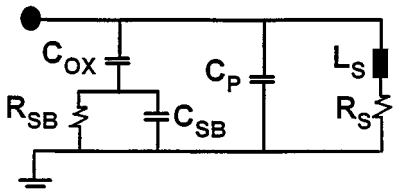

Fig. 16. Lump-element model for simulation of the inductor.

TABLE I
EXTRACTED INDUCTOR MODEL PARAMETERS BEFORE AND AFTER THE PROTON BOMBARDMENT

Proton	L_S (nH)	$R_{SO}(\Omega)$	k_1	k_2	C_P(fF)	C_{OX}(fF)	C_{SB}(fF)	$R_{SB}(\Omega)$
Before	2.35	2.6	0.05	1.52	27	200	12	335
After	2.5	2.44	0.02	1.52	25	200	2.7	1320

Note that R_S has taken into account the skin effect and can be expressed as [17]:

$$R_s = R_{so}(1 + k_1 \omega k_2)$$

where R_{SO} is the dc series resistance of the whole metal spiral, ω is the driving frequency in GHz, and k_1 and k_2 are empirical parameters.It was observed that the great increase of R_{SB} indeed was responsible for the improvement of inductor Q value. In addition, in the above, the inductance was not affected too much by the proton bombardment. Hence, the proton bombardment improves the performance of the integrated inductor.

IV. CONCLUSION

In this paper, several topics related with the technique of using the proton radiation to create isolation regions in silicon wafers for device integration purpose have been studied. It has been shown that the Al masking is an effective means to shield ac-

tive devices and to pattern semi-insulating regions on a silicon wafer for the proton bombardment even up to the fluence of 10^{17} cm^{-2}. It has also been shown that the unmasking direct write of the proton bombardment can be used to achieve isolation in silicon wafer if the proton fluence is kept below 1×10^{14} cm^{-2} with the substrate resistivity level chosen at 140 Ω-cm, or kept at 1×10^{15} cm^{-2} with the substrate resistivity level chosen at 15 Ω-cm. This is especially true if the integrated circuit is composed of only MOS devices. Under the above approaches, the 1 h-200 °C thermal treatment, which is for the device final packaging step, will recover the active device characteristics somewhat, but still give enough high resistivity for the semi-insulating regions. As for the integrated passive inductor fabricated on the surface of the silicon wafer, the proton radiation improves its performance on the Q value.

Thus, one can conservatively conclude that solution exits for integrating with active devices with high performance inductor that receive proton bombardment procedure. For Al mask approach, it is expected that shielding larger passive inductors by using this thickness of Al mask is very easy. The proton energy and Al thickness can even be reduced to improve the mask lateral dimension. For low dose approach, however, additional work must be done. For example, it need to modify Si process with originally high substrate resistivity.

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