On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Process

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***Abstract*—A novel on-chip electrostatic discharge (ESD) protection design by using polysilicon diodes as the ESD clamp devices in CMOS process is first proposed in this paper. Different process splits have been experimentally evaluated to find the suitable doping concentration for optimizing the polysilicon diodes for both on-chip ESD protection design and the application requirements of the smart-card ICs. The secondary breakdown current (It2) of the polysilicon diodes under the forward- and reverse-bias conditions has been measured by the transmission-line-pulse (TLP) generator to investigate its ESD robustness. Moreover, by adding an efficient VDD-to-VSS clamp circuit into the IC, the human-body-model (HBM) ESD robustness of the IC with polysilicon diodes as the ESD clamp devices has been successfully improved from the original ∼300 V to become ≥3 kV. This design has been practically applied in a mass-production smart-card IC.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection circuit, polysilicon diode, smart card, transmission-line-pulse (TLP) generator.**

I. Introduction

In THE smart-card IC application, the electrical power for circuit operations is generated from the transformer (formed by several loops of planner inductor on the circuit board) and the on-chip bridge rectifying circuit into the smart-card IC. The traditional full-wave bridge rectifying circuit formed by four diodes to convert the ac power into dc power is shown in Fig. 1. An ac voltage between terminals Vs1 and Vs2 is rectified into a dc voltage and stored in the capacitor Cs for application across the load. When the smart card is close to a card reader (or detector), the electromagnetic field generated from the card reader is coupled by the transformer in the smart card and charges up the electrical power of the smart card for circuit operation. The coupled ac power is converted into dc power by the on-chip four-diode bridge rectifying circuit in the smart-card IC. With the converted dc power, the information stored in the smart-card IC can be emitted out and detected by the card reader for personal identification or other applications. The typical application of such a smart-card IC to enter a controlled door is illustrated in Fig. 2.

When the on-chip rectifying circuit is realized in a CMOS IC with a p-type substrate, the diodes D1 and D2 are often made by the p–n junctions across p+ diffusion and n-well. The diodes D3 and D4 are often made by the p–n junctions across n+ diffusion and p-substrate. The diode device structures in a CMOS IC with a common p-substrate are illustrated in Fig. 3. Due to the common p-substrate of a CMOS IC, besides the diode structures in Fig. 3, there are four parasitic bipolar junction transistors (BJTs), Q1, Q2, Q3, and Q4, in this structure. Q1 (Q2) is a parasitic vertical p–n–p BJT between the Vs1 (Vs2) and the common p-substrate. Q3 (Q4) is a parasitic lateral n–p–n BJT between the Vs2 (Vs1) and the VDD-biased n-well. These parasitic BJTs would cause the degraded rectification efficiency, or even no rectification at all, for the full-wave bridge rectifying circuit. The parasitic BJTs are drawn into the full-wave bridge rectifying circuit and illustrated in Fig. 4 to show its influence. When the ac voltage is in

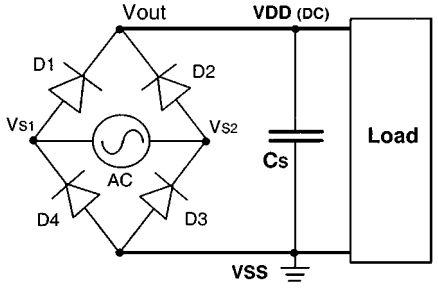

Fig. 1. Traditional full-wave bridge rectifying circuit formed by four diodes to convert the ac power into dc power.

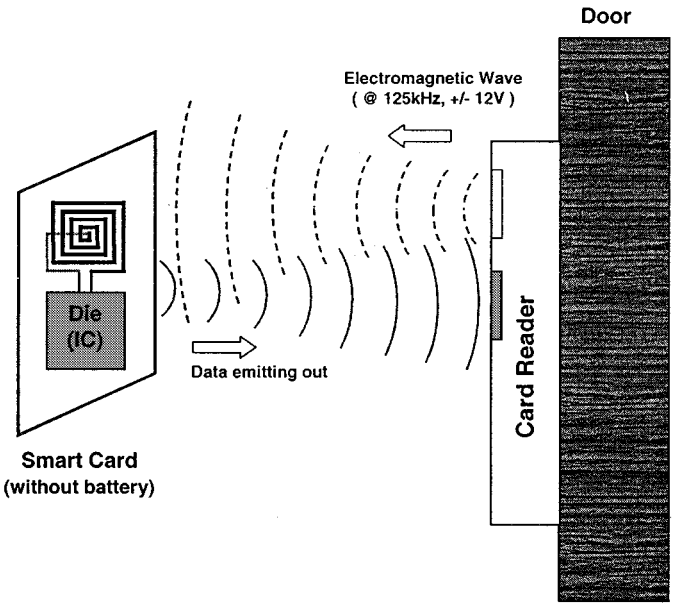

Fig. 2. Typical application of a smart-card IC for personal identification to enter a controlled door.

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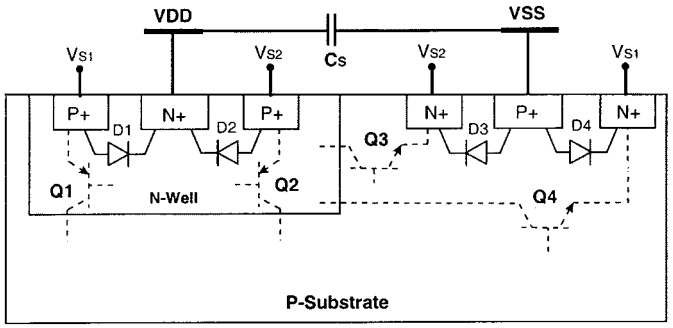


Fig. 3. Device cross-sectional view of the four p–n junction diodes of the full-wave bridge rectifying circuit realized in a CMOS IC with a common p-type substrate.

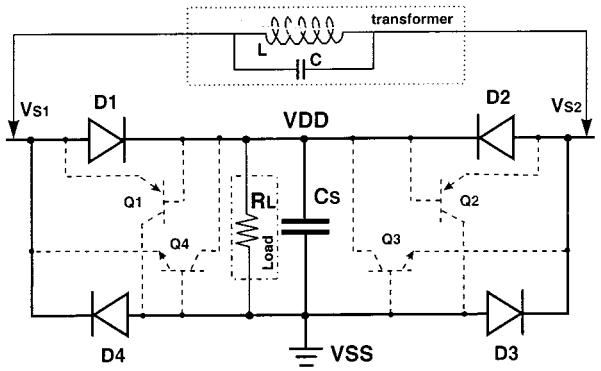


Fig. 4. Leakage current paths along the parasitic BJTs in the traditional full-wave bridge rectifying circuit realized in CMOS IC with a common p-type substrate.

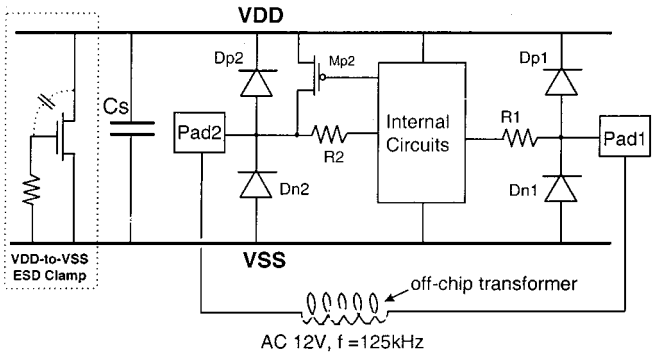


Fig. 5. On-chip bridge rectifying circuit in a smart-card IC realized by four polysilicon diodes with the original design of on-chip ESD protection circuits.

its positive half-wave period (Vs1 > Vs2), the base–emitter junction (the diode D3) of the parasitic BJT Q3 is forward biased to turn on the BJT Q3. Thereby, a great amount of charge current is created that directly flows through the parasitic BJT Q3 (from VDD node to Vs2) instead of through the capacitor Cs. During the positive half-wave period (Vs1 > Vs2), the diode D1 is also forward biased and therefore turns on the parasitic BJT Q1. Some of the charge current is directly flowing through the parasitic vertical BJT Q1 (from Vs1 to VSS node) instead of through the capacitor Cs. Similarly, the same problem caused by the parasitic BJTs Q2 and Q4 occurs during the negative half-wave period (Vs1 < Vs2). Therefore, the rectification efficiency of this full-wave bridge rectifying circuit realized in the CMOS IC with a common substrate is seriously decreased, and could even have no rectification at all.

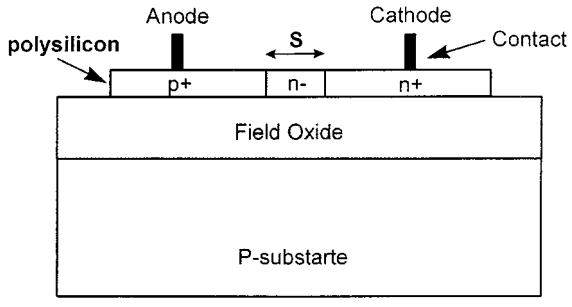
In some modified design, the diodes may be changed to nMOS or pMOS devices in the full-wave bridge rectifying circuit for realization in CMOS IC [1]. The parasitic vertical or lateral BJTs still exist among such device structures to degrade its rectification efficiency. Moreover, the different connections between the bulk and the source of nMOS or pMOS devices in the full-wave bridge rectifying circuit cause the body effect to degrade the power-converting speed and results in a poor rectification efficiency [1].

If the diodes in the full-wave bridge rectifying circuit are realized by the polysilicon diodes, which have no parasitic BJT in their device structures, the aforementioned problem can be totally eliminated. Therefore, the rectification efficiency can become much higher to convert the coupled ac power into dc power for circuit operation in a smart card. However, due to the low heat dissipation capability of the polysilicon layer, the polysilicon diodes connected at the VS1 and Vs2 nodes (which are wire bonded to the circuit board in the final application) result in a very low human-body-model (HBM) electrostatic discharge (ESD) level of around 200–300 V. With such a low ESD level, the die of a smart-card IC assembled into the smart card by chip-on-board (COB) bonding is very susceptible to ESD events. This limits the ability to mass produce this smart-card IC.

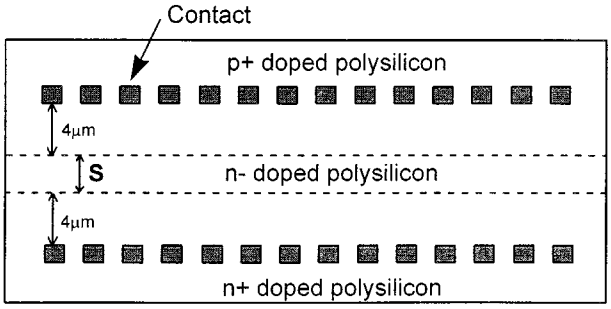
In this paper, the breakdown voltage, leakage current, and ESD performance of the polysilicon diodes are first evaluated in the literature by performing different n- or p-type doping concentrations with experimental process splits. The dependence between the secondary breakdown current (It2) (measured by the transmission-line-pulse generator) and layout spacing in the polysilicon diodes is also characterized in detail. The HBM ESD level of the smart-card IC can be finally improved to $\geq$3 kV by using a new power-rail ESD clamp circuit with the stacked polysilicon diodes as the turn-on control circuit [2].

II. Original Design in a Smart-Card IC

Due to the aforementioned concerns on both leakage and substrate current in practical smart-card applications, the four-diode bridge rectifying circuit cannot be simply realized by using the n+/p-substrate or the p+/n-well junction diodes in a bulk CMOS process. Therefore, the on-chip bridge rectifying circuit in this smart-card IC is realized by four polysilicon diodes, as shown in Fig. 5. The coupled ac voltage across the pad1 and pad2 has a maximum voltage swing of 12 V and a frequency of 125 kHz in the smart-card application. The memorized data or number in the smart-card IC for identification is emitted out by the output pMOS (Mp2) in cooperation with the off-chip transformer. The diodes (Dp1, Dn1, Dp2, and Dn2) to form the four-diode bridge rectifying circuit are all realized by the polysilicon layer with p+/n−/n+-doping concentration. The device structure and layout top view of the polysilicon diodes realized in a CMOS process are shown in Fig. 6(a) and (b), respectively. The polysilicon layer has a thickness of 1500 Å in a 0.8-μm CMOS process. The layout spacing S of the lightly doped center region in polysilicon diode is originally drawn as 3 μm. The anode and cathode contacts of



(a)



(b)

Fig. 6. (a) Device structure and (b) layout top view of the p+/n−/n+ polysilicon diode realized in a 0.8-μm CMOS process.

the polysilicon diode have a clearance of 4 μm to the lightly doped center region.

To sustain a higher breakdown voltage (>12 V) of the polysilicon diode for smart-card application, an extra mask layer is added into the CMOS process flow to implant the n-region in the polysilicon diode. The p+(n+) region in the polysilicon diode is implanted with a doping concentration of 6E15 (3.5E15) cm^{-3}, which is the same as the drain/source implantation of pMOS (nMOS) in the CMOS process.

Due to the limitation of using the bulk p–n junction diodes to realize the bridge rectifying circuit, the on-chip ESD protection circuits for pad1 and pad2 are therefore also realized by the polysilicon diodes (Dp1, Dn1, Dp2, and Dn2) with an input series resistor (R1, R2) of 500 Ω. Each polysilicon diode has a total perimeter of 250 μm. The n-region has a width of 3 μm between the p+ and n+ regions of the polysilicon diode. A gate-coupled nMOS with a device dimension (W/L) of 300 μm/2 μm is also added into the chip across VDD and VSS power lines as the VDD-to-VSS clamp circuit for ESD protection. Such an nMOS has a breakdown voltage of ~16.5 V. However, the HBM ESD level of this smart-card IC fabricated in a 0.8-μm CMOS process is only around ~300 V, especially on the pad1 pin with the polysilicon diodes which are fully isolated from the p-substrate. With an ESD level below 500 V, the die of smart-card IC assembled into the smart card by the COB bonding is very susceptible to ESD events.

To improve the ESD level of the smart-card IC, a process split on increasing the doping concentration of the n-region in the polysilicon diode was investigated in the 0.8-μm CMOS process. The increased doping concentration of the n-region can lower the breakdown voltage of the polysilicon diode, therefore reducing the ESD-generated heat located on the polysilicon diode. The experimental results are summarized in Table I, where the HBM ESD level of pad1 pin in VSS(+) test mode only varies from 150 to 300 V when the n-doping concentration is increased from 3E13 to 9E13 cm^{-3}. Even in the VSS(−) ESD test mode, where the polysilicon diode is forward stressed, the HBM ESD level of pad1 pin only varies from 400 to 600 V. This is quite low for a diode with a perimeter of 250 μm in forward-biased condition. The high turn-on resistance of the polysilicon diode would limit the ESD current discharged through the polysilicon diode and cause ESD damage located on the internal devices.

TABLE I
HBM ESD LEVEL OF A SMART-CARD IC WITH THE ORIGINAL ESD PROTECTION DESIGN UNDER DIFFERENT n-DOPING CONCENTRATIONS

n- Doping Concentration (cm-3)	HBM ESD Level (Volt)			
	VDD(+)	VDD(-)	VSS(+)	VSS(-)
9E13	600	300	300	600
5E13	550	300	250	500
3E13	400	250	150	400

(Failure criterion : ILeakage > 1μA @ 5-V bias)

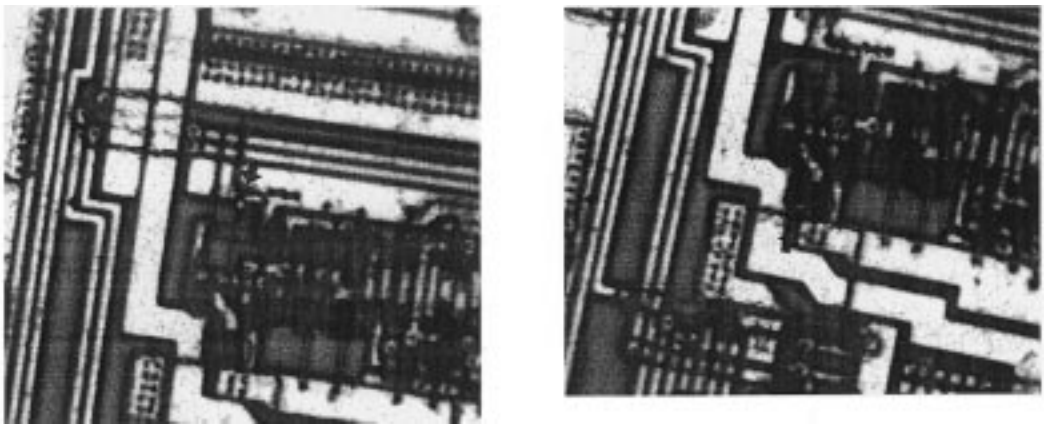
The photo-emission microscope (EMMI) pictures of failure locations on the smart-card IC after the VSS(+) and VDD(−) ESD stresses are shown in Fig. 7(a) and (b), respectively. In Fig. 7(a) [Fig. 7(b)], the ESD failure is located on the nMOS (pMOS) gate oxide of the first input stage that connected to the pad1 pin through the resistor R1, rather than on the polysilicon diodes Dp1 or Dn1. The pMOS and nMOS in the 0.8-μm CMOS process have a gate-oxide thickness of 250 Å. In this original design, the polysilicon diodes and the VDD-to-VSS ESD clamp circuit with gate-coupled nMOS cannot effectively protect the 250-Å gate oxide of the input circuits. The inefficiency of the original ESD protection design in Fig. 5 could be caused by the high trigger voltage (Vt1) of the VDD-to-VSS ESD clamp circuit, the parasitic resistance along the VDD/VSS power rails [3]–[5], or the high turn-on resistance of the polysilicon diodes.

Therefore, simply changing the n-doping concentration cannot effectively improve ESD level of the pad1 pin in such a smart-card IC. A more efficient ESD protection design should be developed to overcome this problem in the smart-card IC with polysilicon diodes.

III. NEW ON-CHIP ESD PROTECTION DESIGN

A. ESD Protection Circuit

To still apply the polysilicon diodes as the ESD protection devices at the pad1 pin, the concept of whole-chip ESD protection by using a more efficient VDD-to-VSS ESD clamp circuit to significantly improve ESD level of the I/O pin [6]–[10] is applied into this smart-card IC. The new proposed on-chip ESD protection circuit is shown in Fig. 8 with a novel VDD-to-VSS ESD clamp circuit [11], where the ESD protection circuit for the pad1 pin has two-stage protection diodes. The VDD-to-VSS ESD clamp circuit is formed by the nMOS Mn3 and its corresponding ESD-detection circuit. The gate of Mn3 is controlled by a stacked diode string, which is also realized by the polysil-



(a) (b)

Fig. 7. EMMI pictures showing the ESD failure location (indicated by the arrows) on the input circuits after (a) the VSS(+) test mode and (b) the VDD(−) test mode, HBM ESD stresses.

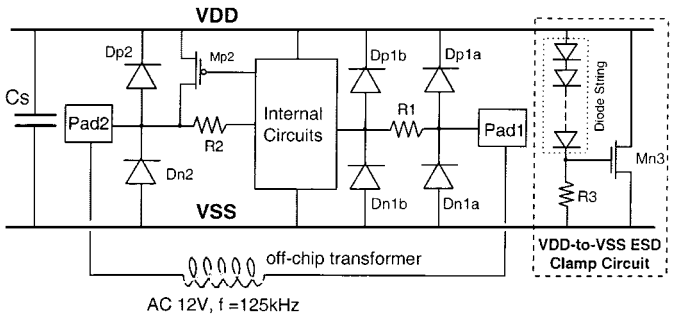


Fig. 8. New design of on-chip ESD protection circuit with a novel VDD-to-VSS ESD clamp circuit in the smart-card IC.

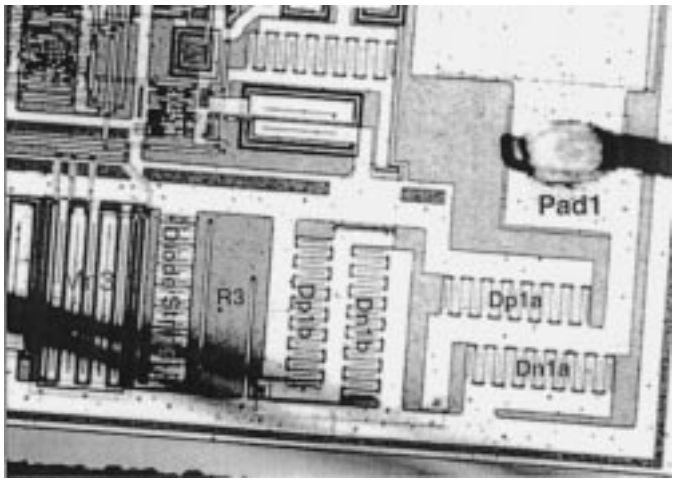


Fig. 9. Partial picture of a smart-card IC with the realization of ESD protection circuit on the pad1 pin and the VDD-to-VSS ESD clamp circuit.

icon diodes. If the stacked diodes were realized by the p+ diffusion in the n-well in CMOS process with a common p-substrate, there was a significant leakage current on the order of milliamperes from VDD to VSS due to the parasitic vertical BJT effect in CMOS process [12]–[14]. But, when the stacked diodes are realized by the polysilicon layer, the leakage current can be reduced below 1 μA under 5-V VDD bias. Therefore, the leakage current from VDD to VSS through the diode string and the resistor $R3$ of 10 kΩ in Fig. 8 can be designed smaller than 1 μA, if the diode number in the stacked diode string is large enough. The detailed calculation to find the suitable number n of stacked polysilicon diodes in the proposed VDD-to-VSS ESD clamp circuit has been derived in the Appendix.

For use in a smart-card IC with converted VDD power, eight polysilicon diodes are used in the diode string to control the gate voltage of Mn3, which has a device dimension (W/L) of 300 μm/2 μm in the practical IC. When the VDD is charged no more than 5 V, the Mn3 is kept off. But when the VDD is charged up greater than 5 V, the Mn3 is turned on to clamp the VDD voltage level. By changing the number of polysilicon diodes in the stacked diode string, the clamped voltage level on VDD can be adjusted for different applications.

With the novel VDD-to-VSS ESD clamp circuit, the ESD current under the VSS(+) ESD stress is discharged through the forward-biased Dp1a to VDD, and then discharged through the turned-on Mn3 to VSS, rather than the breakdown of polysilicon diode Dn1a. In the VDD(−) ESD stress, the negative ESD current is conducted to VSS through the forward-biased Dn1a, and then discharged to the grounded VDD through turned-on Mn3, without causing breakdown on polysilicon diode Dp1a. The second diode stage with Dp1b and Dn1b is used to further clamp overstress voltage across the gate oxide of the input circuits for safer ESD protection. A partial picture of a smart-card IC with realization of ESD protection circuit on the pad1 pin and the VDD-to-VSS ESD clamp circuit is shown in Fig. 9, where the polysilicon diodes of the pad1 pin are all drawn in the multiple-fingers style with a total perimeter of 300 μm for each diode.

B. Leakage Current in the VDD-to-VSS ESD Clamp Circuit

The leakage current from VDD to VSS in the new proposed VDD-to-VSS ESD clamp circuit can be calculated to find the suitable number n of diodes in the stacked diode string under different VDD voltage levels. The leakage current includes the subthreshold current of Mn3 and the diode string current. Because the diodes are all realized by the polysilicon layer, there is no parasitic vertical BJT in these diodes. The leakage current in such polysilicon diode strings is not increased by the parasitic vertical BJT effect [12]–[14]. This makes the proposed

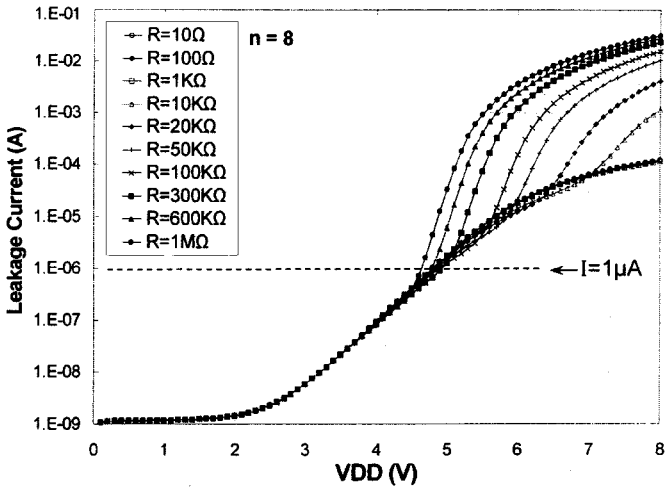


Fig. 10. HSPICE simulated leakage current of the proposed VDD-to-VSS ESD clamp circuit with eight diodes in the stacked diode string under different resistance of $R3$. (Y axis is drawn in log scale.)

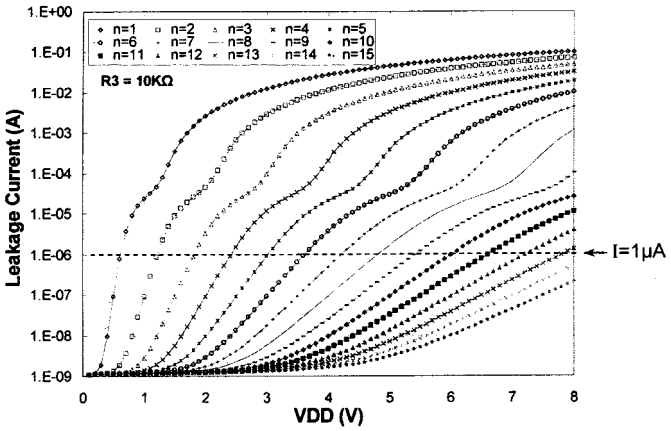


Fig. 11. HSPICE simulated leakage current of the proposed VDD-to-VSS ESD clamp circuit with a fixed $R3$ of 10 kΩ but different diode numbers (n) in the stacked diode string. (Y axis is drawn in log scale.)

VDD-to-VSS ESD clamp circuit to have a much lower leakage current in the IC normal operating condition.

When the diode string has eight stacked diodes ($n = 8$), the leakage current in the proposed VDD-to-VSS ESD clamp circuit under different resistance of $R3$ is simulated by HSPICE, and the results are shown in Fig. 10. When the $R3$ has a higher resistance, the leakage current is slightly increased due to the greater subthreshold current of Mn3, or significantly increased if Mn3 is turned on. By changing the number of diodes in the stacked diode string, the leakage current of the proposed VDD-to-VSS ESD clamp circuit can obviously be reduced. The HSPICE simulated results between the leakage current and VDD voltage level under different diode numbers n are shown in Fig. 11, where the $R3$ is kept at 10 kΩ. The y-axis of Fig. 11 is drawn in log scale to more clearly distinguish the leakage current under different diode numbers. As seen in Fig. 11, the increase of diode number n causes a smaller leakage current at a fixed VDD voltage level. For general IC specification, the leakage current should be smaller than 1 μA. The turn-on voltage $V_{\rm on}$ (defined at $I = 1$ μA) can be found from the I–V curves of Fig. 11. The relation between $V_{\rm on}$ and the diode number n under $R3$ of 10 or 100 kΩ is compared in Fig. 12. The increase of R3 resistance only causes a slight increase on the turn-on voltage $V_{\rm on}$, but the increase of diode number causes a significant increase on the turn-on voltage $V_{\rm on}$. The turn-on voltage $V_{\rm on}$ (defined as $I = 1$ μA) should be greater than VDD of the IC to meet the leakage current specification of smaller than 1 μA. The device dimension W/L of Mn3 in these calculations (Fig. 10–Fig. 12) is fixed at 300 μm/2 μm. The leakage current is also increased if the device dimension of Mn3 is increased. For the IC applications in different CMOS process, the suitable diode number in the stacked diode string can be found by the equations in the Appendix or HSPICE simulation.

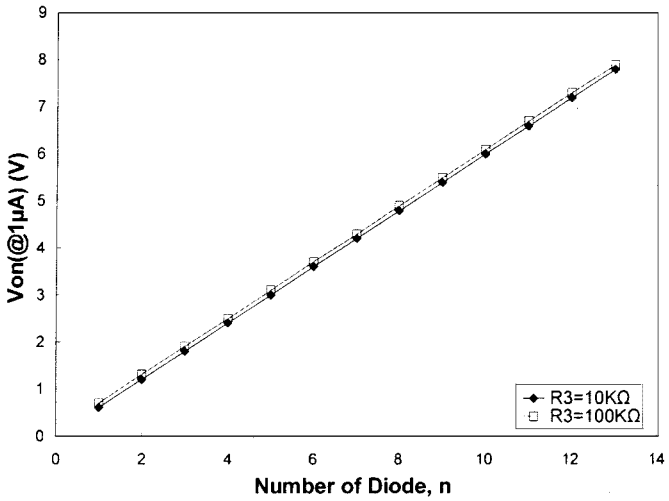


Fig. 12. Relation between $V_{\rm on}$ defined at $I = 1$ μA and the diode number (n) of the VDD-to-VSS ESD clamp circuit under $R3$ of 10 or 100 kΩ.

TABLE II
PROCESS SPLITS ON THE n-DOPING CONCENTRATION TO INVESTIGATE THE BREAKDOWN VOLTAGE AND THE FORWARD-BIASED CURRENT OF THE POLYSILICON DIODES

Split Case	N- Doping Concentration (cm-3)	Current @1-V forward-bias	Breakdown Voltage @1-μA current
# n1	7E13, 80KeV	3.4 μA	23 V
# n2	9E13, 80KeV	24.2 μA	15.6 V
# n3	2E14, 80KeV	807.8 μA	7.8 V
# n4	9E13, 50KeV	7.7 μA	16.5 V
# n5	2E14, 50KeV	706.2 μA	7.8 V

C. Process Splits

To choose a better doping concentration for the n-region in the polysilicon diode for smart-card application, a comprehensive process split with different implantation energy is investigated in Table II. If the n-region has a higher doping concentration or a higher implantation energy, the polysilicon diode has a lower breakdown voltage and a higher forward-biased current, which is better for ESD protection. But, because the transformer-coupled ac voltage could have a maximum voltage swing of 12 V, the breakdown voltage of polysilicon diode is selected to be

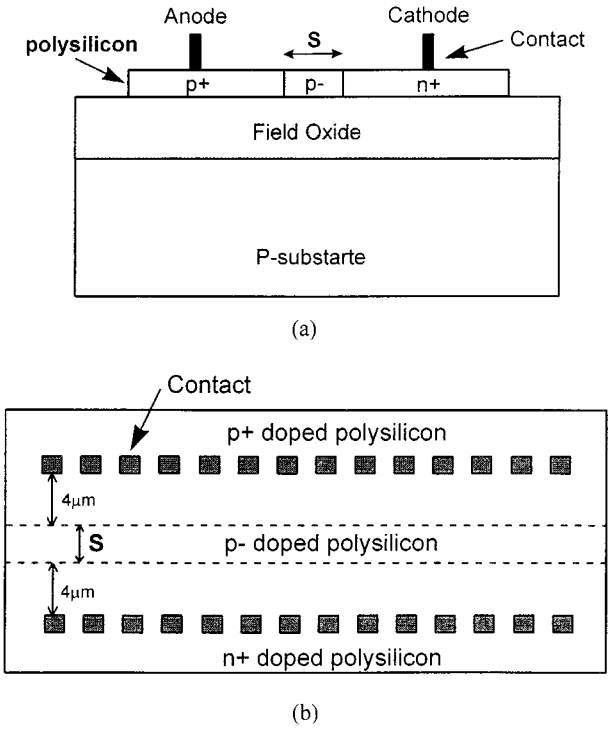


Fig. 13. (a) Device structure and (b) layout top view of the p+/p−/n+ polysilicon diode realized in a CMOS process.

TABLE III
PROCESS SPLITS ON THE p-DOPING CONCENTRATION TO INVESTIGATE THE BREAKDOWN VOLTAGE AND THE FORWARD-BIASED CURRENT OF THE POLYSILICON DIODES

Split Case	P- Doping Concentration (cm-3)	Current @1-V forward-bias	Breakdown Voltage @1-μA current
# p1	1E13, 80KeV	8.4 μA	21.5 V
# p2	5E13, 80KeV	252 μA	12.4 V
# p3	9E13, 80KeV	928 μA	9.3 V

greater than 12 V for safe application. Therefore, the split case of #n2 in Table II is suitable for use in this smart-card IC.

The polysilicon diode can also be realized with a p-type lightly doping region, as shown in Fig. 13(a) and (b). The process split is also used to investigate the characteristics of such a p+/p−/n+ polysilicon diode. The experimental results are listed in Table III, where the polysilicon diode has a layout spacing (the p-doping region) S of 3 μm. Due to the concern for the transformer-coupled maximum ac voltage swing of 12 V, the split case of #p2 in Table III is suitable for use in this smart-card IC.

IV. DEPENDANCE OF LAYOUT PARAMETERS ON It2 OF POLYSILICON DIODES

Although the process splits can find the optimized doping concentration for the lightly doped center region in the polysilicon diode, the ESD performance of the polysilicon diode can be further improved by suitably choosing its layout parameters. Under a fixed process split condition with the n-(of 1.5E14 cm^{-3}) doped center region, many polysilicon diodes

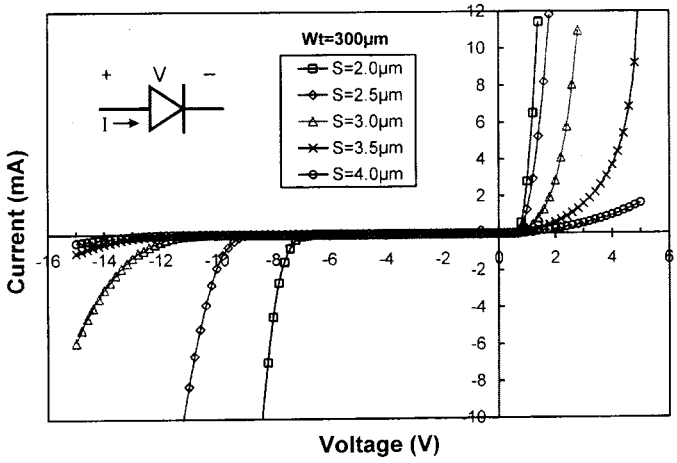


Fig. 14. Measured I–V curves of the p+/n−/n+ polysilicon diodes with a fixed Wt of 300 μm but different S spacings in a CMOS process.

are fabricated in a test wafer with different layout spacings S of the lightly doped center region and different total perimeters Wt. A polysilicon diode with a large device dimension is drawn in the multiple-fingers layout style, in which every finger has a layout length of 30 μm. For a polysilicon diode with a total perimeter Wt of 300 μm, there are ten fingers drawn in parallel in the device layout. The measured I–V curves of the polysilicon diodes with a fixed Wt of 300 μm but different S spacings are shown in Fig. 14. The polysilicon diode with a narrower spacing S has a smaller cut-in voltage in the forward-bias condition, and a smaller (in magnitude) breakdown voltage in the reverse-biased condition.

To further investigate ESD performance of the fabricated polysilicon diodes, the transmission-line-pulse (TLP) generator (according to the prior art of [15]) has been successfully set up with a pulse width of 100 ns [16] and used to measure It2 of the polysilicon diodes. The TLP-measured I–V curves of the polysilicon diodes with a fixed Wt of 300 μm but different S spacings are shown in Fig. 15(a) and (b) in the forward- and reverse-biased conditions, respectively. The dependence of It2 on the layout parameter S in both the forward- and reverse-biased conditions is summarized in Fig. 16. The TLP-measured I–V curves of the polysilicon diodes with a fixed spacing S of 3 μm but different total perimeters Wt are shown in Fig. 17(a) and (b) in the forward- and reverse-biased conditions, respectively. The dependence of It2 on the total perimeter Wt of the polysilicon diode in both forward- and reverse-biased conditions is compared in Fig. 18. A polysilicon diode with a wider perimeter Wt also has a larger volume for heat dissipation, therefore it has a higher It2 value.

As seen in Fig. 16 and Fig. 18, the polysilicon diode in forward-biased condition has a much higher It2 value than it does in the reverse-biased condition. This is due to the different power ($= I_{\rm ESD} \times V_{\rm op}$, the product of ESD current and the operating voltage of device) generated by the ESD current on the polysilicon diode in the forward- and reverse-biased conditions. The diode in the reverse-biased condition has a higher operating voltage $V_{\rm op}$ across itself than in the forward-biased condition. Therefore, the ESD current $I_{\rm ESD}$ generates more

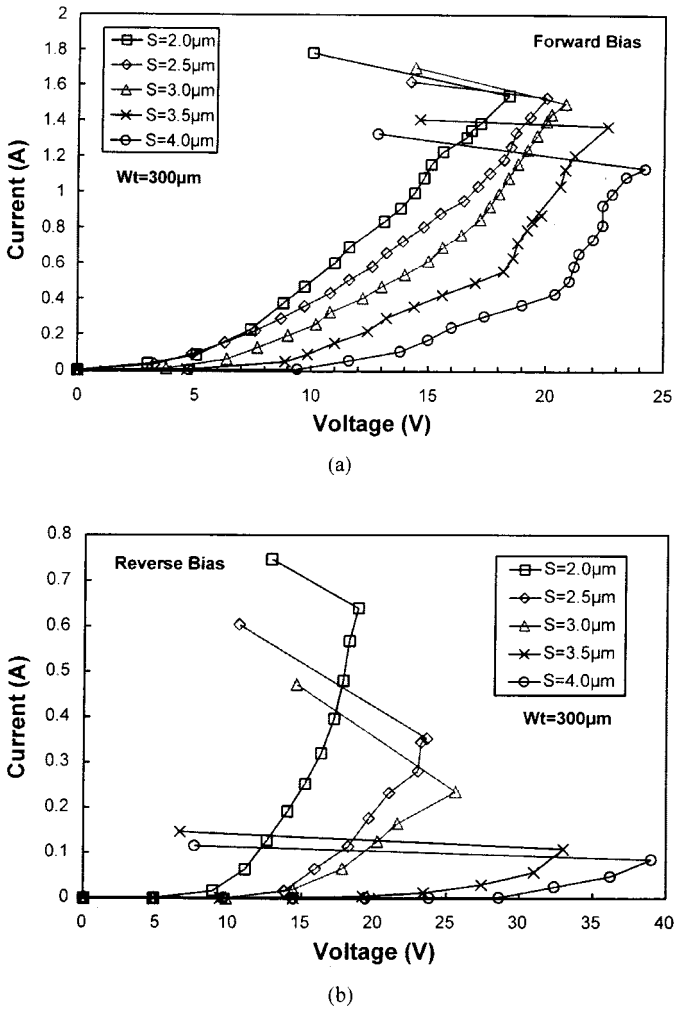


Fig. 15. TLP-measured I–V curves of the polysilicon diodes in (a) the forward-biased condition and (b) the reverse-biased condition, with a fixed Wt of 300 μm but different S spacings.

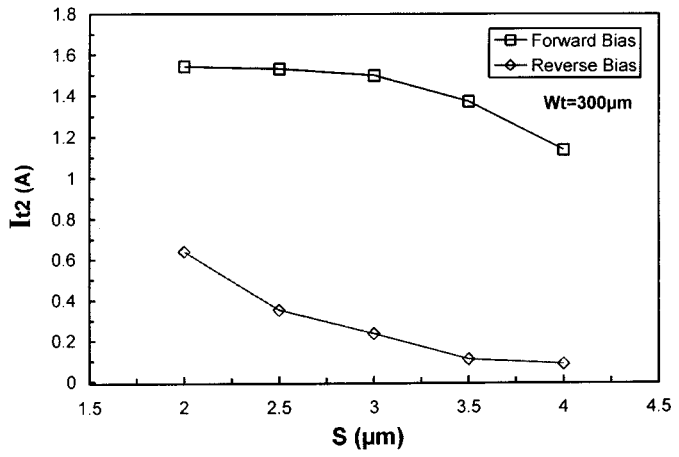


Fig. 16. Dependence of the TLP-measured It2 on the layout parameter S of the polysilicon diodes in both the forward- and reverse-biased conditions.

heat on the polysilicon diode in the reverse-biased condition to cause a lower It2.

When the spacing S increases in the polysilicon diode, the It2 is also decreased, even if the diode is stressed in the forward-biased condition. In the forward-biased condition,

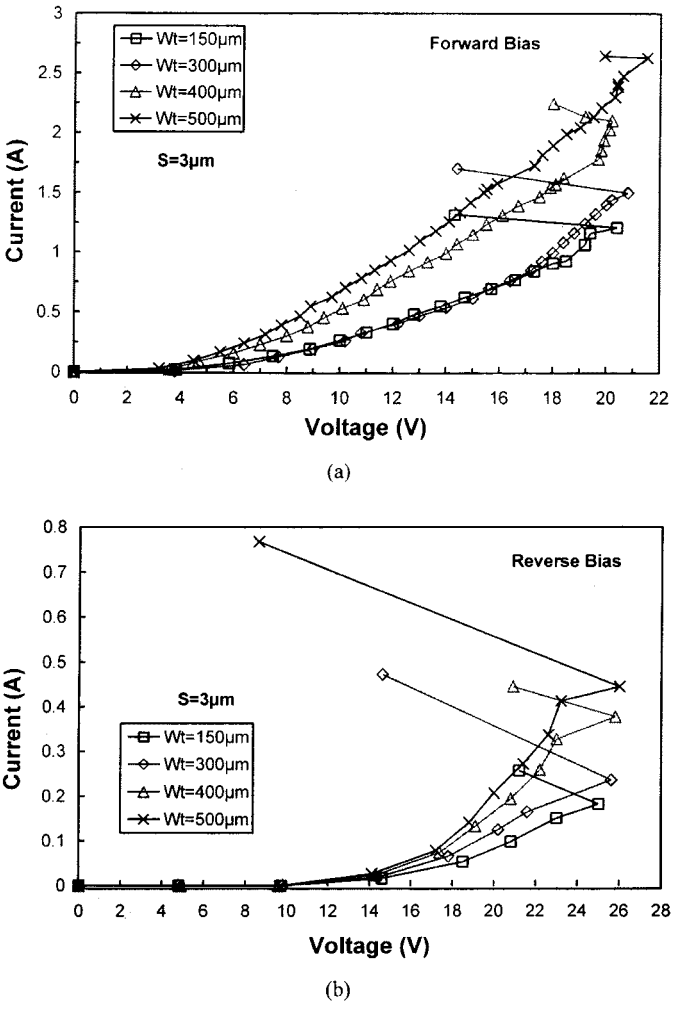


Fig. 17. TLP-measured I–V curves of the polysilicon diodes in (a) the forward-biased condition and (b) the reverse-biased condition, with a fixed spacing S of 3 μm but different total perimeters Wt.

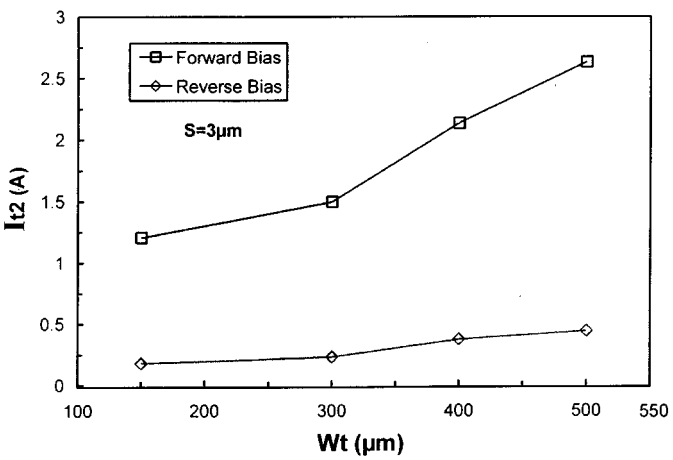


Fig. 18. Dependence of the TLP-measured It2 on the layout parameter Wt (total perimeter) of the polysilicon diodes in both the forward- and reverse-biased conditions.

the power generated by ESD current on the polysilicon diode is mainly decided by the turn-on resistance of the diodes. A polysilicon diode with a smaller layout spacing S has a lower turn-on (breakdown) resistance, therefore it has a relatively

TABLE IV
HBM ESD LEVEL OF THE SMART-CARD IC WITH THE NEW PROPOSED ESD PROTECTION DESIGN

Polysilicon-Diode Doping Concentration (cm-3)	HBM ESD Level (Volt)			
	VDD(+)	VDD(-)	VSS(+)	VSS(-)
N-, 9E13	> 4kV	> 4kV	3kV	> 4kV
P-, 5E13	> 4kV	3kV	3.5kV	> 4kV

(Failure criterion : $I_{Leakage}$ > 1μA @ 5-V bias)

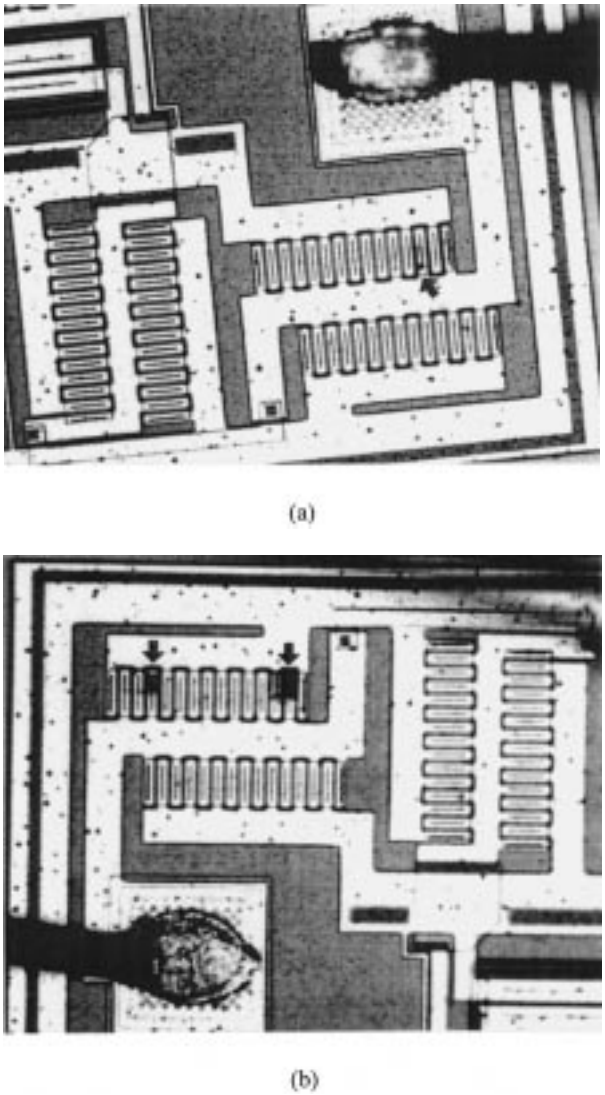
higher It2 in the forward- (reverse-) biased condition. With well understood and detailed investigation on It2 of the polysilicon diodes under different bias conditions and layout parameters, ESD robustness of the smart-card IC can be effectively improved by arranging the polysilicon diodes to discharge ESD current in its forward-biased condition. This can be achieved by designing a more efficient VDD-to-VSS ESD clamp circuit into the chip, as that shown in Fig. 8. The efficient VDD-to-VSS ESD clamp circuit should have a fast turn-on speed and a low turn-on voltage to discharge the ESD current from VDD to VSS.

V. EXPERIMENTAL RESULTS AND DISCUSSION

A. ESD Test and Failure Analysis

The smart-card ICs with the polysilicon diodes and the new proposed ESD protection design in Fig. 8 have been fabricated. The polysilicon diodes realized with the n- or p-doped center regions can perform the desired circuit function for smart-card application. The HBM ESD test results of this new ESD protection design with the polysilicon diodes of n- or p-doped center regions are listed in Table IV. While the polysilicon diodes are realized by the n- (p-) doped center region with a doping concentration of 9E13 (5E13) cm^{-3} and a total perimeter of $Wt = 300$ μm (under the spacing of $S = 3$ μm), the HBM ESD-sustained level of pad1 pin in the VSS(+) ESD test mode is improved to 3 kV (3.5 kV). In the VDD(−) ESD test mode, the HBM ESD-sustained level is improved to >4 kV (3 kV). In both the VSS(−) and VDD(+) ESD test modes, the smart-card IC with polysilicon diodes can sustain the ESD-stress voltage of greater than 4 kV. The HBM ESD level of this smart-card IC under the direct VDD-to-VSS ESD stress is also greater than 4 kV.

A picture showing the failure location on the smart-card IC with the p-doped polysilicon diodes after the pad1 pin is zapped with a 4-kV VSS(+) HBM ESD stress is shown in Fig. 19(a), where the ESD failure is located on the polysilicon diode Dp1a, rather than on the Dn1a or the gate oxide of input circuits. In Fig. 19(b), it shows that the ESD failure is located on the polysilicon diode Dn1a, rather than the diode Dp1a, after the pad1 pin is zapped with a 4-kV VDD(−) HBM ESD stress. From the ESD failure analysis, it has confirmed that the ESD current is actually discharged through the polysilicon diodes in the forward-biased conditions. This is achieved by adding the turn-on efficient VDD-to-VSS ESD clamp circuit into the chip, as well as by reducing the parasitic resistance along the power rails, as shown in Fig. 8. The ESD test results have successfully verified the proposed ESD protection design in the smart-card IC by using the polysilicon diodes as the ESD clamp devices.



(a)

(b)

Fig. 19. Pictures showing the ESD failure location (indicated by the arrows) on the smart-card IC with the p-doped polysilicon diodes after the pad1 pin is zapped with a 4-kV HBM ESD stress in (a) the VSS(+) and (b) the VDD(−) ESD test conditions.

The smart-card IC with n-doped polysilicon diodes has also been verified by the charged-device-model (CDM) ESD test in a socketed CDM tester. The maximum CDM ESD-sustained voltage level of the fabricated smart-card IC is 750 and 600 V in the positive and negative CDM stresses conditions, respectively. A picture indicating the ESD failure location on the smart-card IC with n-doped polysilicon diodes after a negative 700-V CDM ESD stress is shown in Fig. 20, where the ESD failure is located on the polysilicon diode Dn1a, not on the gate oxide of the first input stage. To sustain a higher CDM ESD level, the layout spacing S of the lightly doped center region has to be reduced to lower the breakdown voltage and to decrease the ESD-generated heat on the polysilicon diodes. The polysilicon diode with a reduced spacing S also has a smaller turn-on resistance to quickly discharge the ESD current. But the minimum breakdown voltage of the polysilicon diode in this smart-card application is limited to 12 V, due to the coupled maximum ac voltage. This requirement can be further achieved by arranging the polysilicon diodes into the multistage configuration [11],

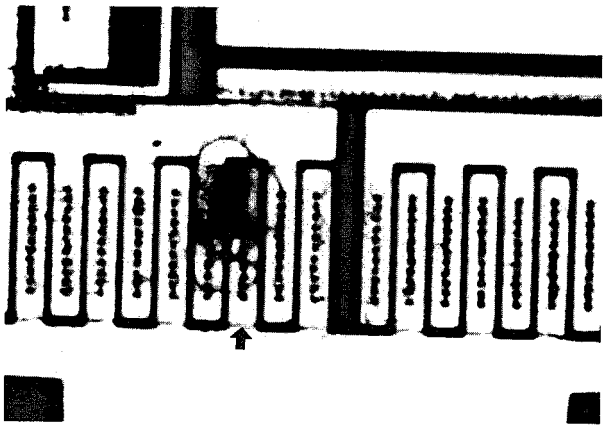


Fig. 20. Picture showing the ESD failure location (indicated by the arrow) on the smart-card IC with the n-doped polysilicon diodes after a negative 700-V CDM ESD stress.

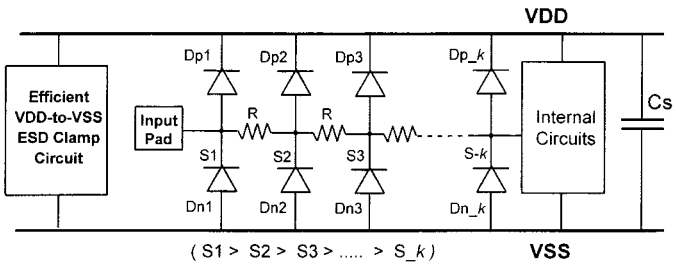


Fig. 21. Alternative input ESD protection design with the polysilicon diodes in a multistage configuration to achieve better ESD protection.

as shown in Fig. 21. The polysilicon diode in every stage has different layout spacing S. The polysilicon diode close to the first input stage of the internal circuits has a narrower spacing S, but the polysilicon diode close to the bond pad has a wider spacing S. The resistance R between every stage can be further reduced to improve CDM ESD level but without degrading its HBM ESD level.

B. Turn-on Verification

The I–V curve of the new proposed VDD-to-VSS ESD clamp circuit with eight stacked n-doped polysilicon diodes is measured in Fig. 22. When the applied voltage across VDD and VSS is increased higher to bias the gate of Mn3 greater than its threshold voltage, the nMOS Mn3 is turned on to conduct current from VDD to VSS. So, the measured I–V curve in Fig. 22 has a sharp current increase when the applied voltage is greater than 5 V.

In order to investigate the turn-on efficiency of the polysilicon diodes at pad1 (Fig. 8) with the help of the new proposed VDD-to-VSS ESD clamp circuit, a 0–8-V voltage pulse is directly applied to pad1 with the VSS pin relatively grounded and the VDD pin floating. The original 0–8-V voltage pulse is generated from a pulse generator with a pulse width of 4 μs and a rise time of $\sim$10 ns, as the dashed line shown in Fig. 23. When such a voltage pulse is applied to pad1, it is clamped to the voltage level shown in Fig. 23. Because the polysilicon diodes of pad1 have a breakdown voltage around 12 V, the applied 8-V voltage does not cause any breakdown on the polysilicon diodes of pad1.

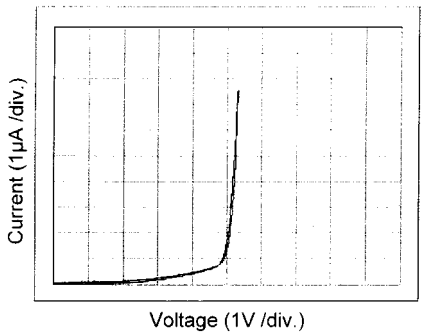


Fig. 22. Measured I–V curve from VDD to VSS of the new proposed VDD-to-VSS ESD clamp circuit with eight stacked n-doped polysilicon diodes.

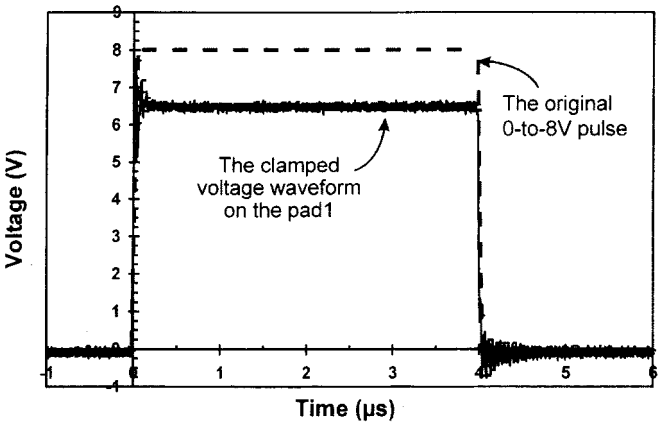


Fig. 23. Measured voltage waveform at pad1 when a 0–8-V voltage pulse is applied to the pad1 with VSS grounded.

But, the 0–8-V voltage pulse is actually clamped to about 6.5 V in Fig. 23. This is due to the turn-on of the VDD-to-VSS ESD clamp circuit. Therefore, the overstress voltage on pad1 is discharged from pad1 to VDD through the forward-biased polysilicon diode, and then discharged to VSS through the turned-on VDD-to-VSS ESD clamp circuit. This has successfully verified the effectiveness of the new proposed VDD-to-VSS ESD clamp circuit with stacked polysilicon diodes to significantly improve ESD level of the I/O pad.

VI. Conclusion

The device characteristics of the polysilicon diodes in CMOS process have been experimentally evaluated by process splits with different doping concentrations. The It2 of the polysilicon diodes under forward- and reverse-bias conditions and different layout parameters has been clearly investigated. The HBM ESD level of the smart-card IC with the polysilicon diodes as ESD protection devices has been successfully improved up to 3 kV in cooperation with a turn-on efficient VDD-to-VSS ESD clamp circuit. By adjusting the number of the stack diodes in the ESD detection circuit, the turn-on efficient VDD-to-VSS ESD clamp circuit can be applied in the IC with different VDD voltage levels. Such ESD-improved smart-card ICs have been in mass production with a large sale volume to offer smart-card manufacturability without any ESD problem.

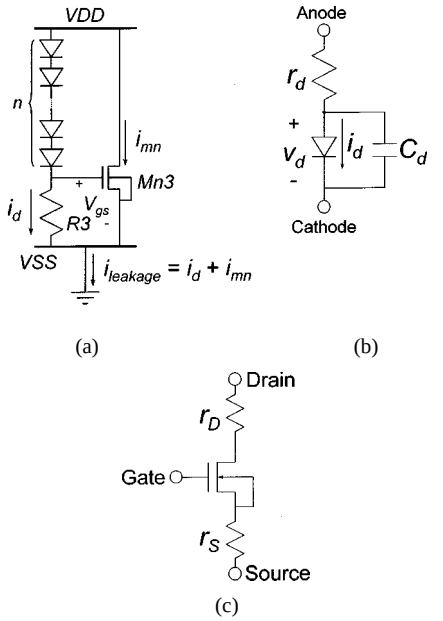


Fig. 24. (a) ESD clamp circuit with stacked polysilicon diodes, and the equivalent circuits of (b) a diode, and (c) an nMOS, for model calculation.

APPENDIX

In Fig. 24(a), a diode string of polysilicon diodes is used to trigger the gate of nMOS. The equivalent circuit of each forward-bias diode is shown in Fig. 24(b), where the series resistor r_d is the turn-on resistance of a polysilicon diode. The equivalent circuit of an nMOS is shown in Fig. 24(c) with the consideration of drain and source resistance, $r_{\rm D}$ and $r_{\rm S}$, respectively. The current of each diode is

$$i_{\rm d} = I_{\rm S}\left(e^{v_d/\eta v_{\rm T}} - 1\right). \tag{A.1}$$

The voltage drop on each diode ($v_{\rm d}$) is the same to each other. $I_{\rm S}$ is the saturation current, $v_{\rm T}$ is the thermal voltage, and the factor η generally has a value between 1 and 2. The total voltage drop $V_{\rm drop}$ across the stacked diodes and the resistor $R3$ (connected between the gate of nMOS and VSS) can be expressed as

$$\begin{aligned} V_{\rm drop} &= i_{\rm d}\cdot R3 + n\cdot(i_{\rm d}\cdot r_d + v_d) \\ &= i_{\rm d}\left(R3 + n\cdot r_d\right) + n\eta v_{\rm T}\,\ln\left(1+\frac{i_{\rm d}}{I_{\rm S}}\right) \end{aligned} \tag{A.2}$$

where n is the stacked number of diodes. This equation can be rewritten to find the n as function of the gate voltage v_{gs} of nMOS as

$$n = \frac{V_{\rm drop} - v_{gs}}{\eta v_{\rm T}\,\ln\left(1+\dfrac{v_{gs}}{R3\cdot I_S}\right) + \dfrac{r_d}{R3}\cdot v_{gs}} \tag{A.3}$$

where

$$v_{gs} = i_{\rm d} R3. \tag{A.4}$$

From the circuit connection of Fig. 8, the $V_{\rm drop}$ equals VDD. So, the number n of stacked polysilicon diodes can be adjusted to reduce the total leakage current, when the IC is operating in normal condition. To limit the leakage current through nMOS, the gate voltage of nMOS has to be less than its threshold voltage $V_{\rm th}$. The leakage current of nMOS operated in the subthreshold region ($v_{gs} < V_{\rm th}$) is [17]

$$\begin{aligned} i_{mn} = &\frac{1}{2}\mu_n C_{\rm OX} a v_{\rm T}^2 \frac{W_{\rm eff}}{L_{\rm eff}}\left(\frac{n_i}{N_A}\right)^2 \\ &\cdot\left(1-\exp\left(-\frac{\rm VDD - i_{mn}\cdot(r_D+r_S)}{v_{\rm T}}\right)\right) \\ &\cdot e^{\psi_s/v_{\rm T}}\left(\frac{\psi_s}{v_{\rm T}}\right)^{-1/2}. \end{aligned} \tag{A.5}$$

Therefore, the total leakage current of this proposed power-rail ESD clamp circuit can be expressed as

$$i_{\rm leakage} = i_{\rm d} + i_{mn} \tag{A.6}$$

where the leakage current through stacked polysilicon diodes $i_{\rm d}$ can be obtained from (A.4), and the leakage current through the nMOS (i_{mn}) can be obtained from (A.5). Finally, the total leakage current ($i_{\rm leakage}$) can be further expressed as a function of v_{gs}.

$$i_{\rm leakage} = \frac{v_{gs}}{R3} + K\cdot\sqrt{\frac{v_{\rm T}}{\psi_s(v_{gs})}}\cdot\exp\left(\frac{\psi_s(v_{gs})}{v_{\rm T}}\right) \tag{A.7}$$

where

$$\psi_s(v_{gs}) = (v_{gs} - V_{\rm FB}) - \frac{1}{2}\xi\left\{\sqrt{1+\frac{4}{\xi}(v_{gs}-V_{\rm FB}-v_{\rm T})}-1\right\}. \tag{A.8}$$

In these equations, the parameters of K and ξ are constant factors for a CMOS process, and they are defined as

$$\begin{aligned} K \equiv &\frac{1}{2}\mu_n C_{\rm OX} a v_{\rm T}^2 \frac{W_{\rm eff}}{L_{\rm eff}}\left(\frac{n_i}{N_A}\right)^2 \\ &\cdot\left(1-\exp\left(-\frac{\rm VDD - i_{mn}\cdot(r_D+r_S)}{v_{\rm T}}\right)\right) \end{aligned} \tag{A.9}$$

and

$$\xi \equiv a^2 v_{\rm T}. \tag{A.10}$$

For a given CMOS process, the value of K and ξ can be determined from process parameters.

From (A.3) and (A.7), the relation between n and $i_{\rm leakage}$ can be calculated with the specified factors of VDD, $R3$, diode parameters, and nMOS dimension. First, some suitable series resistances $R3$ are temporarily chosen to calculate the relation between v_{gs} and n from (A.3). The condition of choosing $R3$ is considered to keep the gate voltage v_{gs} of nMOS smaller than its threshold voltage $V_{\rm th}$ in the normal circuit operating condition. If nMOS is turned off, the leakage current will mainly appear through the diode string and resistor $R3$. For example, when v_{gs} is smaller than 0.01 V, $R3 = 10\ {\rm k}\Omega$ can be chosen to meet the condition of $i_{\rm leakage} < 1\ \mu$A. Secondly, the relation between gate voltage v_{gs} of nMOS and the total leakage current $i_{\rm leakage}$ must be calculated to determine the exact value of n. From (A.2) and (A.4), the relation between v_{gs}, $i_{\rm d}$, and $R3$ can be calculated. Using these values of v_{gs}, the total leakage current $i_{\rm leakage}$ can be calculated from (A.7).

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