High Reliability Polyoxide Fabricated by Using TEOS Oxide Deposited on Disilane Polysilicon Film

Jam Wem Lee, Chung-Len Lee, *Senior Member, IEEE*, Tan Fu Lei, and Chao Sung Lai

***Abstract*—This paper reports the TEOS oxide deposited on the polysilicon film which was prepared by using the disilane chemical vapor deposition. Compared to the thermally grown oxide or TEOS (tetra-ethy1-ortho-silicate) oxide deposited on the conventional silane polysilicon film, it had symmetrical J–E characteristics that had lower leakage currents but much higher breakdown field, a lower electron trapping rate, and a much larger charge to breakdown. These good properties are attributed to the smoother surface of the deposited disilane poly-I film and the more incorporation of nitrogen during the rapid thermal annealing (RTA) in N_2O ambient. It is suitable to be as the inter-polyoxide of the electrically-erasable programmable read only memory (EEPROM).**

I. Introduction

N ORDER to have good data retention characteristics for the deep submicron electrically-erasable programmable read only memory (EEPROM), a thin polyoxide with a low leakage current, a high breakdown field (E_{bd}), a large charge to breakdown (Q_{bd}) and a low electron trapping rate is required [1]–[4]. Recently, TEOS vapor deposited polyoxide with rapid-thermal-annealing (RTA) in N_2O has been reported to have a higher reliability due to its smoother interface after oxidation [5], [6]. The quality of the TEOS (tetra-ethy1-ortho-silicate) polyoxide is strongly related to the surface roughness and the doping concentration of polyI. Unfortunately, for the conventional polysilicon film, the surface roughness increases as the doping concentration of polyI decreases [7], reducing the advantage obtained by the TEOS polyoxide.

Disilane polysilicon film was widely used in fabrication of the low-temperature thin-film transistor (TFT) for its lower deposition temperature and larger grain [8], [9]. It was also used as HSG (hemispherical grain) poly-Si films in dynamically random accessible memories (DRAM's) for its wide transition temperature [10]. It has a much smoother surface in the low doping concentration regime. However, little study was done on growing oxides on it, especially, on depositing TEOS oxide on it. This paper reports, for the first time, the results on investigation on low pressure chemical vapor deposition (LPCVD) TEOS oxide deposited on the disilane polysilicon followed with RTA in N_2O. It is found that the fabricated polyoxide has a very high Q_{bd}, a low electron trapping rate, and a high E_{bd}. The polyoxide, when used in EEPROM applications, can improve performance and reliability of the EEPROM device.

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J. W. Lee, C.-L. Lee, and T. F. Lei are with the Department of Electronic Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.

C. S. Lai is with the Department of Electronic Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C. and also with the Department of Electronic Engineering, Chang Gung University, Tao-Yuan, Taiwan, R.O.C.

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TABLE I
DETAILED PROCESS STEPS FOR EACH SAMPLE

sample	Silane Poly-I	Disilane Poly-I	Thermal O_2	Thermal N_2O	TEOS	TEOS + RT N_2O	TEOS + RT O_2	TEOS + RT N_2
D-TH-O2		▲	▲					
D-TH-N2O		▲		▲				
D-T		▲			▲			
D-T-RT-N2O		▲				▲		
D-T-RT-O2		▲					▲	
D-T-RT-N2		▲						▲
S-TH-N2O	▲			▲				
S-T-RT-N2O	▲					▲		

II. Experiments

In this study, n^+-polysilicon/polyoxide/n^+-polysilicon capacitors were fabricated and used in the measurement. At first, p-type wafers were thermally oxidized in dry O_2 at 950 °C to have a 100 Å oxide. Then a 200 nm disilane polysilicon film (poly-I) was deposited at 460 °C. The poly-I film was then phosphorous-implanted at an energy of 30 keV of a dose of 5×10^{15} cm^{-2}. After rapid-thermal (RT) annealed at 950 °C for 30 s in an N_2 ambient to obtain a sheet resistance of 70 Ω/cm^2 for poly-I, the wafers were then deposited with a TEOS oxide of a thickness of 130 Å at 700 °C. The oxide was then RT annealed in an N_2O ambient at 950 °C for 30 s. For comparison, the same oxide but RT annealed in O_2 or N_2 ambient at 950 °C for 30 s were also prepared. A second silane polysilicon (poly-II) of a thickness of 300 nm was then deposited again. The poly-II was doped by $POCl_3$ and driven-in at 850 °C for 1 h in an N_2 ambient to obtain a sheet resistance of 40 Ω/cm^2. It was then patterned and grown a 100 nm passivation oxide. After contact hole opening, Al film was deposited, patterned, and sintered at 350 °C for 40 min in an N_2 ambient to be gates and contacts of the capacitors. In the above, also for comparison, similar capacitors but with their poly-I grown with silane at 620 °C, of a sheet resistance of 140 Ω/cm^2, were prepared. Also, for comparison, similar capacitors but their oxides grown in O_2 and N_2O at 850 °C by the conventional thermal oxidation method were prepared. The process steps for each sample are compiled in Table I.

The thickness (equivalent oxide thickness E_{ox}) of the oxide was measured by CV measurement and verified by TEM, and Q_{bds} and E_{bds} were measured by an HP4145b semiconductor analyzer.

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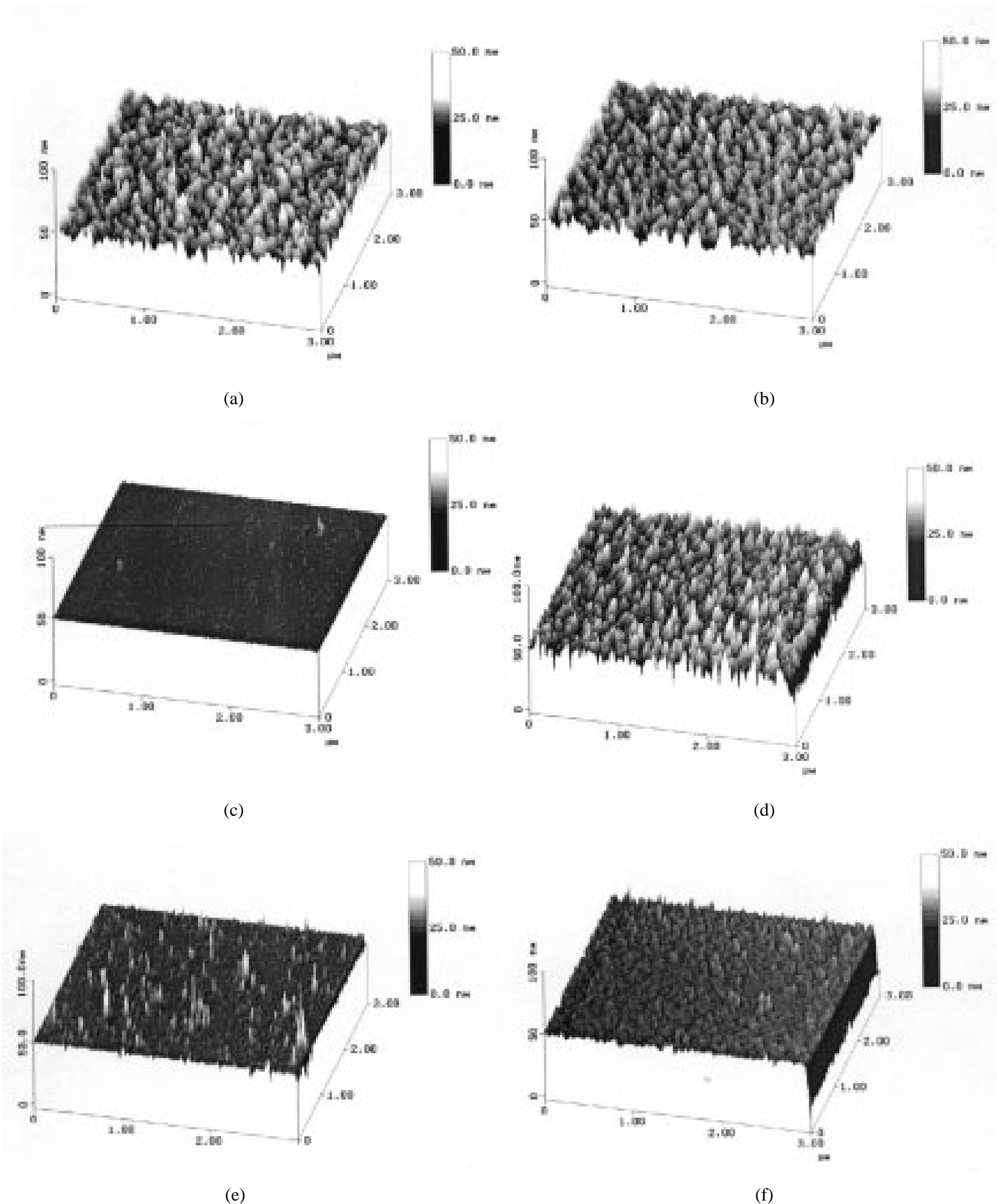


Fig. 1. AFM images of polyI surface of (a) D-TH-O_2; (b) D-TH-N_2O; (c) D-T-RT-N_2O; and (d) S-T-RT-N_2O, (e) D-T, and (f) D-T-RT-O_2 samples with their poly-II and polyoxide removed. The surface roughness is 44 Å, 31 Å, 3 Å, 49 Å, 12 Å, and 34 Å, respectively.

III. Results and Discussion

Fig. 1 shows the atomic force microscope (AFM) images of the poly-I surfaces of the following samples: (a) D-TH-O_2: the O_2 thermal oxide grown on the disilane poly-I; (b) D-TH-N_2O: the N_2O thermal oxide grown on the disilane poly-I; (c) D-T-RT-N_2O: the TEOS oxide deposited on the disilane poly-I with RTN_2O annealing; (d) S-T-RT-N_2O: the TEOS oxide deposited on the silane poly-I with RTN_2O annealing; (e) D-T: the TEOS oxide deposited on the disilane poly-I; and (f) D-T-RT-O_2: the TEOS oxide deposited on the disilane poly-I with RTO_2 annealing, respectively. In the above, all images are the surface images of poly-Is of the capacitors with their poly-II's and polyoxides removed. The roughness obtained from the AFM measurement for each sample are D-TH-O_2: 44 Å, D-TH-N_2O: 31 Å, D-T-RT-N_2O: 3 Å, S-T-RT-N_2O: 49 Å, D-T: 12 Å, and D-T-RT-O_2: 34 Å, respectively. From these pictures and data, it can be found that

1) the TEOS with the RTN_2O sample had the smoothest surface;
2) the disilane samples had smoother surface than that of the silane samples;

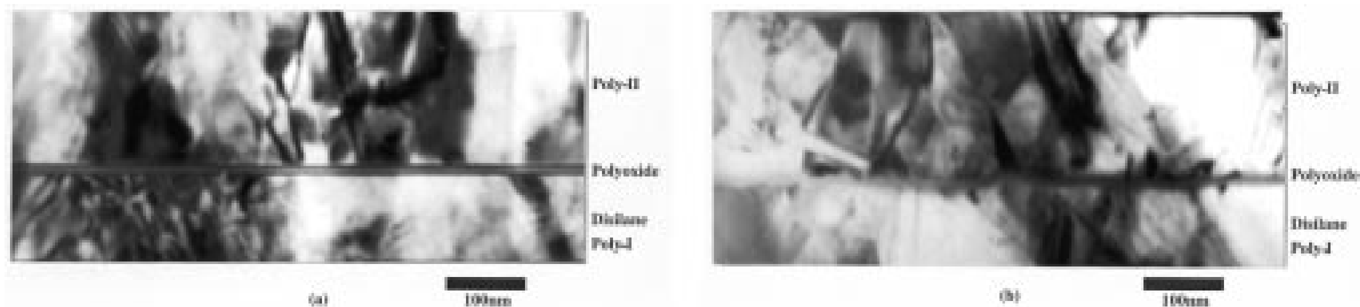


Fig. 2. TEM images of the (a) D-T-RT-N_2O and (b) S-T-RT-N_2O sample. The poly-I thickness is 2000 Å, polyoxide thickness is 150 Å.

3) the polyoxides treated in N_2O ambient improved the poly-I/oxide interface roughness.

In addition, for disilane samples, the thermally grown polyoxide had a rougher interface than that of the TEOS oxide. This indicates that thermal oxidation enhanced interface roughness. Also, the oxides grown or annealed in the N_2O ambient had a smoother interface than those treated in the O_2 ambient. This was probably caused by the fact that N_2O oxidation or annealing provided nitrogen which passivated grain boundaries of the deposited poly-I layer and reduced the grain boundary enhancement effect [1].

Fig. 2 shows the cross section TEM images of the D-T-RT-N_2O and S-T-RT-N_2O samples. These pictures show that the D-T-RT-N_2O sample had a smoother interface than that of the S-T-RT-N_2O sample. Two samples had a similar grain size on the poly-I film. However, it is noticed that, for the D-T-RT-N_2O sample, both its poysilicon-II/oxide/polysilicon-I interfaces had similar smoothness. In addition, from the TEM picture of the D-T-RT-N_2O sample, the oxide thickness can be estimated to be 150 Å, which is the same as the value derived from the CV characteristic of the sample. The dielectric constant of the polyoxide was 3.9.

Fig. 3 shows the (a) positive and (b) negative J–E characteristics of the six samples. The D-T-RT-N_2O sample, i.e., the TEOS oxide deposited on the disilane polysilicon film with RTN_2O annealing, had the lowest leakage current and the highest breakdown field. This could be attributed to the much smoother poly-I of this sample. In the figure, the D-T sample, i.e., the D-T-RT-N_2O sample without the RT N_2O annealing, had a poorer characteristics than that of the D-T-RT-N_2O sample, although it had a relatively smooth poly-I/oxide interface. Hence, the RT annealing in N_2O is an important step in improving the quality of the oxide. It annealed the deposited oxide, created an additional 20 Å thermal oxide at the poly-I/oxide interface, and introduced nitrogen into the oxide. The latter will be addressed further next by the support of SIMS data. In addition, it is seen that besides the D-T-RT-N_2O sample, all other samples had asymmetrical J–E characteristics. That the D-T-RT-N_2O sample had the symmetrical J–E characteristics is believed due to the fact that it had a symmetrical smoothness on its both polysilicon-II/oxide and oxide/polysilicon-I interfaces, as revealed by the previous TEM pictures.

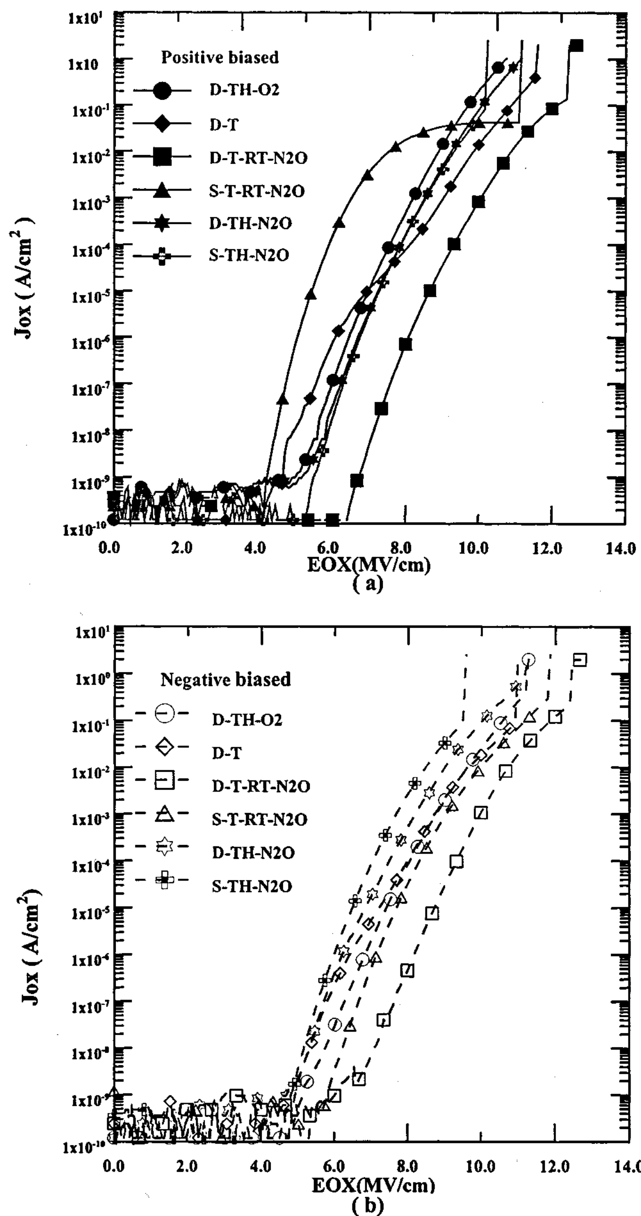


Fig. 3. J–E characteristics of the D-TH-O_2, D-TH-N_2O, S-TH-N_2O, D-T-RT-N_2O, S-T-RT-N_2O, and D-T six samples with (a) poly-II positive biased and (b) poly-II negative biased.

Comparing the J–E characteristics of the D-T sample with those of the thermally grown polyoxides grown on either the disilane poly-I, i.e., D-TH-O_2 and D-TH-N_2O, or on the silane poly-I, i.e., D-TH-N_2O and S-TH-N_2O, we find that the D-T sample, even though it had relatively smooth poly-II/oxide and oxide/poly-II interfaces, had a higher leakage current at the low

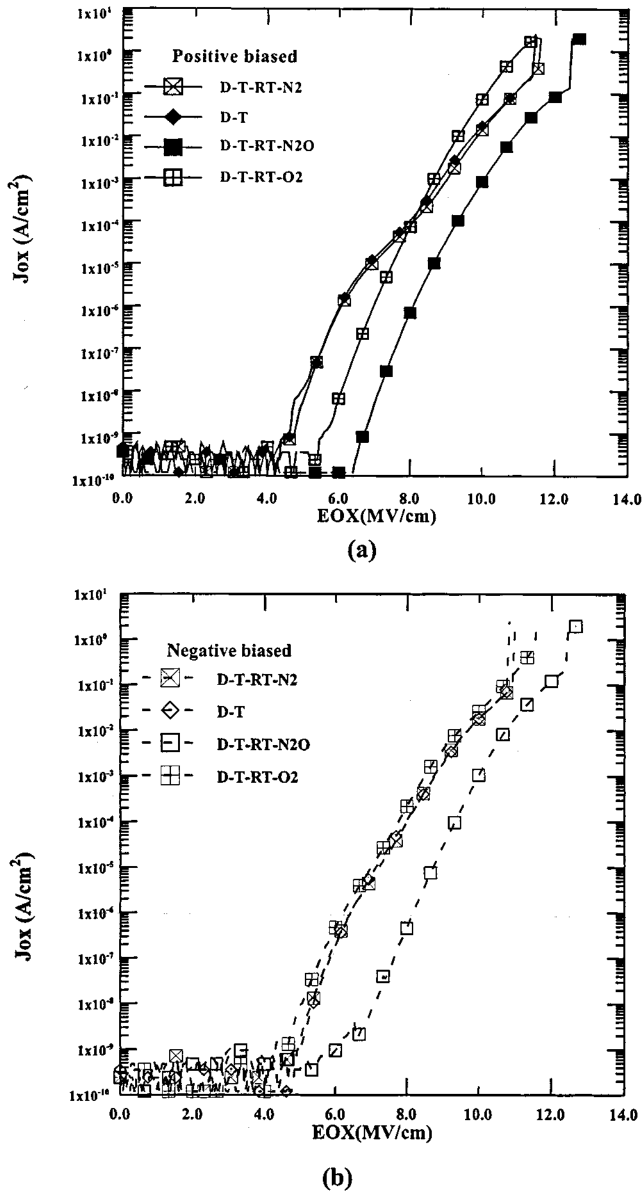


Fig. 4. *J–E* characteristics of the D-T-RT-N_2O, D-T, D-T-N_2, and D-T-RT-O_2 four samples with (a) poly-II positive biased and (b) poly-II negative biased.

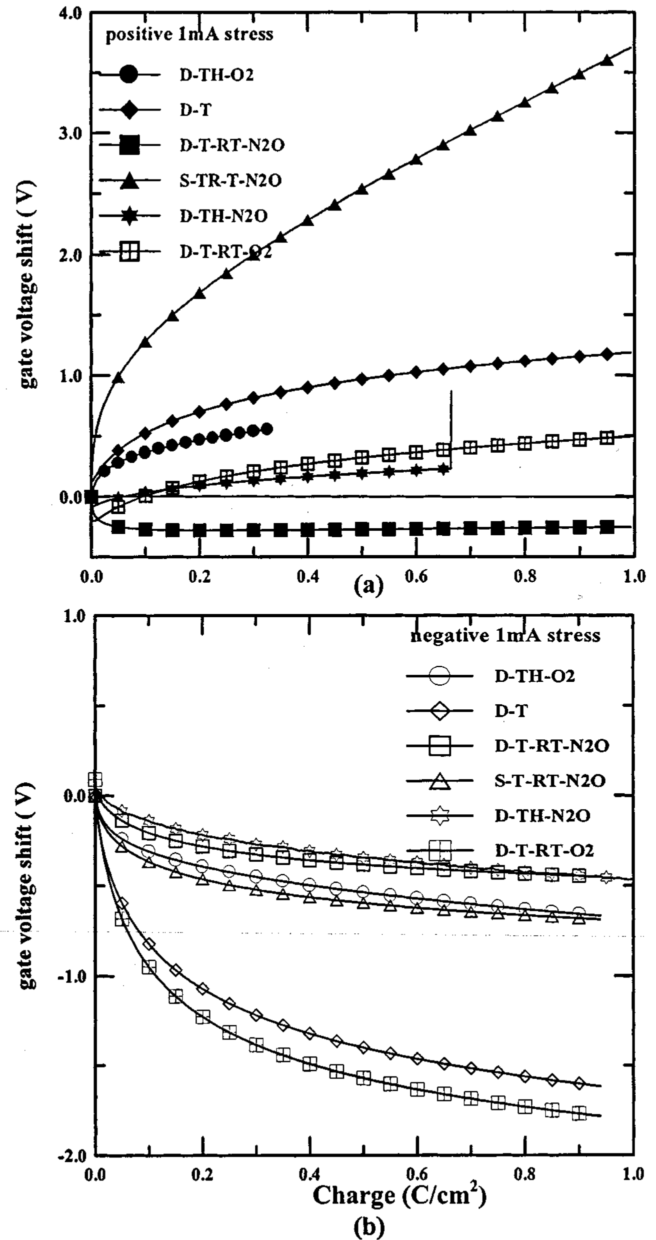
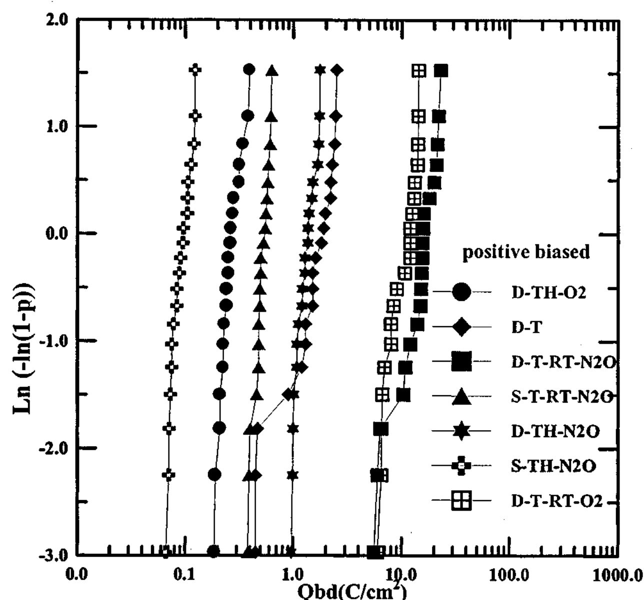


Fig. 5. Electron trapping characteristics of the D-TH-O_2, D-TH-N_2O, D-T-RT-N_2O, S-T-RT-N_2O, D-T-RT-O_2, and D-T six samples with (a) poly-II positive biased and (b) poly-II negative biased.

electric field regime. It is because, the TEOS oxide, deposited at a low temperature (700 °C), had a porous structure before RT annealing. This led a high trap density existing in the oxide, providing conduction paths for injected electrons under the applied field.

Fig. 4 shows the (a) positive *J–E* characteristics and (b) the negative *J–E* characteristics of the TEOS oxide deposited on the disilane films with rapid thermal annealing at 950 °C 30 s in N_2, O_2, and N_2O ambients, respectively. We can see that the RTN_2O annealed sample had the lowest leakage current. This can be simply explained by the fact that it had a relatively smoother interface than those of other samples. The RTN_2 sample did not have any improvement as compared with the as-deposited TEOS sample. In addition, we see that the RTO_2 improved the *J–E* characteristics of the TEOS oxide only in the positive bias. The improvement could be due to the additional thermal oxide grown during the annealing process. However, this process also enhanced the roughness of the polyoxide/polysilicon-I interface, consequently, that of the polysilicon-II/polyoxide interface. This might be the reason that the RTO_2 sample had the worse *J–E* characteristic than that of the as-deposited TEOS sample in the negative bias. Hence, in one word, owing to the smoothest interface and an additional oxide grown during annealing, the TEOS oxide deposited on the disilane polysilicon film with RTN_2O annealing is the best way to fabricate low leakage current polyoxides in our experiment.

Fig. 5 shows electron trapping characteristics of both polarities for the six samples under the 1 mA/cm^2 constant current stress. The electron trapping characteristics under stress are



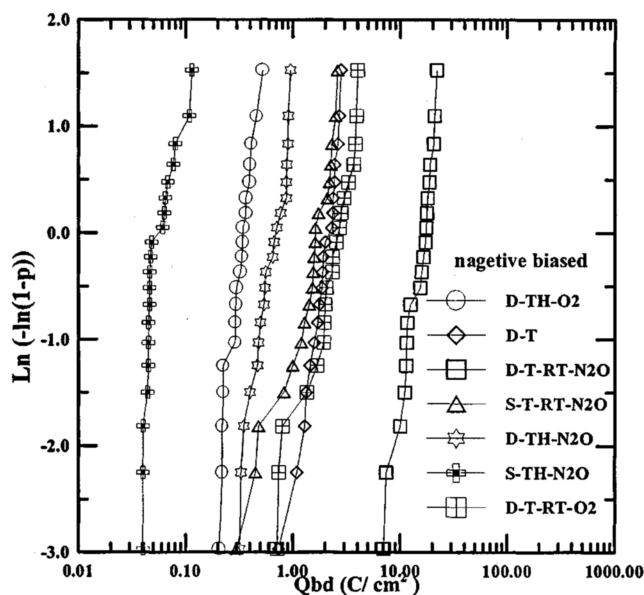


Fig. 6. Weibull plots of Q_{bd} of the D-TH-O_2, D-TH-N_2O, D-T-RT-N_2O, S-T-RT-N_2O, D-T-RT-O_2, and D-T six samples with (a) poly-II positive biased and (b) poly-II negative biased where the oxide thickness of the D-TH-O_2, D-TH-N_2O, and D-T is 130 Å and 150 Å of D-T-RT-N_2O, D-T-RT-O_2, and S-T-RT-N_2O, respectively.

determined by a combination of factors such as the injecting surface roughness, the intrinsic quality of the oxide, and the nitrogen incorporation at the interface. In general, a rougher injecting surface leads to a nonuniform electric field distribution, consequently, nonuniform injected electron distribution both at the injection interface and in the bulk of the polyoxide, leading to a higher trapping rate. In the figure, for the positive stress, where the poly-I was the injecting surface, the S-T-RT-N_2O sample had the highest trapping rate, reflecting its interface roughness. While the D-T-RT-N_2O sample had the lowest trapping rate, which is consistent with the fact that it had the smoothest interface. In addition, for the D-T-RT-N_2O sample,

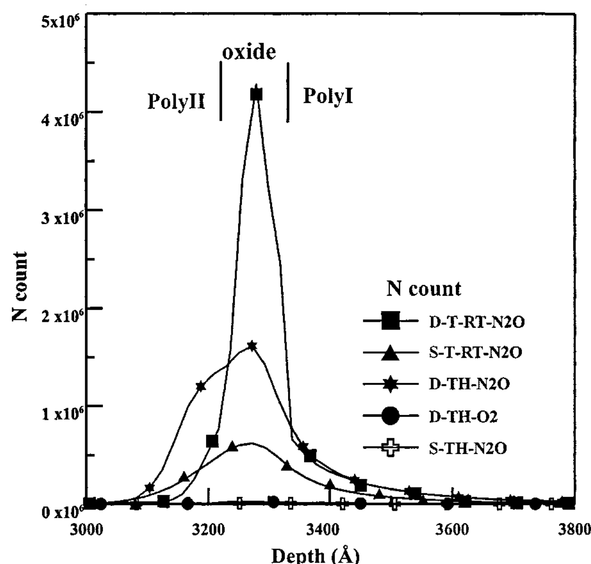


Fig. 7. SIMS profiles of Nitrogen count of the D-TH-O_2, D-TH-N_2O, S-T-RT-N_2O, D-T-RT-N_2O, and S-T-RT-N_2O samples, respectively.

it had asymmetric trapping characteristics, and for the positive polarity stress, it had a net hole trapping characteristic at the beginning stage of the stress. This might be due to the more nitrogen incorporation within the oxide since similar phenomenon were observed for the reported nitrogen-rich oxides prepared by N_2O or NO oxidation [11], [12]. Comparing the positive stress electron trapping characteristics of the variously prepared oxide samples on the disilane poly-I, the N_2O treated samples had smaller electron trapping rates than those of samples without the N_2O treatment. This indicates that N incorporation suppresses electron trapping [1]. For the negative stress electron trapping characteristics, however, since they are less relevant to the interface roughness of the polyoxide/poly-I, the N incorporation and the oxide intrinsic quality are the dominant factors in determining the characteristics. In the figure, it is still seen that the D-T-RT-N_2O sample had the smallest electron trapping rate, which reflected fact that it had the smoothest polysilicon-II/oxide injecting interface and the best oxide quality.

Fig. 6 shows Weibull plots of Q_{bds} of our experimental samples in both polarities, respectively. Also, it is seen that the D-T-RT-N_2O sample had the best Q_{bd} distributions for both polarities. Also, the D-T-RT-O_2 sample had the next better Q_{bd} distributions and the D-T was the third one. That is, for the Q_{bd} distribution consideration, the TEOS deposited on disilane film is a superior process then the thermal or the silane poly-I processes. Furthermore, among all the distributions, the D-T-RT-N_2O sample had the most symmetrical distributions. This is also believed to be due to the fact that the D-T-RT-N_2O had symmetrically smooth surfaces at both poly-I and poly-II interfaces. In addition, the N incorporation might also contribute to the result.

Fig. 7 shows the SIMS nitrogen profiles of D-T-RT-N_2O, S-T-RT-N_2O, D-TH-O_2, D-TH-N_2O, and S-TH-N_2O samples, respectively. The profiles show that the D-T-RT-N_2O samples had the highest nitrogen distribution among all the samples.

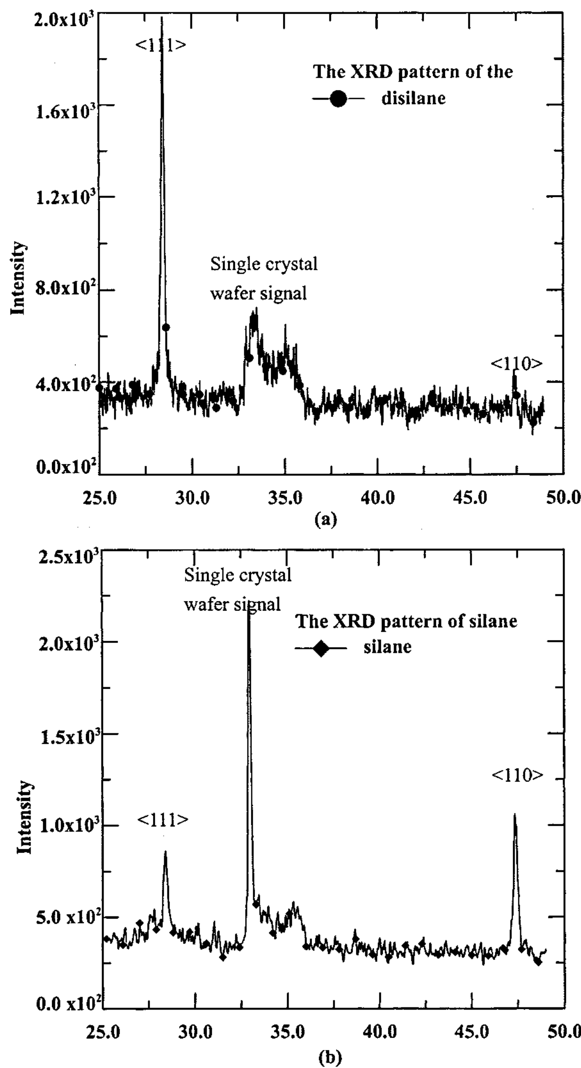


Fig. 8. XRD profiles of (a) disilane and (b) silane samples.

It is believed that it was this higher concentration of nitrogen incorporating reduces the dangling or strained bonds, consequently traps, in oxides. With fewer trappings, also the stronger nitrogen silicon bonds, the oxide had a lower leakage, a lower electron trapping rate, higher E_{bd} and Q_{bd}. In the figure, it is seen that the RT-N_2O samples had higher nitrogen contents than those of the thermal N_2O samples. Also, the disilane samples with the N_2O treatment had higher nitrogen content than those of the silane samples. That is, the nitrogen content in the D-T-RT-N_2O and the D-TH-N_2O samples were higher than that of the S-T-RT-N_2O sample. Fig. 8 shows the XRD (X-ray diffraction) patterns for (a) disilane polysilicon film and (b) silane polysilicon film, respectively. The patterns show that the disilane film had a strong peak at $\langle 111 \rangle$ orientation but weak at $\langle 110 \rangle$ orientations while the silane film had the strong $\langle 110 \rangle$ orientations but relatively weak $\langle 111 \rangle$ orientation. This means that the nitrogen incorporation was heavily dependent on the microstructure of poly-I film. This microstructure variations for polysilicons prepared by different methods had been discussed in [13] and a surface energy dependence model, that is, the microstructure difference will affect the surface energy of the polysilicon, was also proposed. From the SIMS and XRD data, it may be deduced that the disilane polysilicon surface may have a lower barrier in forming Si–N bonds. In our experiment, we also found that the resistivity of the disilane poly-I film was two times lower than that of the silane film. It may also due to this microstructure difference between these two polysilicon films.

In conclusion, with the smoothest interface and the highest nitrogen incorporation, the D-T-RT-N_2O had the smallest electron trapping rate characteristics and also the largest Q_{bd} distribution.

IV. Conclusion

In this work, the TEOS oxide deposited on the disilane polysilicon and then RT annealed in N_2O had been investigated along with other oxides such as those deposited on the silane polysilicon or directly thermally oxidized on polysilicon films. It was found that, due to the smoother surface of the disilane poly-I polysilicon and the higher nitrogen incorporation during the RT N_2O annealing process, the TEOS oxide had symmetrical positive and negative J–E characteristics, a much lower electron trapping rate, and a high Q_{bd} than all other oxides. The oxide is very suitable for the application as the inter-polyoxide for EEPROM.

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Jam Wem Lee was born in Taitung, Taiwan, R.O.C., on November 10, 1973. He received the B.S. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan. He is currently pursuing the Ph.D. degree in electronics engineering at National Chiao Tung University, where he is now researching the characteristics of the thin polyoxides, ultrathin oxides, and thin high k dielectrics.

Chung-Len Lee (S'70–M'75–M'81–SM'92) received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 1968, and the M.S. and Ph.D. degrees from Carnegie Mellon University, Pittsburgh, PA, in 1971 and 1975, respectively, all in electrical engineering.

Since 1975, he has been with the Department of Electronic Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he has been engaged in teaching and research in the fields of semiconductor devices, integrated circuits, VLSI, and computer-aided design and testing. He has supervised more than 100 M.S. and Ph.D. students to complete their theses and has published more than 200 papers in the above areas. He has been involved in various technical activities in the above areas in Taiwan and other parts of Asia.

Dr. Lee is on the Editorial Board of JETTA.

Tai-Fu Lei was born in Keelung, Taiwan, R.O.C., on September 17, 1944. He received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 1967, and the M.S. and Ph.D. degrees in electronics engineering from National Chaio Tung University, Hsinchu, Taiwan, in 1970 and 1979, respectively.

From 1970 to 1972, he was with the Fine Products Microelectronics Corporation, Taiwan, as an Engineer working on the fabrication of small-signal transistors. From 1980 to 1982, he was the Plant Manager of Photronic Corporation, Taiwan. In 1983, he joined the Faculty at National Chiao Tung University as an Associate Professor in the Department of Electronic Engineering and the Institute of Electronics, where he is currently a Professor. From 1984 to 1986, he was the Director of the Semiconductor Research Center. From 1991 to 1998, he was the Deputy Director of National Nano Device Laboratory, Taiwan. From 1998 to 2000, he was the Chairman of the Department of Electronics Engineering. His research interests are semiconductor devices and VLSI technologies.

Chao-Sung Lai was born in I-Lan, Taiwan, R.O.C., on May 20, 1969. He received the B.S. and Ph.D. degrees from National Chiao Tung University, Hsinchu, Taiwan, in 1991 and 1996, respectively.

In 1996, he joined the National Nano Device Laboratory, Hsinchu, where he was engaged in the research of SOl devices. In 1997, he joined the Chang Gung University, Tao-Yuan, Taiwan, as an Assistant Professor, where he has been engaged in the research of the characterization and reliability of deep-submicron MOSFET's, nitrated thin gate oxides, shallow trench isolation, and the modeling of dielectrics' reliability. He was the consultant of Nan-Ya Technology, Inc. for the 0.18-μm Logic-Team since 1997.

Dr. Lai won the Lam Award in 1997.