Effect of Temperature and Illumination on the Instability of a-Si:H Thin-Film Transistors under AC Gate Bias Stress

2001 Jpn. J. Appl. Phys. 40 L316

(http://iopscience.iop.org/1347-4065/40/4A/L316)

Jpn. J. Appl. Phys. Vol. 40 (2001) pp. L316–L318
Part 2, No. 4A, 1 April 2001

Effect of Temperature and Illumination on the Instability of a-Si:H Thin-Film Transistors under AC Gate Bias Stress

Chun-Yao HUANG, Teh-Hung TENG, Cheng-Jer YANG, Chang-Ho TSENG and Huang-Chung CHENG *
Department of Electronics Engineering and Institute of Electronics, Semiconductor Research Center, National Chiao-Tung University, Hsinchu 300, Taiwan, Republic of China

(Received September 8, 2000; accepted for publication October 25, 2000)

This work investigates the temperature and illumination effects on the a-Si:H thin-film transistors (a-SiH TFTs) under AC gate bias stress to find the larger threshold voltage shift and subthreshold swing change for the bias-temperature-stress (BTS) and bias-illumination-stress (BIS). Excess carriers from thermal-generation electron-hole pairs or photoexcited electron-hole pairs may significantly influence the instability of a-Si:H TFTs during bias stress. The instability mechanisms originate from the carrier-induced defect creation enhanced by thermal generation in the BTS case and also emphasized by photoexcitation for the BIS case. Both stress conditions will induce a larger threshold voltage shift and higher cutoff frequency than those for simple bias stresses.

KEYWORDS: a-Si:H TFTs, AC, bias-temperature-stress, bias-illumination-stress

Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) are now widely used as switch devices in large-area electronic devices such as active matrix liquid-crystal displays (AMLCDs). In addition to their application in LCDs, a-Si:H TFTs are also used in image sensors[1] and monographic printing devices,[2] including high-voltage TFT applications. Instability is a very important issue in a-Si:H TFTs, as it can degrade their electrical characteristics and affects the product lifetime. Hence, improving their stability has become an important issue.

For instability analysis of a-Si:H TFTs, two important electrical characteristics are extracted, namely, the threshold voltage shift and subthreshold swing change after a prolonged performance of the gate bias stress. The instability which causes the variation of electrical characteristics of the a-Si:H TFTs is attributed to two mechanisms. The first is charge trapping in a gate insulator of SiN_x,[3] and the second is state creation in an a-Si:H film.[4] Charge trapping is caused by carrier injection into SiN_x when the bias is applied to the gate electrode. This instability mechanism occurs in high gate bias operations or for TFTs with bad gate insulators, and creates more trap sites in SiN_x. State creation in a-Si:H films resembles the Staebler-Wronski effect[5] and is thought to be due to the breaking of weak Si–Si bonds and the formation of Si dangling bond defects associated with hydrogen motion.[6–8] The dangling bond formation is attributed to the breaking of Si–Si weak bonds in the a-Si:H layer while the a-Si:H layer is biased toward strong accumulation. This mechanism dominates in low-bias operations and in a-Si:H with a higher density of defects. In addition to two instability mechanisms, the defect pool model[9] was also introduced to explain the distribution of created defects in the energy band gap of a-Si:H. This concept, which describes the dependence of the energy position and the density of the dangling bonds in the equilibrated materials at the Fermi energy position during equilibration, was incorporated to enable discussion of the instability mechanisms of the stressed a-Si:H TFTs.

Generally, the instability of a-Si:H TFTs is discussed under DC bias stress.[2,3,10,11] However, the TFTs used in LCDs are operated in the AC mode. Although this field has received considerable interest[12–16] the dependence of TFT characteristics on the signal frequency has been little discussed. This work systematically studies the behavior of a-Si:H TFTs under various signal frequencies of bias stress with temperature or illumination to determine the relationship between TFT instability and signal frequency.

The a-Si:H TFTs used in the experiment had the conventionally inverted staggered structure. After depositing and patterning the Cr electrodes on the Corning 7059 glass substrates, three layers, i.e., silicon nitride, a-Si:H, and n^+ a-Si:H film, were deposited in a plasma-enhanced chemical vapor deposition (PECVD) system. After forming the Al source/drain contact electrodes, the n^+ a-Si:H layers between the source and drain were etched off by reactive ion etching. Consequently, the passivation layer was deposited to cap the channel region. An HP 41501A pulse generator and an HP 4156 precise semiconductor parameter analyzer were then used to apply the stress to the TFTs and extract the transfer characteristics after the application of AC bias stress. The bias measurement was performed for up to 1000 s and the transfer curves at the drain-to-source voltage of 1 V in the dark were extracted. The threshold voltage (V_{th}) is defined as the gate voltage at the intersection of the tangent of the I_d vs V_g curve at $I_d = 0.15$ mA. The subthreshold swing (S) is defined as the inverse slope of the drain current within the subthreshold region in logarithmic scale. During the bias stress, the source and drain electrodes were commonly grounded to prevent electrical field distortion. Additionally, substrate heating (50°C) or illumination was applied as desired during the AC gate bias stress.

The instability of a-Si:H TFTs reveals the frequency effects as different polarities of the AC bias were applied. Preliminary results from the previous experiment indicated the main cause of the resistance-capacitance (RC) effect which is caused by the resistivity while electrons and holes were passing through the n^+ source and drain. In other words, these effects are attributed to the concentration of carriers induced by gate bias in the channel of devices per gate signal cycle. That is, a large density of carriers creates more metastable defects than a low density.[17]

Figure 1 illustrates the variation of ΔV_{th} and ΔS versus signal frequency for a-Si:H TFTs stressed under various positive bias stress conditions. Shifts in electrical characteristics remain almost fixed with the variation of signal frequency, revealing frequency independence due to a low RC value.[16]

*E-mail address: hccheng@cc.nctu.edu.tw

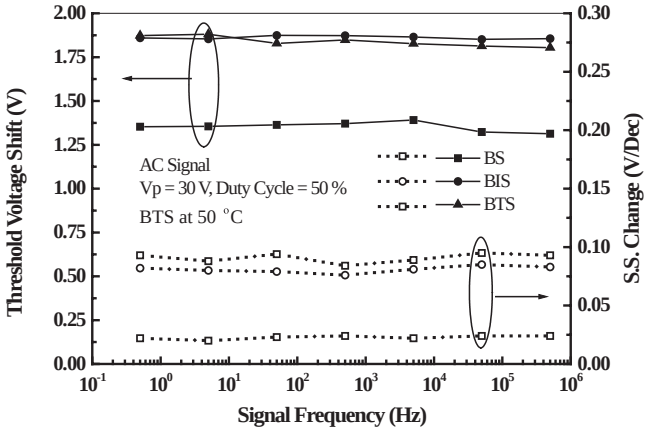

Fig. 1. Threshold voltage shift and subthreshold swing change versus signal frequency for a-Si:H TFTs stressed under different positive bias conditions, including bias stress (BS) and bias-illumination stress at 30°C, and bias-temperature stress at 50°C.

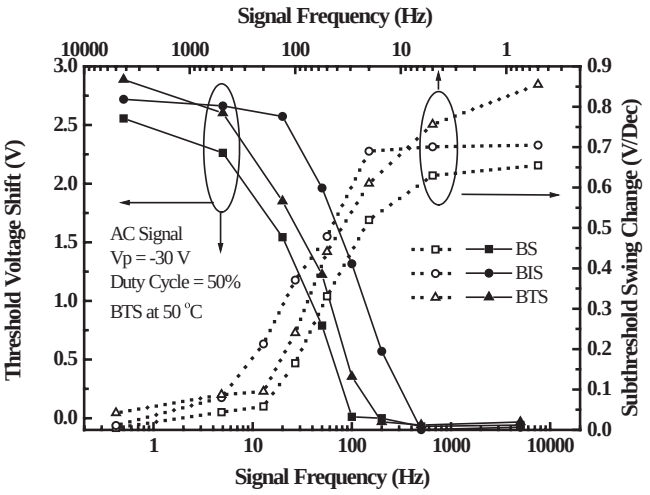

Fig. 2. Threshold voltage shift and subthreshold swing change as a function of signal frequency for a-Si:H TFTs stressed under different negative stress conditions, including bias stress (BS) and bias-illumination stress at 30°C, and bias-temperature stress at 50°C.

Additionally, the above phenomenon also indicates that the $\Delta V_{\rm th}$ and ΔS for TFTs stressed at BTS and BIS are larger than that at bias stress (BS). Figure 2 plots the relationship between $\Delta V_{\rm th}$ and signal frequency for negative bias stress conditions. The figure reveals that the $\Delta V_{\rm th}$ and ΔS of BTS and BIS are larger than those of BS and show frequency dependence with a distinct cutoff frequency. The $V_{\rm th}$ and S shifts of TFTs stressed at BTS and BIS exhibit a higher cutoff frequency than BS. The instability mechanisms can be attributed to a greater number of more created defect states owing to excess photoinduced carriers under illumination and thermal-enhanced defect formation and/or charge trapping with temperature stress.

To clarify the temperature and illumination effects on TFT instability, Fig. 3 shows the transfer characteristics of a-Si:H TFTs measured at 30°C and 50°C, both in the dark and under illumination. The current increase under illumination is due to photoexcitation of electrons and holes (i.e., photocurrent), and the current increase at 50°C originates from thermal-generation electron-hole pairs. At 30 V, the current increases from 41.6 nA to 65.1 nA as the temperature increases from

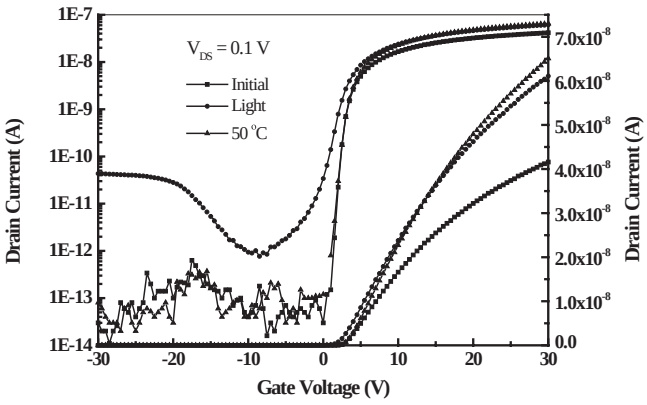

Fig. 3. Id-Vg transfer characteristics of a-Si:H TFTs under different measurement conditions. Measurements were performed under illumination and in the dark at different temperatures.

Table I. Currents at $V_{\rm g} = \pm 30$ V under different measurement conditions.

	30°C	Illumination	50°C
$V_{\rm g} = 30$ V	4.16×10^{-8} A	6.11×10^{-8} A	6.51×10^{-8} A
$V_{\rm g} = -30$ V	3×10^{-14} A	4.34×10^{-8} A	8×10^{-14} A

30°C to 50°C, and increases to 61.1 nA under illumination. On the other hand, at -30 V, the current changes from 30 fA to 43.4 pA under illumination but only increases to 80 fA at 50°C due to holes induced by the negative gate bias being blocked in an n^+ a-Si:H S/D. The difference in drain current is found to be that the dominant carriers are electrons under the positive gate bias and holes under the negative gate bias.[7] Table I lists the currents under different measurement conditions.

Figure 1 reveals that the $\Delta V_{\rm th}$ and ΔS under BTS and BIS are larger than those under BS. However, the instability mechanism differs between them. Under BTS, the creation of defect states via hydrogen motion is enhanced as the temperature increases due to an increase in the rate of hydrogen diffusion and a reduction in the formation barrier of defect states. Meanwhile, under BIS, the same phenomenon is attributed to the high carrier-induced defect-creation rate because numerous carriers generated by the illumination accumulate at the a-Si:H/SiN_x interface of TFT.[17] Table I shows that the current increases significantly under illumination. Thus, the degradation of electrical characteristics of TFTs stressed under BIS is also more serious than that under BS. In Fig. 2, the $\Delta V_{\rm th}$ and ΔS under BTS or BIS are also larger than under BS and have a higher cutoff frequency because of thermal generation or photoexcited electron-hole pairs. However, the currents at 50°C or under illumination differ under negative gate bias. As the temperature increases to 50°C, the current is only 80 fA. Hence, the mechanisms degrading the characteristics of TFTs are both thermal-enhanced defect formation and carrier-induced defect creation. For the BIS, the dominant mechanism is carrier-induced defect creation because of the large current ($I_{\rm d} = 43.4$ pA) that exists under illumination. Due to the large photoexcited carriers under illumination, holes can accumulate at the a-Si:H/SiN_x interface through the photocurrent, causing more defects to be created in the a-Si:H layers during each negative cycle.

This work investigated how temperature and illumination affect the instability of a-Si:H TFTs under AC bias stress. The ΔV_{th} and ΔS under BTS and BIS were found to be larger than those under simple bias stress, while the curves of the ΔV_{th} and ΔS of TFTs stressed under BTS and BIS shift toward a high frequency under negative AC bias. This phenomenon is attributed to carrier-induced defect creation combined with thermal-enhanced defect formation at BTS, and more serious carrier-induced defect creation due to photoexcited electron-hole pairs at BIS. Thus, we conclude that the larger density of carriers induced by every cycle causes more metastable defects, significantly degrading the electrical characteristics of a-Si:H TFTs.

This research was supported in part by the Republic of China National Science Council (ROC NSC) under contract No. NSC-89-2215-E009-068. Technical support from the Semiconductor Research Center in National Chiao-Tung University, the National Nano Device Laboratory, and the Unipac Optoelectronics Corporation are also acknowledged.

1) M. Matsumura, H. Hayama, Y. Nara and K. Ishibashi: Jpn. J. Appl. Phys. **20** (1980) 311.
2) J. Magarino: Appl. Phys. A **41** (1986) 297.
3) M. J. Powell: Appl. Phys. Lett. **43** (1983) 597.
4) C. van Berkel and M. J. Powell: Appl. Phys. Lett. **51** (1987) 1094.
5) L. Staebler and C. R. Wronski: J. Appl. Phys. **51** (1980) 292.
6) M. Stutzman, W. B. Jackson and C. C. Tsai: Phys. Rev. Lett. B **32** (1985) 23.
7) W. B. Jackson, J. M. Marshall and M. D. Moyer: Phys. Rev. B **39** (1989) 1164.
8) W. B. Jackson: Phys. Rev. B **41** (1990) 257.
9) M. J. Powell, C. van Berkel, A. R. Franklin, S. C. Deane and W. I. Milne: Phys. Rev. B **45** (1992) 4160.
10) T. Ogawa, S. Hotta and H. Takezawa: Mater. Res. Soc. Symp. Proc. **192** (1990) 385.
11) J. kanicki, C. Godet and A. V. Gelatos: Mater. Res. Soc. Symp. Proc. **219** (1991) 45.
12) R. Oritsuki, T. Horii, A. Sasano, K. Tsutsui, T. Koizumi, Y. Kaneko and T. Tsukada: Jpn. J. Appl. Phys. **30** (1991) 3719.
13) F. R. Libsh and J. Kanichi: SID'93 Dig. Tech. Pap. (1993) p. 455.
14) C. S. Chiang and J. Kanicki: *Proc. EuroDisplay'96* (SID, San Jose, 1996) p. 13.
15) C. S. Chiang, J. Kanicki, S. Nishida and K. Takechi: *AM-LCD'96 Dig. Tech. Pap.* (SID, Kobe, 1996) p. 265.
16) C. Y. Huang, T. H. Teng, J. W. Tsai and H. C. Cheng: submitted to Jpn. J. Appl. Phys.
17) W. B. Jackson: Phys. Rev. B **41** (1990) 1059.