AIP Journal of Applied Physics

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Citation: Journal of Applied Physics **89**, 3447 (2001); doi: 10.1063/1.1347405
View online: http://dx.doi.org/10.1063/1.1347405
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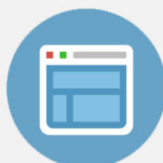

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Comparison of ultrathin $CoTiO_3$ and $NiTiO_3$ high-*k* gate dielectrics

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(Received 23 August 2000; accepted for publication 13 December 2000)

High-*k* cobalt–titanium oxide ($CoTiO_3$) and nickel–titanium oxide ($NiTiO_3$) were formed by directly oxidizing sputtered Co/Ti and Ni/Ti film. $Al/CoTiO_3/Si_3N_4/Si$ and $Al/NiTiO_3/Si_3N_4/Si$ capacitor structures were fabricated and measured. The effective dielectric constant (k value$\cong$45) with buffer layer for $CoTiO_3$ is larger than that of $NiTiO_3$. In addition, $CoTiO_3$ depicts excellent electrical properties at the same time. This metal oxide thus appears to be a very promising high-*k* gate dielectric for future ultralarge scale integrated devices. © *2001 American Institute of Physics.*
[DOI: 10.1063/1.1347405]

I. INTRODUCTION

To continue the scaling trend of complementary metal–oxide–semiconductor (CMOS) technology, the high leakage current is inevitable due to direct tunneling when oxide thickness is less than 25 Å.[1] In order to suppress the tunneling current, alternative gate dielectric with higher dielectric constant than conventional SiO_2 is necessary to provide a physically thicker film for the required equivalent oxide thickness E_{OT}. Gate dielectric materials having high dielectric constant, low interface state density, and good thermal stability are needed for future gate dielectric applications. Ultrathin silicon nitride[2] and Al_2O_3 (Ref. 3) gate dielectrics are proposed to replace the conventional oxide to meet the need for increased capacitance, while maintaining a low gate leakage. Because the dielectric constant is only two times larger than that of SiO_2, the technology life span of nitride or Al_2O_3 is expected to last no longer than two or three generations. Recently, many high-*k* materials such as HfO_2, ZrO_2, Ta_2O_5, and TiO_2 gate dielectric films have been widely studied;[4–7] however, these high-*k* films having a slightly higher leakage current and lower-*k* value may not be an adequate choice for alternative gate dielectric application. Materials having too high dielectric constant such as $SrTiO_3$ or $BaTiO_3$ may cause short-channel performance degradation due to the fringing fields from the gate to source/drain regions.[8] Also, dielectric constant materials larger than 50 are suitable only for dynamic random access memory applications, but inadequate as the gate dielectric of metal–oxide–semiconductor devices.

The formation of interfacial silicon oxide layer during the metal–oxide deposition process is a serious issue high-*k* gate dielectric development. An interfacial SiO_2 layer with a thickness over 20 Å was obtained when Ta_2O_5 was deposited directly on silicon. This interfacial oxide layer will limit the scalability of high-*k* dielectrics and cause poor interface quality.[9] Besides, thermal stability of the high-*k* dielectric is another major concern, as severe degradation of the dielectric quality has been shown to occur after Ta_2O_5 is subjected to processing temperature above 800 °C.[10] In this article, we report high-*k* dielectrics, i.e., $CoTiO_3$ and $NiTiO_3$, which is formed by direct oxidation of sputtering Co/Ti and Ni/Ti films. These metal–oxides were explored for their electrical property influence on oxidizing different temperature and time.

II. EXPERIMENT

Samples were fabricated on 6-in.-diam, *p*-type (100)-oriented Si wafers with resistivity of 14–21 Ω cm. All the wafers were first cleaned by the standard RCA clean method. To avoid reaction between metal and silicon during the sputtering process and later high-temperature oxide step, a 10 Å Si_3N_4 film was grown by NH_3 (flow rate 105 sccm, pressure 500 mTorr) nitridation of the Si substrate in a low pressure chemical vapor deposition system at 800 °C for 1 h. Afterward, all samples were immediately deposited in sequence with Ti (50 Å) and then Co (50 Å) or Ni (50 Å) film from independent targets by using the physical vapor deposition method. The direct thermal oxidation was carried out at 700, 750, or 800 °C in diluted $O_2(N_2/O_2=2/1)$ gas as listed in Table I to form cobalt–titanium oxide and nickel–titanium oxide films. A 5000 Å Al film was deposited on the wafer by a thermal coater to serve as the gate electrode. The gate of the MOS capacitor was defined by lithography, and then Al was etched by wet etching solutions. Finally, a 5000 Å Al film was also deposited on the backside of the wafers after stripping the oxide on the backside. The x-ray diffraction (XRD) provides identify of the composition and the phase of these new metal–oxide films. The equivalent oxide thickness of $CoTiO_3$ and $NiTiO_3$ oxidized for Si_3N_4 buffered layer structures was by high frequency capacitance–voltage ($C-V$) of 0.1 MHz at an operating range of -3–2 V in the strong accumulation region without considering quantum mechanical effects. The physical thickness was doubly checked by transmission electron micros-

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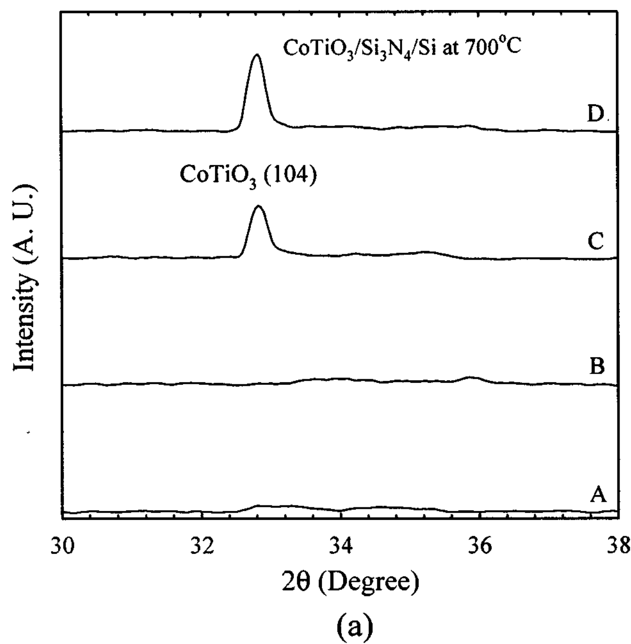


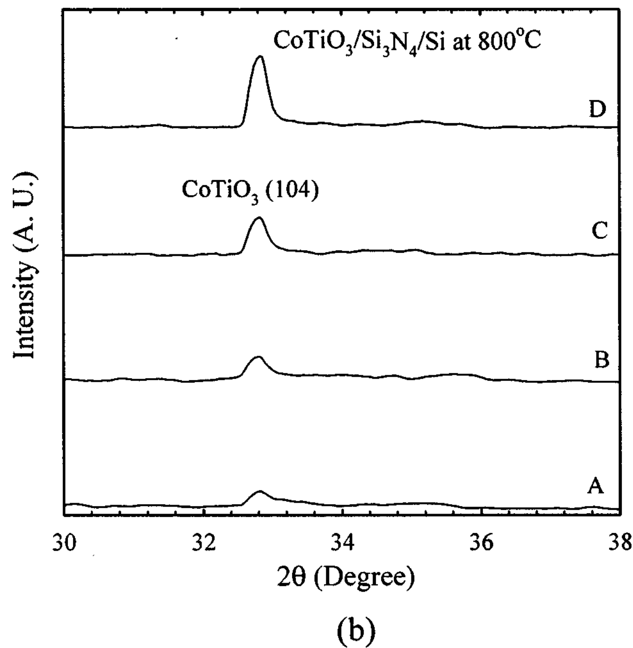
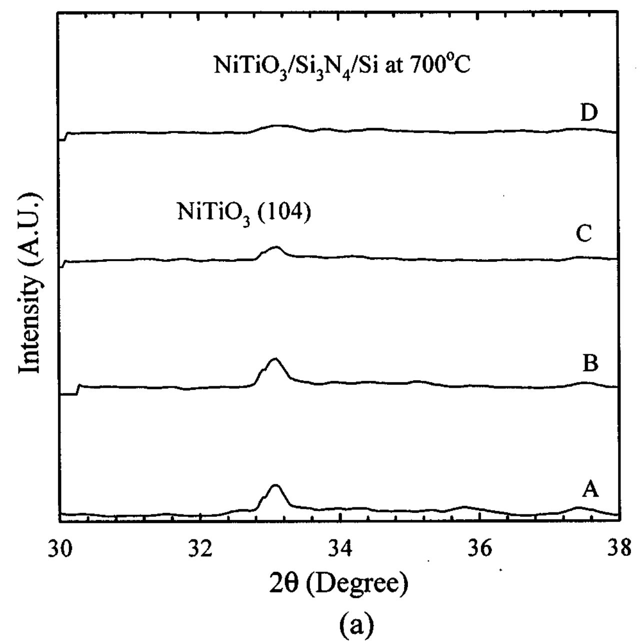


FIG. 1. XRD spectrum of $CoTiO_3$ films oxidized at: (a) 700 °C and (b) 800 °C for various conditions.



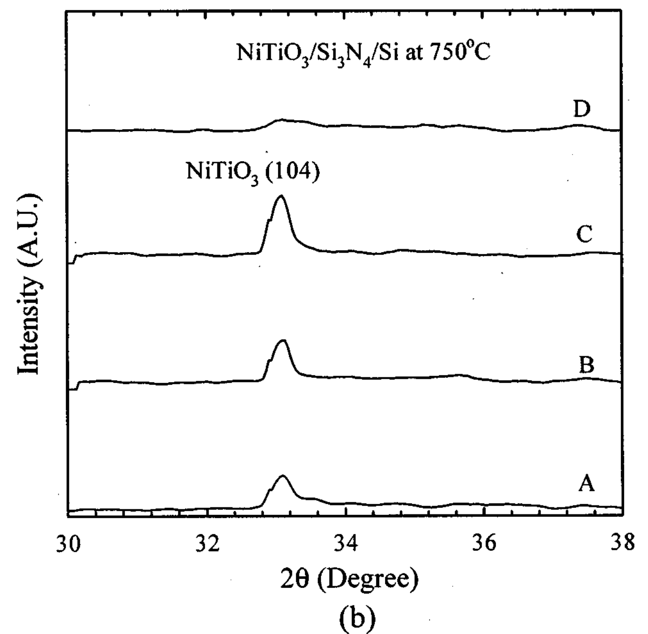


FIG. 2. XRD spectrum of $NiTiO_3$ films oxidized at: (a) 700 °C and (b) 750 °C for various conditions.

copy to obtain the *k* value. The electrical properties and reliability characteristics of the metal–oxide were measured by using the Hewlett–Packard (HP) 4156 semiconductor parameter analyzer.

TABLE I. Various oxidation conditions for $CoTiO_3$ and $NiTiO_3$ films.

Condition	Oxidation and annealing time
A	Oxidation for 5 min in diluted $O_2(N_2/O_2=1/1)$ gas
B	Oxidation for 5 min in diluted $O_2(N_2/O_2=1/1)$ gas and annealing for 5 min in N_2 gas
C	Oxidation for 10 min in diluted $O_2(N_2/O_2=1/1)$ gas
D	Oxidation for 10 min in diluted $O_2(N_2/O_2=1/1)$ gas and annealing for 10 min in N_2 gas

III. RESULTS AND DISCUSSION

Film crystallization and degradation during the backend thermal process is a major concern for metal–oxide with high dielectric constant. The Ilmenite structure is the $CoTiO_3$ (Ref. 11) and $NiTiO_3$ compounds in which Co or Ni and Ti both prefer to form a structure of octahedral coordination.[12] This structure is similar to the corundum structure of Al_2O_3, which is density and stable.[3,12] Figures 1(a)and 1(b) show XRD spectra of oxidizing at various conditions for $CoTiO_3$ samples. Samples with the Si_3N_4 buffer layer and oxidized at either 700 or 800 °C reacted with oxygen and formed cobalt–titanium oxide films (named $CoTiO_3/Si_3N_4/Si$). Samples oxidized at 800 °C under conditions A and B [Fig.

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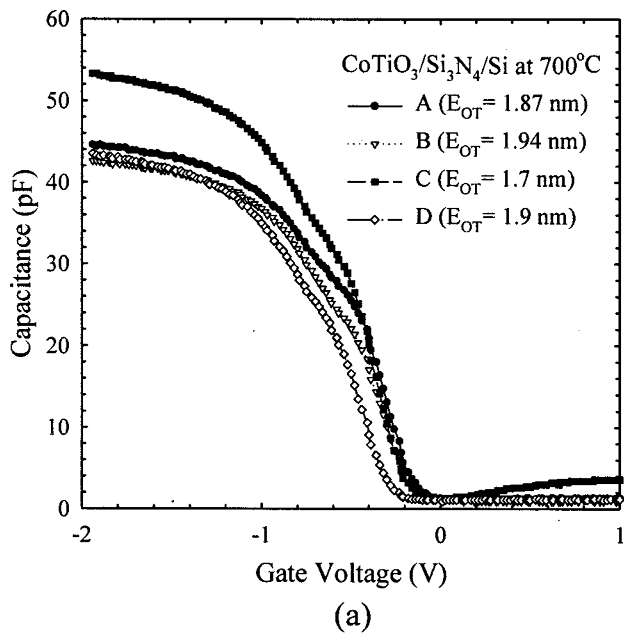


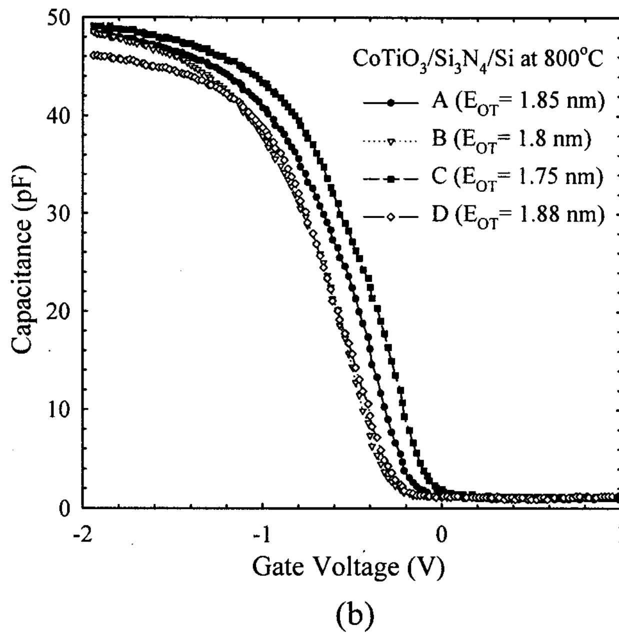
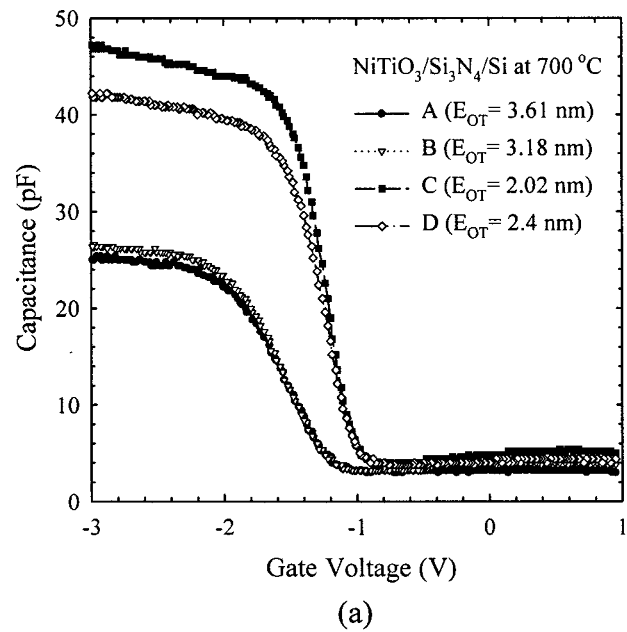


FIG. 3. $C-V$ curves of $CoTiO_3$ films oxidized at: (a) 700 °C and (b) 800 °C for various conditions.



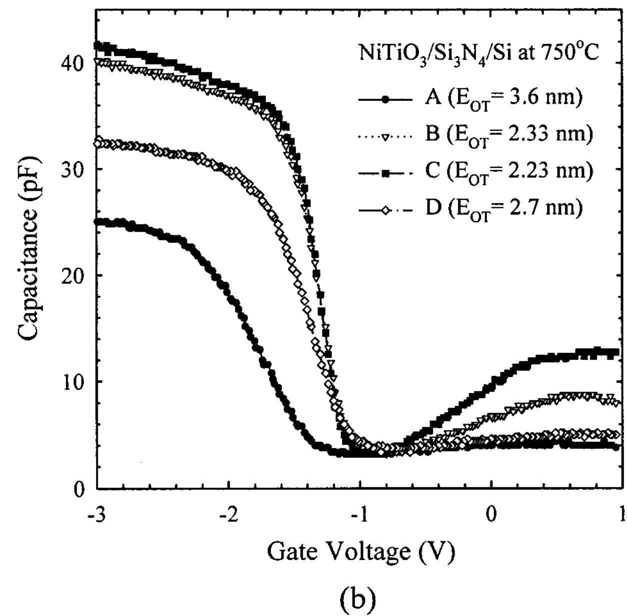


FIG. 4. $C-V$ curves of $NiTiO_3$ films oxidized at: (a) 700 °C and (b) 750 °C for various conditions.

2(b)] had a stronger spectrum than those of samples oxidized at 700 °C [Fig. 2(a)]. No noticeable $CoTiO_3$ crystal peak is observed for oxidation at 700 °C and 5 min, suggesting that there was insufficient time for crystallization. The $CoTiO_3/Si_3N_4/Si$ oxidized at either 700 or 800 °C for condition D (oxidation for 10 min, with additional 10 min N_2 annealing) has a stronger spectrum than that oxidized at condition C (only oxidation for 10 min). This implies that a sample oxidized and annealed for a long time can enhance crystallization of $CoTiO_3$. Figures 2(a) and 2(b) show the $NiTiO_3$ with the S_3N_4 buffer layer (named $NiTiO_3/Si_3N_4/Si$) for oxidation at 700 and 750 °C. Samples oxidized at 750 °C have a stronger spectrum than those oxidized at 700 °C. However, samples oxidized at 700 and 750 °C with condition D exhibit a weak peak. This phenomenon could be explained by the fact that the ultrathin silicon nitride buffer layer was not able to retard the nickel diffusion at an elevated oxidation and annealing process.

The tendency to form an interfacial silicon oxide layer during sputtering and thermal process makes it very difficult to realize the high k that one wishes to achieve. The use of a high quality silicon nitride buffer layer solves this problem.[11] The E_{OT} of these metal oxides with Si_3N_4 buffer layers are extracted from the $C-V$ curves of Figs. 3(a) and 3(b). Well behavior $C-V$ characteristics were observed for the $CoTiO_3/Si_3N_4/Si$ capacitor even with an E_{OT} of less than 20 Å. It is clear that the $CoTiO_3/Si_3N_4/Si$ capacitor with oxidation at 800 °C shows less distortion in the depletion region

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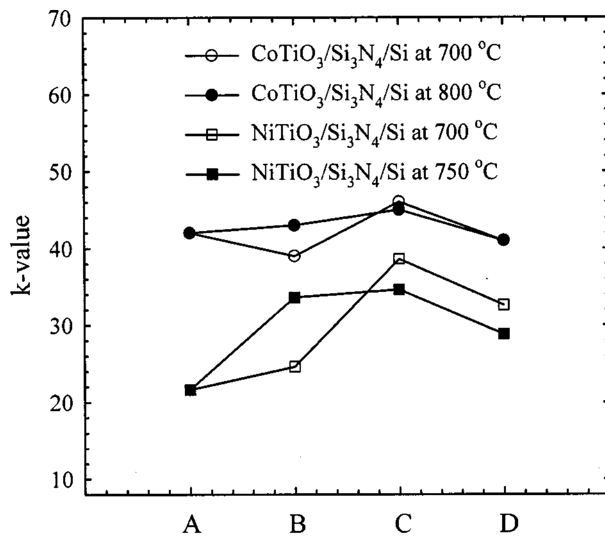
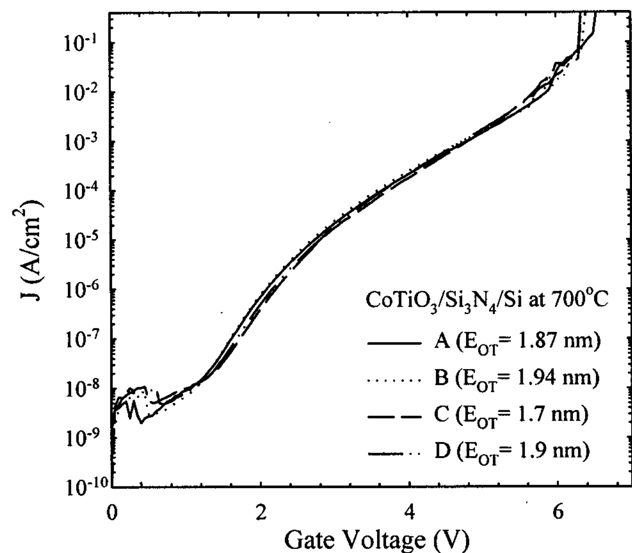


FIG. 5. The k value of $CoTiO_3$ and $NiTiO_3$ films oxidized at various temperatures and conditions.



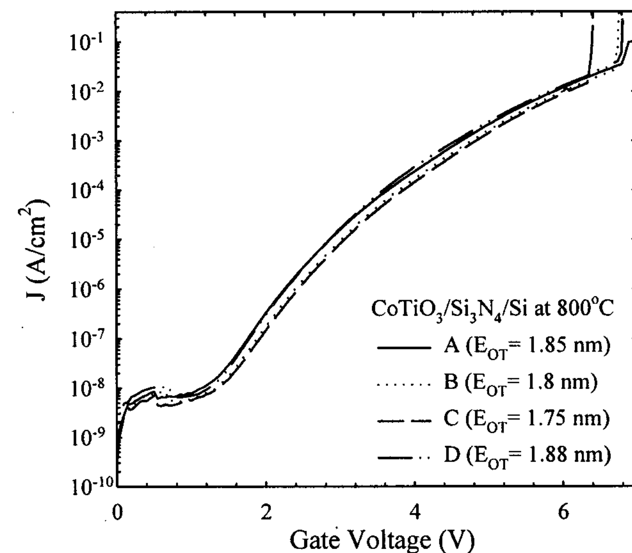


FIG. 6. $J-V$ characteristics of $CoTiO_3$ films oxidized at: (a) 700 °C and (b) 800 °C for various conditions.

than that of oxidation at 700 °C. This indicates that there could be insufficient temperature for densification and crystallization by oxidizing and annealing at 700 °C. The $C-V$ curves and E_{OT} with various process conditions for the $NiTiO_3/Si_3N_4/Si$ capacitor are shown in Figs. 4(a) and 4(b). The flatband voltage of the $NiTiO_3/Si_3N_4/Si$ capacitor is over -1.5 V, which is a larger than that of $CoTiO_3/Si_3N_4/Si$ of -1 V. The result is that $CoTiO_3$ can imply a lesser amount of fixed charge than $NiTiO_3$. In addition, as the E_{OT} of the $NiTiO_3/Si_3N_4/Si$ capacitor increases, it is suggested that nickel diffusion into the buffer layer will limit the scalability of high-k dielectrics and cause poor interface quality. The decreased capacitance value of conditions A and B oxidized at 700 °C for the $NiTiO_3/Si_3N_4/Si$ capacitor could be due to insufficient time for crystallization at this temperature. Nevertheless, the $NiTiO_3/Si_3N_4/Si$ capacitor oxidized at 750 °C for conditions A and D decreases capacitance value. This suggests that film crystallization has insufficient time at 750 °C and $NiTiO_3$ crystallization damages the ultrathin silicon nitride buffer layer to reduce k value.

The effective dielectric constant (k value) of these metal–oxides with buffer layer depends on the process conditions. The $CoTiO_3$ film including the silicon nitride buffer layer depicts a higher value than that of $NiTiO_3$ as shown in Fig. 5. On the other hand, it shows that samples oxidized at 700 °C in condition C for the $CoTiO_3/Si_3N_4/Si$ and $NiTiO_3/Si_3N_4/Si$ stacks have the highest k value among the four conditions. This result could be explained because metal–oxide for crystallization was insufficient by oxidizing time in conditions A and B. The metal–oxide formed crystallization in condition D seems to have damaged the ultrathin nitride buffer layer. Condition C is the optimum condition.

Figures 6(a) and 6(b) show the corresponding $J-V$ characteristics of $CoTiO_3/Si_3N_4/Si$ samples oxidized at 700 and 800 °C, respectively. It is noted that metal–oxides oxidized at 800 °C show compatible leakage current compared to the sample oxidized at 700 °C. Since all curves are close to each other, the gate leakage current and breakdown voltage of $CoTiO_3$ film is almost independent of those oxidized at different conditions. However, the gate leakage current and breakdown voltage of $NiTiO_3$ film depend on oxidizing at different conditions, as shown in Figs. 7(a) and 7(b). The gate leakage current density at a low field of $NiTiO_3/Si_3N_4/Si$ oxidized at 750 °C is lower than that oxidized at 700 °C. Thus, high temperature processes benefit from full crystallization of film.

Figure 8(a) shows the result after constant current stressing at -1 mA/cm^2 for the $CoTiO_3/Si_3N_4/Si$ stack. Time dependent dielectric breakdown measurement shows that there was no considerable charge trapping for these capacitors oxidized at 800 °C for condition C. No significant stress-induced-leakage current (SILC) was observed for these

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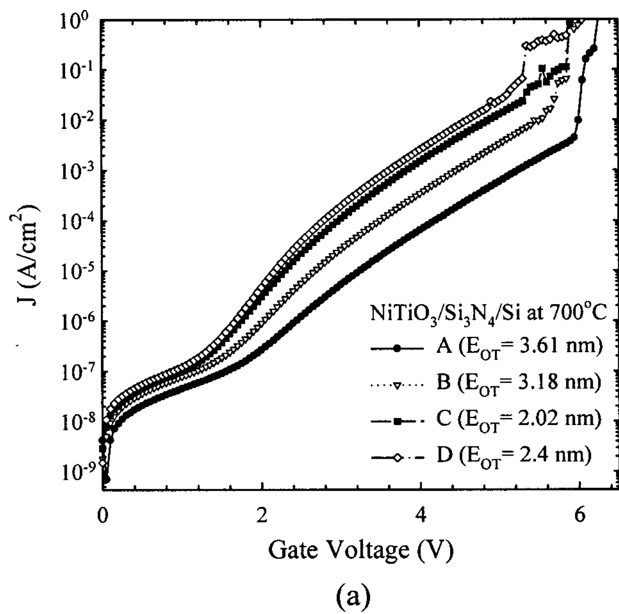


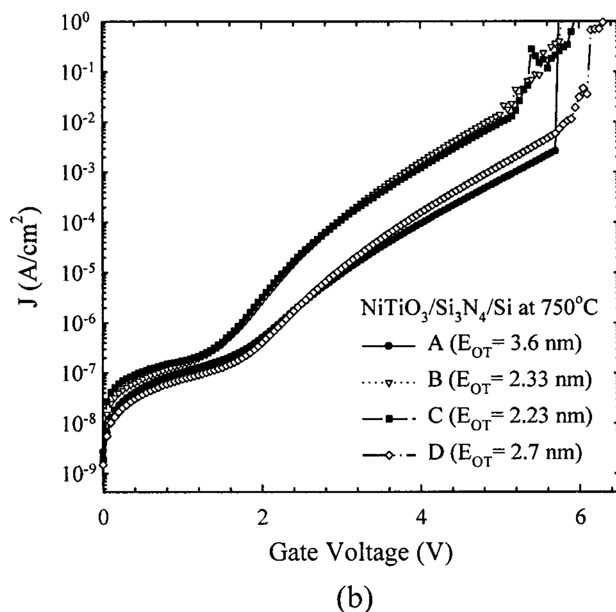
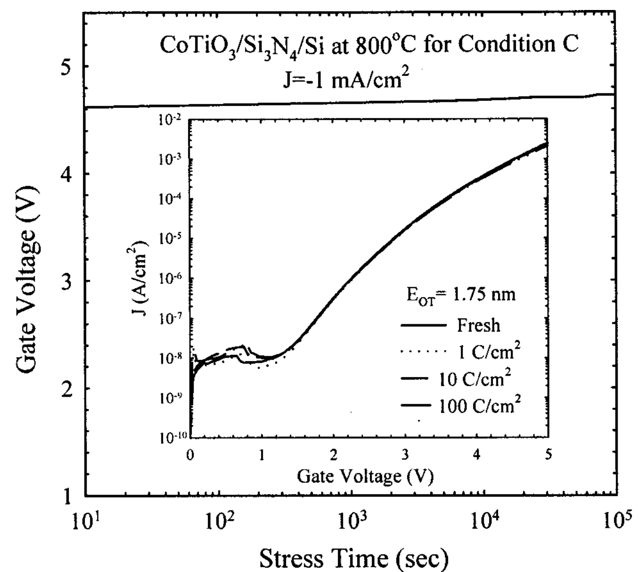


FIG. 7. $J-V$ characteristics of NiTiO$_3$ films oxidized at: (a) 700 °C and (b) 750 °C for various conditions.



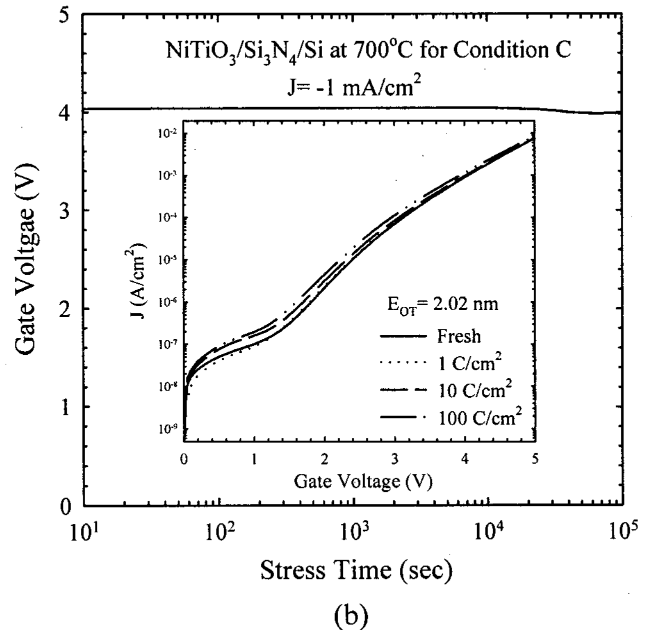


FIG. 8. The gate voltage during constant current stress of -1 mA/cm^2. Inset shows SILC under constant voltage stress for: (a) CoTiO$_3$/Si$_3$N$_4$/Si capacitors oxidized at 800 °C for condition C and (b) NiTiO$_3$/Si$_3$N$_4$/Si capacitors oxidized at 700 °C for condition C.

samples even after 10^5 s stressing, as shown in the inset of Fig. 8(a). On the other hand, from Fig. 8(b), the time dependence of the gate voltage shows that there is no significant charge trapping for the NiTiO$_3$/Si$_3$N$_4$/Si stack oxidized at 700 °C in condition C. No significant increase of leakage current was formed for these samples after 10^5 s stressing, as shown in the inset of Fig. 8(b). However, it indicates that some traps or defects exist in the NiTiO$_3$/Si$_3$N$_4$/Si structure. This phenomenon could result from nickel diffusion into the silicon interface, causing excessively fixed charge. From the above result, it is clearly seen that CoTiO$_3$/Si$_3$N$_4$/Si capacitors exhibit a less significant increase of leakage current in SILC than NiTiO$_3$/Si$_3$N$_4$/Si capacitors.

IV. CONCLUSION

We have reported high-k material cobalt–titanium oxide (CoTiO$_3$) and nickel–titanium oxide (NiTiO$_3$), which is formed by direct oxidation of the sputtered Co/Ti and Ni/Ti film. The CoTiO$_3$/Si$_3$N$_4$/Si structure shows higher k value and better electrical properties, such as low gate leakage current at low voltage operation and high reliability after stressing, than the NiTiO$_3$/Si$_3$N$_4$/Si structure. This high-k material with CoTiO$_3$ thus appears to be very promising for future ultralarge scale integrated devices.

ACKNOWLEDGMENTS

The authors would like to express their appreciation to the entire staff of the Semiconductor Research Center, National Chiao Tung University for their technical help. Finan-

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cial support was from National Science Council Taiwan, Republic of China under Contract No. NSC89-2215-E009-306.

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