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Tung Ming Pan, Tan Fu Lei, and Tien Sheng Chao

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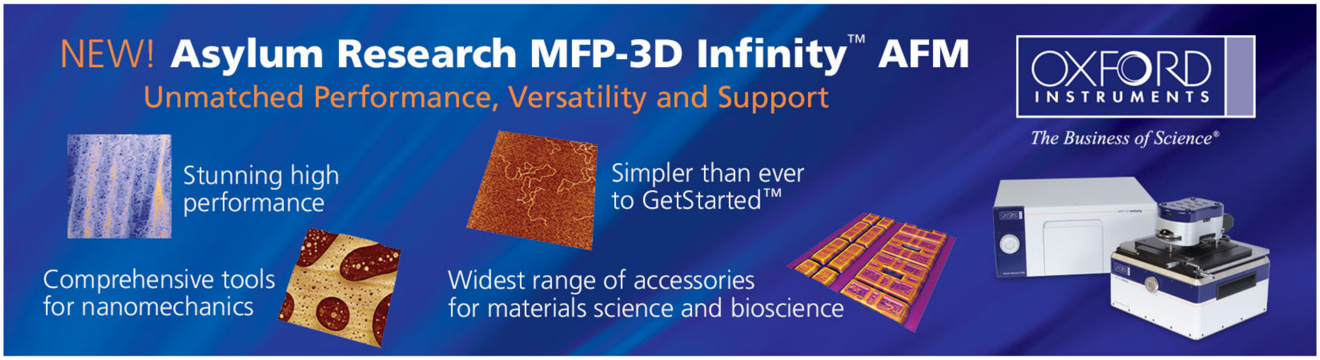

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High-*k* cobalt–titanium oxide dielectrics formed by oxidation of sputtered Co/Ti or Ti/Co films

Tung Ming Pan and Tan Fu Lei
Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, Republic of China

Tien Sheng Chao[a]
National Nano Device Laboratories, and Department of Engineering and System Science, National Tsing Hua University, Hsinchu 300, Taiwan, Republic of China

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High-*k* cobalt–titanium oxide ($CoTiO_3$) film was formed by directly oxidizing sputtered Co/Ti or Ti/Co films. $Al/CoTiO_3/Si_3N_4/Si$ capacitor structures were fabricated and measured. Excellent electrical properties with an effective dielectric constant (i.e., *k* value) as high as 40 have been achieved for a $CoTiO_3$ gate dielectric with a buffer layer. The metal–oxide thus appears to be a very promising high-*k* gate dielectric for future ultralarge scale integrated devices. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1352044]

As conventional SiO_2 gate dielectric scales down to less than 20 Å, a high leakage current is inevitable due to the occurrence of direct tunneling. To solve this problem, high-*k* (>3.9 of oxide) dielectric materials that allow a physically thicker film for the required equivalent oxide thickness (E_{OT}) are proposed to replace the conventional SiO_2.[1] Thus, gate dielectric materials having high dielectric constant, low interface state density and good thermal stability appear to be promising for future gate dielectric application. Recently, Si_3N_4 ($k=7$), Al_2O_3 ($k=9$), Ta_2O_5 ($k=25$), and TiO_2 ($k=40$) gate dielectric films have been widely studied.[2–5] However, these high-*k* films still exhibit undesirable high leakage current. The formation of an interfacial silicon oxide layer during the metal–oxide deposition process is a serious issue in high-*k* gate dielectric development. An interfacial SiO_2 layer with a thickness over 20 Å was obtained when Ta_2O_5 was deposited directly on silicon. This interfacial oxide layer seriously limits the scalability of high-*k* dielectrics and causes poor interface quality.[6] Besides, thermal stability of the high-*k* dielectric material is another major concern. Severe degradation of the dielectric quality has been shown to occur after Ta_2O_5 is subjected to processing temperature above 800 °C.[7] In this letter, we reported a cobalt–titanium oxide ($CoTiO_3$) film as an alternative gate dielectric. This $CoTiO_3$ film is formed by direct oxidation of Co/Ti or Ti/Co films. From our results, the dielectric constant can reach as high as 40, while depicting excellent electrical properties.

Samples were fabricated on *p*-type (100)-oriented Si wafers with resistivity of 14–21 Ω cm. All wafers were first cleaned by a standard Radio Corporation of America clean. To avoid reaction between metal and silicon during the sputtering process and later high-temperature oxidation step, a 10 Å Si_3N_4 film was first grown by NH_3 nitridation of the Si substrate in low-pressure chemical vapor deposition system at 800 °C for 1 h. Afterwards, samples were immediately deposited in sequence first with a 50 Å Ti and then a 50 Å Co (Co/Ti), or first a 50 Å Co and then 50 Å Ti (Ti/Co) film from independent targets by using a physical vapor deposition method. Direct thermal oxidation was carried out at 700 or 800 °C in diluted O_2 ($N_2/O_2=2/1$) gas for 5 min and annealed in N_2 ambient for 5 min to form $CoTiO_3$ films. A 5000 Å Al film was deposited on the wafer by a thermal coater to serve as the gate electrode. The gate of the metal–oxide–semiconductor (MOS) capacitor was defined by lithography, and then the Al was etched by a wet etching solution. Finally, a 5000 Å Al film was also deposited on the back side of the wafers after stripping the oxide on the back side. X-ray diffraction (XRD) was used to identify the composition and the phase of these new metal–oxide films. The gate dielectrics of MOS capacitors with an area of 2.5×10^{-5} cm^2 were measured. The E_{OT} (17.9–21.2 Å) of $CoTiO_3$ with a Si_3N_4 buffered layer structure was obtained by high frequency capacitance–voltage ($C-V$) of 0.1 MHz at an operating range of −2–2 V in a strong accumulation

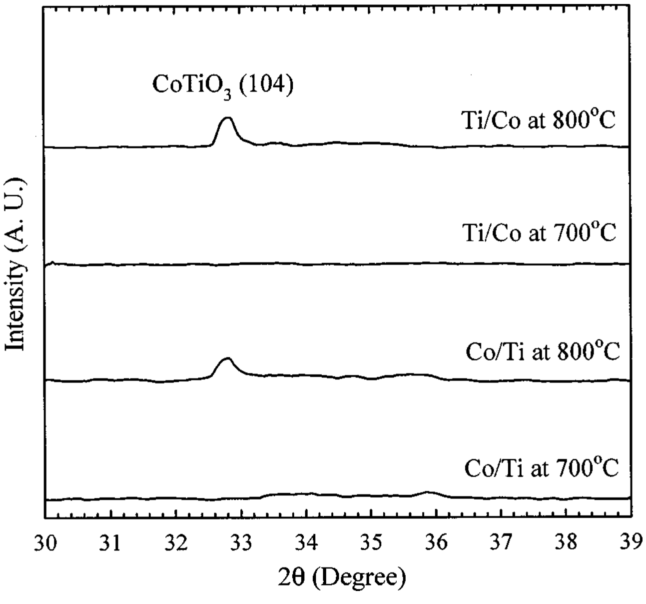

FIG. 1. XRD spectra of $CoTiO_3$ films with various stack structures and temperatures.

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[a] Electronic mail: tschao@ndl.gov.tw

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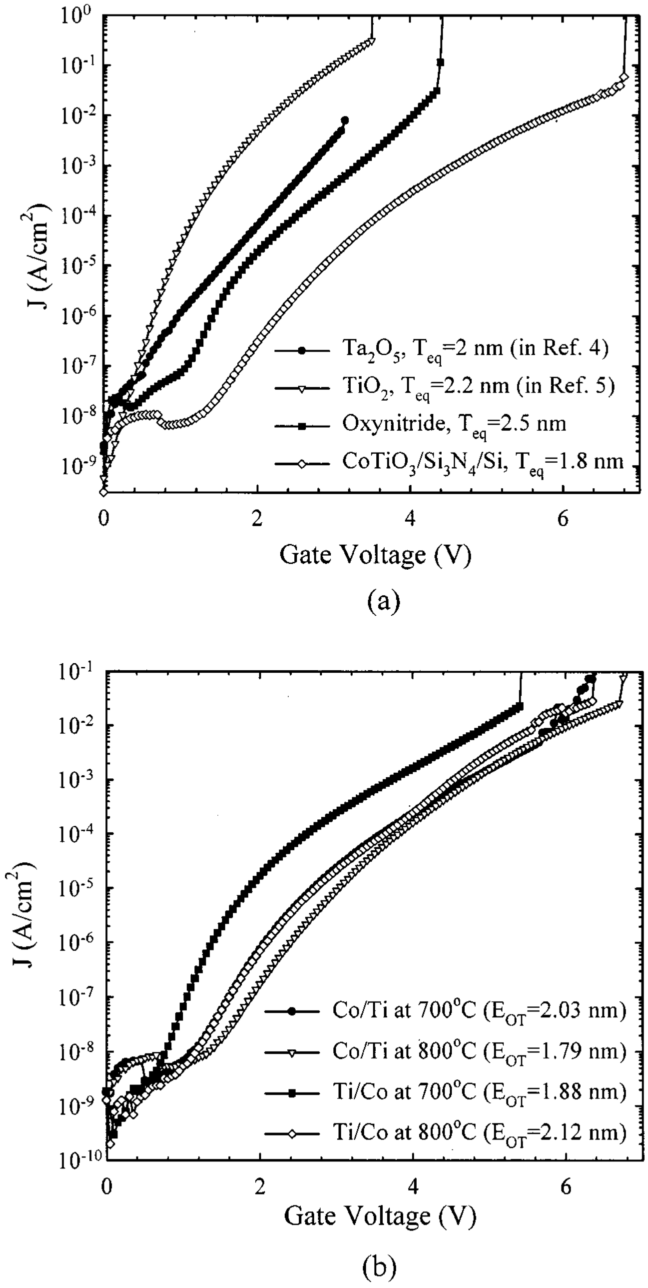

(a)

(b)

FIG. 2. *J–V* characteristics of (a) different gate dielectric material films with various equivalent oxide thicknesses and (b) $CoTiO_3$ films with various stack structures and temperatures.

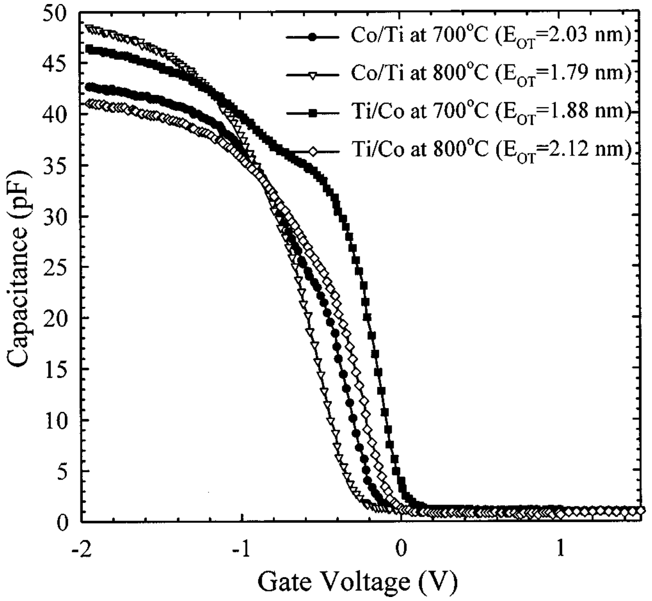

FIG. 3. High-frequency *C–V* curves of Co/Ti and Ti/Co films with 700 and 800 °C oxidation.

region without considering quantum mechanical effects. The physical thickness (~200 Å) was doubly checked by transmission electron microscopy to obtain the *k* value. The *k* value (36.8–43.6) is calculated by timing 3.9 to the physical thickness and dividing it by the E_{OT}. The electrical properties and reliability characteristics of the metal oxide were measured by using an Hewlett–Packard 4156 semiconductor parameter analyzer.

Film crystallization and degradation during a back-end thermal process is a major concern for high-dielectric-constant metal–oxide materials. Figure 1 shows the resultant XRD spectra. From the results, Co/Ti and Ti/Co samples oxidized at either 700 or 800 °C are found to react with oxygen and form $CoTiO_3$ films as shown in Fig. 1. The sample oxidized at 800 °C has a stronger spectrum than that of the sample oxidized at 700 °C. No noticeable $CoTiO_3$ crystal peak is observed for oxidation at 700 °C, suggesting insufficient time for crystallization, as shown in Fig. 1. Figure 2(a) shows current density–voltage (*J–V*) curves for different gate dielectric films. With a thinner E_{OT} of 1.8 nm, the $CoTiO_3/Si_3N_4/Si$ sample shows a lower leakage at low field and a higher breakdown voltage than those of Ta_2O_5 (E_{OT}= 2.0 nm, in Ref. 4), TiO_2 (E_{OT}= 2.2 nm, in Ref. 5), or oxynitride (E_{OT}= 2.5 nm). Figure 2(b) shows *J–V* curves of $CoTiO_3$ capacitors. Co/Ti and Ti/Co capacitors oxidized at 700 and 800 °C were compared. It is found that the Co/Ti capacitor oxidized at 800 °C demonstrates the highest breakdown voltage among all samples. In addition, the metal oxide oxidized at 800 °C exhibits a lower leakage current than that oxidized at 700 °C, implying that samples oxidized at 800 °C may exhibit $CoTiO_3$ crystallization.

The formation of an interfacial silicon oxide layer during sputtering and thermal processing makes it very difficult to

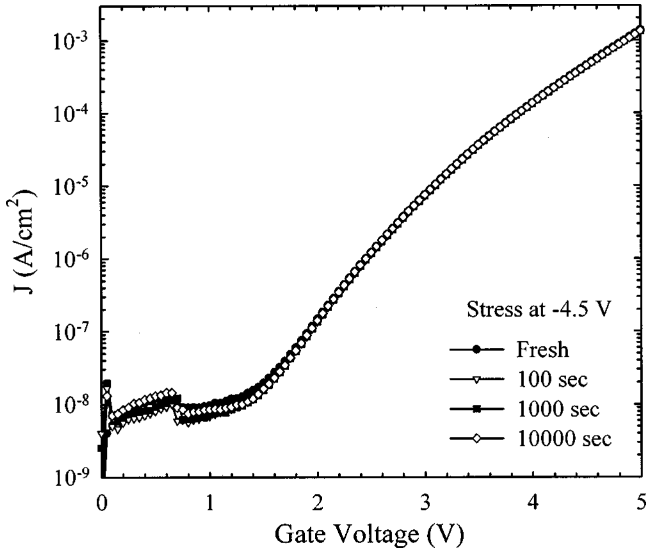

FIG. 4. SILC for Co/Ti capacitors with 800 °C oxidation.

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realize a high-*k* value. An effective method to solve this problem is to use a high quality silicon nitride buffer layer.[8] Figure 3 shows the high frequency ($C-V$) curves for Co/Ti and Ti/Co capacitors oxidized at 700 and 800 °C. It is found that the Co/Ti stack capacitor exhibits a higher capacitance (*k* value) than the Ti/Co stack capacitors. Figure 4 shows the result after constant voltage stress at -4.5 V for Co/Ti stack capacitors. No significant stress induced leakage current (SILC) was observed for these four samples even after 10^4 s stressing.

In summary, we have demonstrated a high-*k* $CoTiO_3$ which is formed by direct oxidation of the sputtered Co/Ti and Ti/Co film. The $CoTiO_3/Si_3N_4/Si$ stack by sputtering Co/Ti film oxidation shows higher *k* value and better electrical properties, such as low gate leakage current at low voltage operation, and high reliability after stressing. This high-*k* material with $CoTiO_3$ thus appears to be very promising for future ultralarge scale integrated devices.

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