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The reaction of Co and $Si_{1-x}Ge_x$ for MOSFET with poly-$Si_{1-x}Ge_x$ gate

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Abstract

The effects of Ge on the interfacial reaction between Co and poly-$Si_{1-x}Ge_x$ materials were studied. Poly-$Si_{1-x}Ge_x$ layers prepared at 580°C by ultra-high vacuum chemical molecular epitaxy (UHVCME) system were subjected to Co silicidation at various rapid thermal annealing (RTA) temperatures ranging from 500 to 900°C. From X-ray diffractometry (XRD), Co($Si_{1-y}Ge_y$) cubic structure was formed with RTA temperature ranging from 500 to 800°C for $x = 0.09$, while $CoSi_2$ was formed at 900°C. However, for $x = 0.21$, Co($Si_{1-y}Ge_y$) persisted even after 900°C RTA annealing, and $CoSi_2$ was not found. These results indicate that Ge atoms retard the formation of $CoSi_2$. As a result, the RTA temperature needed to obtain low sheet resistance has to be increased with increasing Ge content. Finally, p-channel metal-oxide-semiconductor (MOS) transistors with poly-$Si_{1-x}Ge_x$-gate have been successfully integrated with Co salicidation process.

Keywords: Poly-SiGe; Co; Silicide

1. Introduction

Polycrystalline silicon-germanium (poly-$Si_{1-x}Ge_x$) material has recently been shown to be a promising alternative to pure polycrystalline silicon (poly-Si) for various applications in IC technologies [1–3]. By taking advantage of its lower processing temperature, thin film transistor (TFT) with processing temperature not exceeding 550°C can be fabricated with poly-$Si_{1-x}Ge_x$ films [1]. Furthermore, the compatibility with existing silicon processing technology and the ability of threshold voltage adjustment by changing the Ge content have made heavily doped p-type poly-$Si_{1-x}Ge_x$ a very promising gate-electrode material for deep submicrometer complementary metal-oxide-semiconductor (CMOS) technologies [2,3]. In order to reduce the interconnection and contact resistance for high-performance circuit applications, metal silicidation of poly-$Si_{1-x}Ge_x$-gate and Si-source/drain is indispensable. Significant efforts have thus been made to understand the phase formations and properties of metal/$Si_{1-x}Ge_x$ reactions. Among the potential metal silicides, $CoSi_2$ depicts many advantages including low resistivity, relatively small lattice mismatch with Si, and compatibility with self-aligned silicide (salicide) scheme [4,5]. Three cobalt silicide phases, i.e., Co_2Si, CoSi, and $CoSi_2$, are known to form in sequence after annealing Co/Si bilayer structure [6]. In the past few years, the reaction of Co/epitaxial-$Si_{1-x}Ge_x$/Si system has been actively studied [7–11], while the studies of Co/poly-$Si_{1-x}Ge_x$ reaction still lack. For the ternary phase diagram of the Co–Si–Ge system, a miscible ternary compound, Co($Si_{1-y}Ge_y$), is found after low temperature furnace annealing (in the range 400–700°C) [9]. However, for the different crystal structures of $CoSi_2$ and $CoGe_2$, addition with preferable reaction between Co and Si, only the $CoSi_2$ phase can be observed at higher temperatures (~700°C by furnace annealing) [9]. For the poly-$Si_{1-x}Ge_x$ used as the gate in metal-oxide-semiconductor (MOS) transistor, it is usually highly doped to degeneration. During thermal processing, the dopants may redistribute and interfere with the Si–Co interaction. A surface accumulation of boron redistributed from $Si_{1-x}Ge_x$ consumption layer is observed in the Co/epitaxial-$Si_{1-x}Ge_x$ system, and boron in the underlying unconsumed $Si_{1-x}Ge_x$ region is unaltered [12,13]. We expect that the reaction of Co with poly-$Si_{1-x}Ge_x$ has the same result to avoid the poly-gate-depletion effect in poly-$Si_{1-x}Ge_x$-gated MOS device.

In this paper, we have studied the interfacial reaction of Co with p^+ poly-$Si_{1-x}Ge_x$ film in salicide processes suitable for MOS transistor application. The effects of Ge content

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Table 1
Phase formation and crystal orientation after the reaction of Co and poly-$Si_{1-x}Ge_x$ at different RTA temperatures

Temperature (°C)	Co/poly-$Si_{0.91}Ge_{0.09}$	Co/poly-$Si_{0.79}Ge_{0.21}$
500–700	$Co(Si_{1-y}Ge_y)$: (2 1 0), (2 1 1) and (2 0 0)	$Co(Si_{1-y}Ge_y)$: (2 1 0), (2 1 1) and (2 0 0)
800	CoSi: (2 1 1) $CoSi_2$: (3 1 1)	CoSi: (2 1 1)
900	$CoSi_2$: (1 1 1), (2 2 0) and (3 1 1)	CoSi: (2 1 1)

on the compound formation and boron redistribution during silicidation were also studied.

2. Experimental

In this work, 6 in. (1 0 0) Si wafers coated with a thermal nitride were used as the substrates. Poly-$Si_{0.91}Ge_{0.09}$ and poly-$Si_{0.79}Ge_{0.21}$ films about 2000 Å thick were grown by an ultra-high vacuum chemical molecular epitaxy (UHVCME) system, and were doped by BF_2 implantation to a boron concentration of $\sim 1\times10^{20}$ cm^{-3}. The strain of grain was small in the as-deposited poly-$Si_{1-x}Ge_x$ films [14]. Wafers with grown poly-$Si_{1-x}Ge_x$ films were then cleaned by a standard RCA-clean, and dipped in HF:H_2O (1:50) for 30 s for native oxide removal. After rinse and spin-dry, wafers were immediately loaded into a sputter-deposition chamber to deposit a 17 nm-thick Co thin film and a 30 nm-thick TiN-capping layer on top of the Co film. The Co/poly-$Si_{1-x}Ge_x$ reaction was performed at different temperatures in a conventional rapid thermal annealing (RTA) system under N_2 ambient for 30 s. After silicidation process, TiN capping layer and the unreacted Co film were selectively removed by wet etching in $4H_2SO_4$:$1H_2O_2$ (30%) solution for 5 min. The sheet resistance was determined by four-point probe measurement. While the structural and compositional properties of the reacted thin films were carefully examined by X-ray diffractometry (XRD), Auger electron spectroscopy (AES), and Secondary ion mass spectroscopy (SIMS).

In this study, p-channel MOS transistors with p^+-poly-$Si_{1-x}Ge_x$ gate were also fabricated on 6-in. p-type Si wafer using the nitride(30 Å)/oxide(30 Å) layer as the gate dielectric structure [3]. The 200 nm-thick undoped poly-$Si_{0.64}Ge_{0.36}$ layer was grown by UHVCME system. Standard poly-Si plasma etch recipe was then used to pattern the poly-$Si_{1-x}Ge_x$ film. The source/drain junctions were formed by BF_2 implantation. After a cleaning step and HF dip, 10 nm Co and 30 nm TiN were sputtered on the wafer. The Co salicide was performed by a two-step RTA annealing. The first-step annealing was 480°C for 30 s. TiN capping layer and the unreacted Co film were selectively removed by wet etching. Then, the second-step annealing was performed at 850°C for 30 s.

3. Results and discussion

The phase formation, together with its crystal orientations after Co silicidation on poly-$Si_{0.91}Ge_{0.09}$ and poly-$Si_{0.79}Ge_{0.21}$ layers was monitored by XRD in the θ–2θ geometry. The measurement results are summarized in Table 1. We can see that in the range 500–700°C of RTA temperature, the predominant phase is $Co(Si_{1-y}Ge_y)$, as Co_2Si phase could be removed during the selective wet etching of TiN/Co film. However, the diffraction peaks associated with $Co(Si_{1-y}Ge_y)$ move towards those of CoSi with increasing RTA temperature. This indicates that the Ge content in $Co(Si_{1-y}Ge_y)$ decreases with increasing RTA temperature. The result was also observed on the reaction of Co and epitaxial-$Si_{1-x}Ge_x$ [13]. By Vegard's law, the Ge indices y in $Co(Si_{1-y}Ge_y)$ can be calculated from the locations of X-ray diffraction peaks. For Co/poly-$Si_{0.91}Ge_{0.09}$ samples, the calculated Ge indices are 0.08, 0.06, and 0.03 for the samples annealed at 500, 600, and 700°C, respectively. Above 800°C, only CoSi and $CoSi_2$ are found and no Co–Ge phase is observed. It has been reported that the heat formation of CoSi (-7 Kcal (g atom)$^{-1}$) is much lower than that of CoGe (-4 Kcal (g atom)$^{-1}$) [9]. Thus, in Co/$Si_{1-x}Ge_x$ reaction at 600–800°C, Ge may be rejected in favor of Co–Si reaction [9]. This implies that more Ge atoms are segregated from the $Co(Si_{1-y}Ge_y)$ phase with increasing temperature. Fig. 1 shows the AES spectra of Co/poly-$Si_{0.91}Ge_{0.09}$ sample annealed at 900°C. In this figure, TiN capping layer and the unreacted Co film have been removed. As illustrated, the segregated Ge atoms accumulate in the surface of the sample, and the Ge/Si atomic ratio in the middle of the reacted layer is less than that of the underlying poly-$Si_{1-x}Ge_x$ layer. This is similar to previous observation on the reaction of Co and epitaxial-$Si_{1-x}Ge_x$ [7,12,13]. Because the transformation of CoSi to $CoSi_2$ can

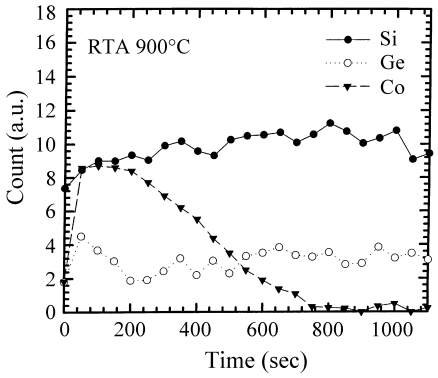

Fig. 1. AES spectra after Co annealing on poly-$Si_{0.91}Ge_{0.09}$ layers at 900°C.

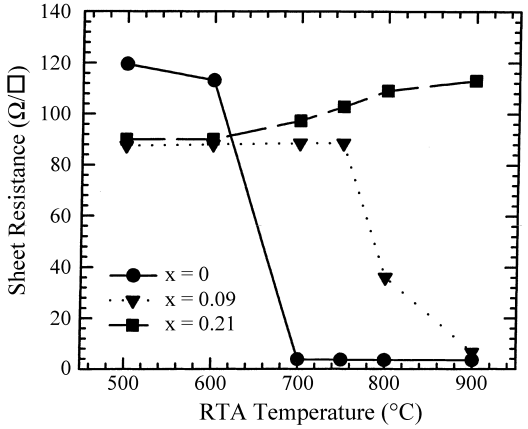

Fig. 2. Temperature dependence of sheet resistance for various Co/poly-$Si_{1-x}Ge_x$ and Co/poly-Si samples.

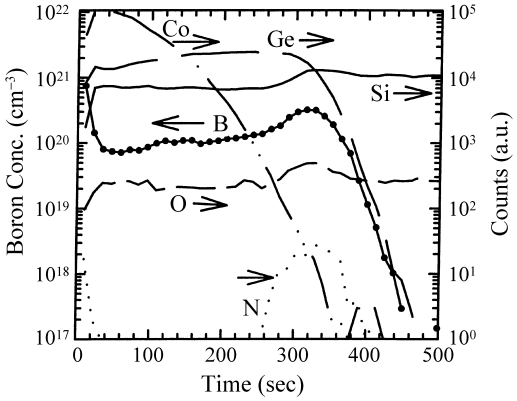

Fig. 3. The SIMS depth profile for Co(10 nm)/poly-$Si_{0.79}Ge_{0.21}$(200 nm) on nitride/oxide gate dielectric structure after 850°C RTA annealing.

only occur when Co diffusion dominates at the interface between the Co and the reacted region, the Ge-rich interfacial layer will act as diffusion barrier, and retard the formation of $CoSi_2$ [7]. This phenomenon is more severe for Co/poly-$Si_{0.79}Ge_{0.21}$ sample, so no $CoSi_2$ is observed even after 900°C annealing. While for Co/poly-$Si_{0.91}Ge_{0.09}$ sample, $CoSi_2$ phase could be identified after 900°C annealing, and the main diffraction peaks correspond to (1 1 1), (2 2 0) and (3 1 1) orientations. In addition, the main crystal orientations of $CoSi_2$ are the same as that of the poly-$Si_{1-x}Ge_x$ [14]. This indicates that $CoSi_2$ has the tendency to grow along the underlying poly-$Si_{1-x}Ge_x$ orientation.

Fig. 2 demonstrates the dependence of sheet resistance on the RTA temperatures for Co/poly-$Si_{0.91}Ge_{0.09}$ and Co/poly-$Si_{0.79}Ge_{0.21}$ samples. The conventional Co/poly-Si samples were also measured for comparison. At 500 and 600°C, the sheet resistance of Co/poly-Si sample is much higher than that of the Co/poly-$Si_{1-x}Ge_x$ sample. This is probably because of the relatively low resistivity of the CoGe phase. On the other hand, the sheet resistance of the reacted Co/poly-$Si_{1-x}Ge_x$ films after 700 and 800°C annealing is much higher than that of the Co/poly-Si counterparts. This is believed to be due to the formation of a Ge-rich surface layer by Ge segregation and the high-resistive CoSi growth in Co/poly-$Si_{1-x}Ge_x$ films. While the low-resistivity $CoSi_2$ phase has already been formed for Co/poly-Si reaction at these intermediate temperatures (i.e., 700 and 800°C), as is confirmed from the X-ray diffraction spectra. In addition, the sheet resistance begins to decrease for Co/poly-$Si_{0.91}Ge_{0.09}$ with 800°C annealing, but the sheet resistance for Co/poly-$Si_{0.79}Ge_{0.21}$ remains high. This indicates that the formation of $CoSi_2$ is indeed retarded in high Ge content samples. This may be due to the decrease of Co or Si diffusion as a result of the Ge accumulation at the Co/poly-$Si_{1-x}Ge_x$ reaction interface [7]. While the sheet resistance of Co/poly-$Si_{0.91}Ge_{0.09}$ samples is reduced to less than 10 Ω/□ after 900°C annealing, indicating the conversion of CoSi phase to $CoSi_2$ phase, the sheet resistance of Co/poly-$Si_{0.79}Ge_{0.21}$ sample increases instead with increasing RTA temperature. As illustrated by X-ray diffraction results, more reduction in Ge content is found in Co($Si_{1-y}Ge_y$) phase with increasing RTA temperature. This leads to the increase of relatively high-resistive CoSi in Co($Si_{1-y}Ge_y$) phase. From Fig. 2, the lowest RTA temperature required to achieve the lowest sheet resistance are ∼700, 900, and >900°C for Co/poly-Si, Co/poly-$Si_{0.91}Ge_{0.09}$, and Co/poly-$Si_{0.79}Ge_{0.21}$, respectively. These values are higher than those of the Co/epitaxial-$Si_{1-x}Ge_x$ case as found in our previous experiment, which are ∼650, 800, and 800°C for Co/Si, Co/$Si_{0.91}Ge_{0.09}$, and Co/$Si_{0.8}Ge_{0.2}$, respectively [13]. These results are intriguing, as it indicates that the reaction of Co and $Si_{1-x}Ge_x$ is influenced by the orientation of the $Si_{1-x}Ge_x$ substrate.

For the reaction between Co and heavily boron-doped poly-$Si_{1-x}Ge_x$, boron may redistribute in the reacted region during RTA annealing and affect the Co/$Si_{1-x}Ge_x$ interaction. Fig. 3 shows the SIMS depth profile of Co/poly-$Si_{0.79}Ge_{0.21}$ sample annealed at 850°C. Because of the low solubility of boron in Co silicide [12], the boron atoms could be released from the consumed $Si_{1-x}Ge_x$ region, and accumulate near the silicide surface, as illustrated in the Fig. 3. It is worthy to note here that, although the boron concentration is reduced within the silicide region, its concentration still remains high enough in the unreacted poly-$Si_{1-x}Ge_x$ ($\sim 1 \times 10^{20}$ cm^{-3}) layer. This is extremely important, as it is necessary to avoid poly-gate depletion effect for poly-$Si_{1-x}Ge_x$-gated MOS transistor applications. Furthermore, a weaker surface accumulation of Ge atoms was observed in Fig. 3 than in Fig. 1, this is due to either resolution limitation of SIMS apparatus or the relatively higher Ge content of unreacted films in Fig. 3. In addition, the Ge content near the poly-$Si_{1-x}Ge_x$/nitride interface remains essentially unchanged as compared to the as-deposited poly-$Si_{1-x}Ge_x$ film. These features ensure that the threshold voltage is well controlled with the incorporation of Co silicidation process.

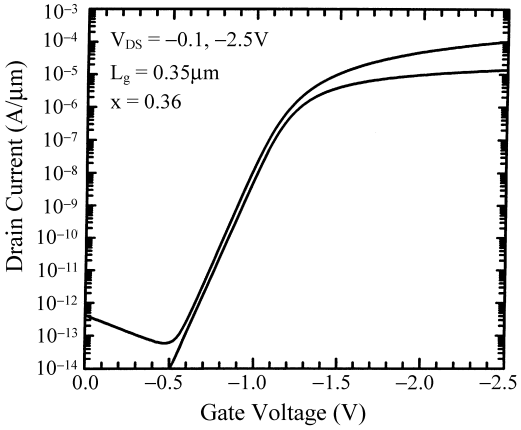

Fig. 4. Transfer characteristics of p-channel MOSFET with Co-salicided poly-$Si_{0.64}Ge_{0.36}$ gate.

The subthreshold characteristics of a typical p-channel MOS transistor with Co-salicided poly-$Si_{0.64}Ge_{0.36}$ gate are shown in Fig. 4. The effective channel length L_{eff} is 0.35 μm for the device. From the figure, the subthreshold slope is found to be approximately 83 mV dec^{-1}, and the drain-induced barrier lowering (DIBL) is approximately 15 mV V^{-1}. The off-state leakage current is less than 10 pA μm^{-1}. These values are essentially the same as those of the device without Co salicidation, an indication that the Co salicidation process does not degrade the device performance. In addition, we have also measured the gate-drain leakage and its value is found to be less than 0.01 pA μm^{-1}, indicating that no bridging occurs between gate and drain (or source). Finally, by comparing the drive current, the device with Co salicide (~0.102 mA μm^{-1} at $V_{GS} = V_{DS} = -2.5$ V) shows a higher drive current than its counterpart without Co salicide (~0.093 mA μm^{-1} at $V_{GS} = V_{DS} = -2.5$ V). This can be explained by the lower source/drain sheet resistance (~15 Ω/□, compared to ~50Ω/□ without Co salicide). Although the higher sheet resistance of Co/poly-$Si_{1-x}Ge_x$ gate, compared to Co/poly-Si, does not affect the DC performance of the device, it may increase the gate delay time. This disadvantage can be overcome by capping a sacrificial Si layer on top of the poly-$Si_{1-x}Ge_x$ film. In this way, the resultant sheet resistance can be lowered by about an order of magnitude, as shown in Fig. 5. In addition, the sheet resistances of Co/poly-Si-gate had comparable values with those of Co/Si-source/drain.

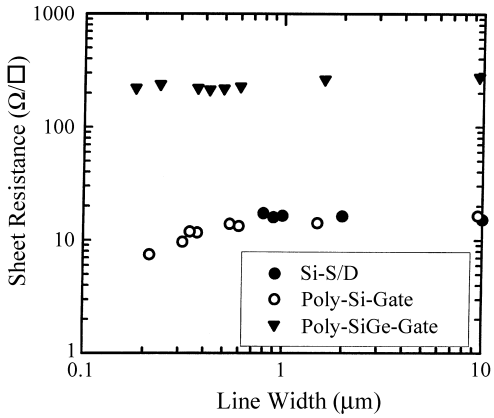

Fig. 5. The dependence of sheet resistance on line width for Co/Si, Co/poly-Si, and Co/poly-$Si_{0.64}Ge_{0.36}$ after 850°C RTA annealing. The thickness of Co was 10 nm.

4. Conclusion

In this paper, a detailed comparison on the Co reaction with poly-$Si_{0.91}Ge_{0.09}$ and poly-$Si_{0.79}Ge_{0.21}$ were studied. The phase sequence in the reaction of Co with poly-$Si_{0.91}Ge_{0.09}$ is found to be $Co(Si_{1-y}Ge_y)$, $CoSi + CoSi_2$, and $CoSi_2$, from 500–700, 800, to 900°C annealing, respectively. However, the phase sequence in the reaction of Co with poly-$Si_{0.79}Ge_{0.21}$ is found to be $Co(Si_{1-y}Ge_y)$, and CoSi from 500–700, to 800–900°C annealing, and no $CoSi_2$ phase is found even after high temperature annealing. The retardation of the $CoSi_2$ phase formation is believed to be due to the Ge atoms segregated to the upper silicide region and the monosilicide (and disilicide) boundaries, as observed from AES analyses. Because of the retardation of $CoSi_2$ phase in higher Ge content samples, the RTA temperature has to be increased to achieve the desired low sheet resistance, which is not compatible with the trend of low thermal budget. This disadvantage, however, can be overcome by employing a sacrificial poly-Si layer on top of the poly-$Si_{1-x}Ge_x$ film for MOS device fabrication. Finally, we have successfully fabricated p-channel poly-$Si_{1-x}Ge_x$-gated MOSFET with Co salicide. The device shows an improved drive current with otherwise the same device parameters, as compared to the device without salicide, presumably due to its lower series resistance.

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