# Differential Capacitance Measurements of Relaxation-Induced Defects in InGaAs/GaAs Schottky Diodes

Jenn-Fang Chen, Nie-Chuan Chen, Jiin-Shung Wang, and Y. F. Chen

Abstract—The use of a differential capacitance technique for characterizing the relaxation-induced defect states in Schottky diodes has been studied. Based on a proposed equivalent circuit including the effect of potential drop across the carrier-depletion layer, a simple equation of capacitance at different voltages and frequencies is derived and compared with experimental data obtained from relaxed In<sub>0,2</sub>Ga<sub>0,8</sub>As/GaAs samples. It is shown that the carrier-depletion layer will introduce capacitance dispersion over frequency like traps; from it the device's geometric parameters, the resistance of the carrier-depletion layer and the ionization energy of the deep level that gives rise to this resistance can be obtained. The relation between the low-frequency capacitance and reverse voltage can be well explained by the depletion of the free carriers between the Schottky depletion and the carrier-depletion layer. The relaxation-induced traps are believed to be at 0.535 and 0.36 eV, respectively, in the GaAs and In<sub>0.2</sub>Ga<sub>0.8</sub>As regions.

Index Terms—Capacitance spectroscopy, deep traps, In-GaAs/GaAs, Schottky diodes.

# I. INTRODUCTION

ATTICE relaxation [1], [2] in InGaAs/GaAs material system has been found to generate misfit dislocations [3]–[8] and give rise to carrier depletion [9], [10]. This carrier depletion is so drastic that it extends beyond the relaxed InGaAs layer to GaAs regions and generates a carrier-depletion region [10]. In order to characterize the relaxation-induced defects, a GaAs Schottky diode with a relaxed InGaAs layer is often used. However, using deep-level transient spectroscopy (DLTS) to analyze the defect traps in such a structure is complicated, since it can not be treated as a simple Schottky diode with traps. Instead, the whole structure is similar to a Schottky depletion region and a carrier-depletion region connected in series [11]. Since admittance spectroscopy is suitable for deriving device's equivalent circuits, it can be used to characterize a device with certain structures. Therefore, in this paper, we present a simple formulation and show how to use capacitance spectroscopy to extract the device's parameters and characterize the relaxation-induced traps in In<sub>0,2</sub>Ga<sub>0,8</sub>As/GaAs system.

Manuscript received December 8, 1999; revised April 19, 2000. This work was supported by the National Science Council, R.O.C., under Contract NSC-87-2112-M-009-022. The review of this paper was arranged by Editor P. K. Bhattacharya.

Publisher Item Identifier S 0018-9383(01)00758-4.

#### II. THEORY

# A. Band Diagram and Equivalent Circuit

We have previously observed a dominating trap at 0.33-0.49 eV in relaxed In<sub>0.2</sub>Ga<sub>0.8</sub>As/GaAs quantum-well Schottky diodes by DLTS measurement [11]. A similar trap at 0.395 eV was also observed by Uchida et al. [9]. This trap is believed to give rise to a carrier-depletion layer around the relaxed InGaAs layer. Based on this information, a proposed band diagram consisting of a Schottky depletion region and a carrier-depletion layer is shown in Fig. 1(a); from it we will derive an equation of differential capacitance as a function of reverse voltage and frequency. Note that under small reverse voltages, there exists a relatively carrier concentrated region between the Schottky depletion and carrier-depletion layer. An incremental reverse potential  $\delta V$  will deplete the free carriers (represented by  $\delta Q_1$ ) at the left edge of the carrier-depletion layer and the free carriers (represented by  $\delta Q_2$ ) in the concentrated region. From Gauss' law, the total incremental potential is given by the sum of the incremental potentials across  $L_1$  and  $L_2$ , as follows:

$$\delta V = \delta V_1 + \delta V_2 = \left(\frac{\delta Q_1}{\varepsilon}\right) L_1 + \left(\frac{\delta Q_1 + \delta Q_2}{\varepsilon}\right) L_2.$$

On substituting  $\delta Q_1 = \varepsilon \delta V_1/L_1$  into the above equation, the ratio of the potential drop across  $L_1$  to the total potential drop can be written by

$$\frac{\delta V_1}{\delta V} = \frac{L_1}{(L_1 + L_2) + \frac{\delta Q_2}{\delta V_1} \frac{L_1 L_2}{\varepsilon}}.$$
 (1)

This equation expresses the potential distribution across the device in terms of the term  $\delta Q_2/\delta V_1$  that accounts for the detailed band structure under different reverse voltages.

# B. C-F Spectra

The ac properties of the device with the band diagram in Fig. 1(a) can be represented by the equivalent circuit in Fig. 1(b). The carrier-depletion layer is assumed represented by a parallel combination of a resistance R and geometric capacitance (per unit area)  $C_1 = \varepsilon/L_1$ , here  $\varepsilon$  is the permittivity of the material and  $L_1$  is the width of the high-resistance layer. The Schottky depletion layer is represented by a depletion capacitance per unit area  $C_2 = \varepsilon/L_2$ , here  $L_2$  is the depletion layer width. The corresponding conductive component is neglected due to a high Schottky barrier height. To include the effect of reverse voltages, we add in the equivalent circuit a steady-state voltage  $V_1$  across

J.-F. Chen, N.-C. Chen, and J.-S. Wang are with the Department of Electrophysics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.

Y. F. Chen is with the Department of Physics, National Taiwan University, Taipei, Taiwan, R.O.C.

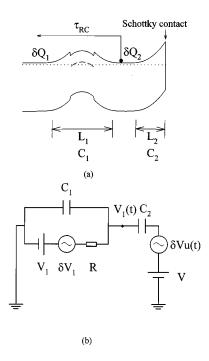


Fig. 1. (a) Proposed band diagram consisting of a Schottky depletion region and a carrier-depletion layer caused by the lattice-relaxation induced trap at about 0.36 eV. (b) Corresponding ac equivalent circuit model including a steady-state voltage  $V_1$  across the carrier-depletion layer at t < 0 due to an applied reverse voltage V.

the carrier-depletion layer at t < 0 due to an applied reverse voltage V. The energy level at the edge of the high-resistance layer is taken as zero reference potential. It is clear that the circuit gives rise to a time constant  $\tau_{RC} = R(C_1 + C_2)$  for the free carriers in the concentrated region to traverse through the carrier-depletion layer. After applying an infinite small voltage  $\delta V u(t)$  at t=0 [where u(t) is a unit step function and is defined as u(t < 0) = 0 and  $u(t \ge 0) = 1$ ], the voltage drop across the carrier-depletion layer can be written in the form:  $V_1(t) = V_1 + [A \exp(-t/\tau_{RC}) + B]u(t)$ , where constants A and B are to be solved from the initial and final conditions. From the partition of capacitor voltage, the initial condition for  $V_1(t)$  is  $V_1(t=0) = V_1 + C_2/(C_1 + C_2) \delta V$ . The final condition is determined by assuming an additional infinite small steady-state voltage of  $\delta V_1$  across the carrier-depletion layer at  $t=\infty$ , that is,  $V_1(t=\infty)=V_1+\delta V_1$ . By substituting these two conditions,  $V_1(t)$  is given by

$$V_1(t) = V_1 + \left[ \left( \frac{C_2}{C_1 + C_2} \delta V - \delta V_1 \right) \cdot \exp(-t/\tau_{RC}) + \delta V_1 \right] u(t).$$

From the voltage across  $C_2$  which is simply given by  $V_2(t) = V + \delta V u(t) - V_1(t)$ , the current flowing through the device becomes

$$i(t) = C_2 dV_2(t)/dt$$

$$= \frac{C_2}{\tau_{RC}} \left[ \left( \frac{C_2}{C_1 + C_2} \delta V - \delta V_1 \right) \exp(-t/\tau_{RC}) \right] u(t)$$

$$+ \frac{C_1 C_2}{C_1 + C_2} \delta V \delta(t)$$

where  $\delta(t)$  is a unit impulse function and is defined as  $\delta(t) = du(t)/dt$ . The frequency-dependent capacitance  $C(\omega)$  and  $G(\omega)$  can be determined from the Fourier transform of i(t):

$$C(\omega) = \frac{1}{\delta V} \int_0^\infty i(t) \cos(\omega t) dt$$
$$= C_2 \left( \frac{C_2}{C_1 + C_2} - \frac{\delta V_1}{\delta V} \right) \frac{1}{1 + \omega^2 \tau_{RC}^2} + \frac{C_1 C_2}{C_1 + C_2}$$
(2)

and

$$G(\omega) = \frac{\omega}{\delta V} \int_0^\infty i(t) \sin(\omega t) dt$$
$$= \frac{\omega^2 \tau_{RC} C_2 \left(\frac{C_2}{C_1 + C_2} - \frac{\delta V_1}{\delta V}\right)}{1 + \omega^2 \tau_{RC}^2}.$$

Note that the frequency behavior in these equations is similar to that in conventional Schottky diodes with traps [12]. Therefore, the effect of the free carriers in the concentrated region to traverse through the carrier-depletion layer is to produce a step-like capacitance drop over frequency.

Equation (2) shows that the capacitance drops from the low-frequency capacitance of  $C_L = C_2(1-\delta V_1/\delta V)$  to the high-frequency capacitance of  $C_1C_2/(C_1+C_2)$ . The inflexion frequency at which the capacitance drops is given by  $\omega_{\rm inf.}=1/R(C_1+C_2)$ . At high frequencies where  $1/\omega \ll R(C_1+C_2)$ , no free carriers can follow the frequency to traverse through the high-resistance layer, thus  $\delta Q_2=0$  so that the high-resistance layer behaves as a perfect insulator and the device acts as the series sum of  $C_1$  and  $C_2$ . The high-frequency capacitance allows us to determine  $L_1+L_2$  and the inflexion frequency allows us to find the temperature dependence R(T) and the ionization energy of the deep level that gives rise to this resistance. On substituting the previously derived  $\delta V_1/\delta V$  from (1), the low-frequency capacitance becomes

$$C_L = \varepsilon \frac{1 + \frac{\delta Q_2}{\delta V_1} \frac{L_1}{\varepsilon}}{L_1 + L_2 + \frac{\delta Q_2}{\delta V_1} \frac{L_1 L_2}{\varepsilon}}.$$
 (3)

## C. Variation of $C_L$ versus Reverse Voltage

1) Under Small Reverse Voltage: Note that (3) is a function of  $\delta Q_2/\delta V_1$  which depends on reverse voltages. Under small reverse voltages such that the band structure on both sides of the carrier-depletion layer still remains symmetric, the concentration in the concentrated region is close to the background concentration  $n(6\times 10^{16}~{\rm cm^{-3}})$ . Under this condition, most of the applied potential will drop only across the Schottky depletion region ( $\delta V_1=0$ ) and deplete the carriers in the concentrated region approximately by reducing its width l, that is  $\delta Q_2\approx qn\,\delta l$ , thus, we obtain  $\delta Q_2/\delta V_1\to\infty$  and the low-frequency capacitance reduces to the Schottky depletion capacitance, that is,  $C_L(V\to 0)\approx \varepsilon/L_2=C_2$ . Therefore, under small reverse voltages,  $C_L$  decreases with increasing reverse voltages in a way similar to that in a simple Schottky diode. This low-frequency capacitance allows us to obtain the Schottky depletion width,

the barrier height, and the carrier concentration in the concentrated region by differentiating  $1/C_L^2$  with reverse voltage.

- 2) Under Intermediate Reverse Voltage: Upon increasing the reverse voltage, some of the applied potential will drop across the carrier-depletion layer, which can drastically deplete the carriers in the concentrated region. Let us approximate the carriers in the concentrated region as  $Q_2 \approx qnl = qN_Ce^{-(E_C-E_F)/kT}l$ , here  $N_C$  is the effective density of states in the conduction band. Assuming that the variation of  $Q_2$  is dominated by the variation in  $E_C-E_F$  from the voltage drop across the carrier-depletion layer, that is,  $\delta V_1 = (1/q)\,\delta(E_C-E_F)$ , we obtain  $\delta Q_2/\delta V_1 = -qQ_2/kT$  which gives  $Q_2 \propto e^{-qV_1/kT}$  after integration. This equation describes that  $\delta Q_2/\delta V_1$  exponentially decreases with increasing the voltage drop across the carrier-depletion layer. Consequently,  $C_L$  will show a drastic variation with increasing reverse voltage.
- 3) Under Large Reverse Voltage: Under large reverse voltages, almost all  $Q_2$  are depleted and the concentrated region no longer exists, thus,  $\delta Q_2/\delta V_1 \to 0$ . From (3), the low-frequency capacitance approaches the high-frequency capacitance, that is,  $C_L(V \to \infty) \approx \varepsilon/(L_1 + L_2)$ .

#### III. EXPERIMENTAL

# A. Sample Fabrication

The sample structure is a  $0.6~\mu m$ -thick n-type GaAs Schottky diode inserted in the middle with an  $\rm In_{0.2}Ga_{0.8}As$  layer of 100, 200 and 1000 Å, respectively. The samples were grown on n<sup>+</sup> — GaAs (001) substrates by Varian Gen II molecular beam epitaxy. All the GaAs and InGaAs layers were doped with Si at a nominal concentration of  $6\times 10^{16}~\rm cm^{-3}$ . This concentration allows us to penetrate the Schottky depletion edge to the InGaAs layer by applying reverse voltages. Details of growth were reported previously [10]. Schottky contacts were fabricated by evaporating Au with dot diameter of 1500  $\mu m$ . An HP4194 gain-phase analyzer was used to measure the capacitance—frequency (C–F) spectra. The small signal oscillation level was maintained at 100 mV.

# B. Experimental C-F Spectra

Fig. 2(a) shows the apparent carrier concentration converted from capacitance-voltage (C-V) data (shown in the inset) for all three samples. A carrier confinement was found in the quantum-well region in the samples with 100 and 200 Å-thick InGaAs. On the other hand, carrier depletion was seen in the sample with 1000 Å-thick InGaAs. The carrier depletion is so drastic that it extends beyond the well region into the GaAs layers and is believed to be caused by lattice relaxation since 1000 Å is much larger than the reported critical thickness of between 200 and 300 Å determined from x-ray diffraction [10]. This lattice relaxation gives rise to step-like capacitance drops over frequency as can be seen in the capacitance-frequency (C-F) spectra at V = -1 V in Fig. 2(b). For comparison, curves in the inset are the C-F spectra for the samples with 100 and 200 Å-thick InGaAs, which show no detectable capacitance drop. For the time being, let us concentrate on the high-frequency capacitance drop from  $\sim 1.2$  to  $\sim 0.4$  nF

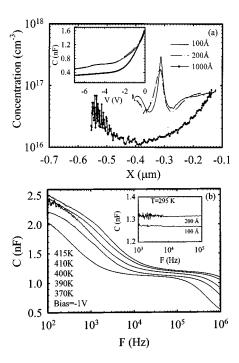


Fig. 2. (a) Apparent carrier concentration converted from C-V data shown in the inset for samples with 100, 200 and 1000 Å-thick InGaAs layers. Carrier depletion can be seen in the 1000 Å sample. (b) The C-F spectra measured at V=-1 V for the 1000 Å sample. For comparison, curves in the inset are the C-F spectra for the 100 and 200 Å samples.

observed in the 1000 Å sample. We intend to show that it is produced by the effect of carriers  $Q_2$  traversing through the carrier-depletion layer as expressed in (2).

# C. Variation of $C_L$ and $C_H$ versus Reverse Voltage

Fig. 3(a) and (b) shows the detailed temperature-dependent high-frequency capacitance drop measured at V = -0.5 V and -2.5 V, respectively, for the 1000 Å sample. For comparison with the theory, we denote the capacitance measured at  $\sim 10^2$ Hz as the low-frequency capacitance  $\mathcal{C}_L$  and the capacitance measured at  $\sim 10^6$  Hz as the high-frequency capacitance  $C_H$ . Their values (at T = 300K) are plotted as a function of reverse voltages in Fig. 4. It can be seen that  $C_H$  slightly decreases with increasing reverse voltages, which is consistent with the previously discussed formula:  $C_H = C_1 C_2/(C_1 + C_2) = \varepsilon/(L_1 + C_2)$  $L_2$ ). From  $C_H \approx 400 \text{ pF}$  (at  $\sim 0 \text{ V}$ ), we obtain  $L_1 + L_2 = 0.51$  $\mu$ m, and from  $C_H \approx 300 \text{ pF}$  (at V = -8 V), we obtain  $L_1+L_2=0.68\,\mu\mathrm{m}$  which is close to the total epitaxial thickness of 0.7  $\mu$ m. As for the low-frequency capacitance,  $C_L$  decreases initially like a simple Schottky diode from 1600 pF (at V = 0 V) to about 600 pF, beyond that, it displays a significant variation corresponding to the onset of drastic depletion of the carriers  $Q_2$ . When carriers  $Q_2$  are completely depleted,  $C_L$  approaches the high-frequency capacitance of about 400 pF. This shows that the behavior of  $C_L$  versus reverse voltage is consistent with the theory. The fact that a Schottky barrier height of  $0.8\,\mathrm{eV}$  obtained from the intercept of  $1/C_L^2$  with voltage axis, as shown in the inset of Fig. 4, also confirms that  $\mathcal{C}_L$  is approximately equal to  $C_2$  for small voltages. From its 0 V value, we obtain  $L_2 = 0.13$  $\mu$ m. In conjunction with  $L_1 + L_2 = 0.51 \ \mu$ m (at  $V = \sim 0 \ V$ ), we obtain  $L_1=0.38~\mu\mathrm{m}$ , which is much larger than the InGaAs

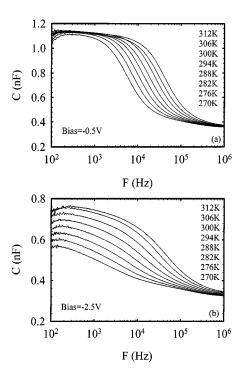


Fig. 3. Temperature-dependent capacitance dispersion measured (a) at  $V=-0.5~\rm V$  and (b)  $-2.5~\rm V$ , respectively, for the sample with  $1000~\rm \AA$ -thick InGaAs.

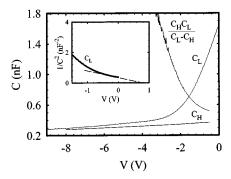


Fig. 4. Low- and high-frequency capacitance  $C_L$  and  $C_H$  (at  $T=300\,\mathrm{K}$ ) as a function of reverse voltages for the sample with 1000 Å-thick InGaAs. A Schottky barrier height of  $\sim$ 0.8 eV was obtained from the intercept of  $1/C_L^2$  with voltage axis as shown in the inset.

thickness of 0.1  $\mu$ m, implying the carrier depletion extends into the GaAs regions. Assuming equal depletion on both sides, we obtain a thickness of  $\Delta l=0.3-(0.13+0.14)=0.03~\mu$ m for the concentrated region at 0 V.

The (2) illustrates that the capacitance drops at the inflexion frequency given by  $\omega_{\inf} = 1/R(C_1+C_2)$ . By fitting this equation to the experimental C–F spectra, the R can be obtained if  $C_1$  and  $C_2$  are first determined. From the experimental  $C_H$  and  $C_L$ , one can obtain  $C_1$  from

$$C_1 = \frac{C_H C_L}{C_L - C_H} - \frac{\varepsilon}{\left(\frac{\delta Q_2}{\delta V_1}\right) \frac{L_1^2}{\varepsilon}}.$$
 (4)

This equation shows that  $C_1$  is equal to  $C_H C_L/(C_L - C_H)$  only for small voltages  $(\delta Q_2/\delta V_1 \to \infty)$ . For large voltages, due to a strong decrease in  $\delta Q_2/\delta V_1$ ,  $C_H C_L/(C_L - C_H)$  will accordingly increase sharply with reverse voltage, as shown in

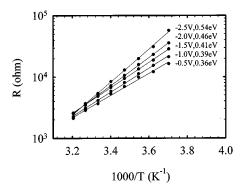


Fig. 5. Resistance versus 1000/T obtained by the high-frequency inflexion frequency from the sample with 1000 Å-thick InGaAs. The activation energy was found to increase from 0.36 eV to 0.54 eV from V=-0.5 to -2.5 V.

Fig. 4. This result also confirms that the term  $\delta Q_2/\delta V_1$  decreases sharply with increasing the reverse voltage.

As to obtain  $C_2$ , as previously mentioned,  $C_2$  is equal to  $C_L$ under small reverse voltages. At small voltages,  $C_L$  is simply the Schottky depletion capacitance that is determined by the carrier concentration in the concentrated layer. However, the concentrated layer contains a large amount of traps as is reflected by the carrier depletion in Fig. 2(a). Due to the trap capture, the free carrier concentration was found to reduce significantly when the measurement temperature is lowered. Fig. 3 shows the decrease of  $C_L$  with lowering temperature for the C-F spectra at V = -2.5 V. In contrast,  $C_L$  is almost temperature-independent at V = -0.5 V. This result can be explained by the presence of a higher concentration of traps in the region close to the InGaAs layer. This decrease of  $C_L$  would result in an overestimation of the emission time from the inflexion frequency, leading to an erroneous estimation of the activation energy. This effect is shown in Fig. 5 for the obtained R versus 1000/T for several reverse voltages. As can be seen, the R increases monotonously with increasing reverse voltages at low temperature while the Rremains almost a constant at high temperature. This effect leads to an increase of activation energy from 0.36 to 0.54 eV as reverse voltage increases from 0.5 to 2.5 V. Therefore, we should take 0.36 eV for the activation energy of R. Assume R is limited by the conduction from the thermal excitation of electrons to the conduction band, this result suggests that Fermi energy is located at 0.36 eV below the minimum of the conduction band in the InGaAs layer. Assuming a single accepter trap is responsible for the carrier depletion which produces the R, this trap should be at about 0.36 eV in the InGaAs layer.

As previously shown, the carrier depletion extends to the GaAs region, meaning that the trap is not confined in the InGaAs layer but extends to the concentrated region. As previously discussed, under small voltages, the applied potential drop is almost across the Schottky depletion region and the carrier-depletion region has almost no effect on capacitance. Therefore, we selected a small voltage sweep from 0 to -0.5 V for DLTS measurement to probe the GaAs layer in the concentrated region. The DLTS spectra were taken with a fill time of 5 s and the result is shown in Fig. 6. As can be seen, a dominating signal at about 270 to 300 K was observed in the 1000 Å sample. As shown in Fig. 6, no similar DLTS signal was

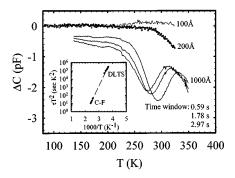


Fig. 6. DLTS spectra measured for the samples with 100, 20, and 1000 Å-thick InGaAs layers. The fill time was set for 5 s. Data were taken after sweeping a voltage from 0 to -4 V for the 100 and 200 Å samples and from 0 to -0.5 V for the 1000 Å sample. The time window was 0.59 s for the 100 and 200 Å samples. The obtained emission times for the 1000 Å sample are consistent with those obtained from the low-frequency inflexion frequencies in the C-F spectra as shown in the Arrhenius plot in the inset.

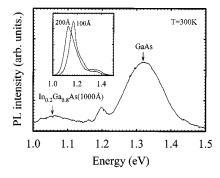


Fig. 7. PL spectra at 300 K for the sample with 1000 Å-thick InGaAs layer. Shown in the inset are the PL spectra at 300K for the 100 and 200 Å-thick InGaAs layers.

detected in the 100 and 200 Å samples where the DLTS spectra were taken after sweeping the voltage from 0 to -4 V. The activation energy and capture cross section were determined to be 0.535 eV and  $1.1 \times 10^{-16}$  cm<sup>2</sup>. As shown in the Arrhenius plot in the inset of Fig. 6, the emission times obtained from DLTS could be connected almost by a straight line with those from the low-frequency capacitance drop (from  $\sim 2.5$  to  $\sim 1.2$ nF) in the C-F spectra in Fig. 2(b). This result seems to suggest that the low-frequency capacitance drop in the C-F spectra originates from the carrier emission from the trap in the concentrated region. These emission times should correspond to the trap emission times because they are much longer than the RC time constant previously mentioned. The activation energy obtained indicates that the trap locates at 0.535 eV in the GaAs region, which is about 0.175 eV larger than the activation energy (0.36 eV) of R. We found that this difference is approximately equal to the conduction-band offset between GaAs and In<sub>0.2</sub>Ga<sub>0.8</sub>As. Fig. 7 shows the 300 K photoluminescence (PL) for the 1000 Å sample. For comparison, the PL spectra at 300 K for the 100 and 200 Å samples are shown in the inset, where strong InGaAs peaks at around 1.17 and 1.13 eV were observed with their intensities being one order of magnitude higher than that of the GaAs peaks. In contrast, the InGaAs peak was much weaker than the GaAs peak for the 1000 Å sample. The reduced intensity also supports the relaxation of the InGaAs layer for the 1000 Å sample. As shown in Fig. 7, an energy difference of 0.26 eV between the GaAs and  $In_{0.2}Ga_{0.8}As$  peaks at 300 K was obtained for the 1000 Å sample. Taking a ratio of 7:3 between the conduction- and valence-band offset [13], a conduction-band offset about 0.18 eV was obtained. This may explain a difference of 0.175 eV for the activation energies obtained in the InGaAs and GaAs layers.

## IV. CONCLUSIONS

The characterizations of relaxation-induced traps for  $In_{0.2}Ga_{0.8}As/GaAs$  Schottky diodes using capacitance spectroscopy technique were investigated. A simple procedure for deriving a C–V–F equation is described. It is shown that at low voltages, the low-frequency capacitance is equal to the Schottky depletion capacitance; at high voltages, it approaches the high-frequency capacitance. The experimental data were shown to be compatible with the theory, allowing us to obtain the device's parameters. The activation energy of 0.36 eV was determined for the resistance of the relaxation-induced depletion layer, implying the presence of a trap at about 0.36 eV in the InGaAs layer. A dominating trap at 0.53 eV was detected in the GaAs region by DLTS. This energy difference could be explained by the conduction-band offset between GaAs and  $In_{0.2}Ga_{0.8}As$ .

# REFERENCES

- J. W. Mattews, S. Mader, and T. B. Light, "Accommodation of misfit across the interface between crystals of semiconducting elements or compounds," *J. Appl. Phys.*, vol. 41, pp. 3800–3804, 1970.
- [2] R. People and J. C. Bean, "Calculation of critical layer thickness versus lattice mismatch for Ge<sub>x</sub>Si<sub>1-x</sub>/Si strained-layer heterostructures," *Appl. Phys. Lett.*, vol. 47, pp. 322–324, 1985.
- [3] I. J. Fritz, P. L. Gourley, and L. R. Dawson, "Critical layer thickness in In<sub>0.2</sub>Ga<sub>0.8</sub>As/GaAs single strained quantum well structures," *Appl. Phys. Lett.*, vol. 51, pp. 1004–1006, 1987.
- [4] P. J. Orders and B. F. Usher, "Determination of critical layer thickness in In<sub>x</sub> Ga<sub>1-x</sub> As/GaAs heterostructures by X-ray diffraction," *Appl. Phys. Lett.*, vol. 50, pp. 980–983, 1987.
- [5] M. J. Joyce, M. Galand, and J. Tann, "Observation of interface defects in strained InGaAs-GaAs by photoluminescence spectroscopy," *J. Appl. Phys.*, vol. 65, pp. 1377–1379, 1989.
- [6] M. Gal et al., "Observation of compressive and tensile strains in In-GaAs/GaAs by photoluminescence spectroscopy," Appl. Phys. Lett., vol. 53, pp. 113–115, 1988.
- [7] G. P. Watson et al., "The measurement of deep level states caused by misfit dislocations in InGaAs/GaAs grown on patterned GaAs substrates," J. Appl. Phys., vol. 71, pp. 3399–3407, 1992.
- [8] J. Zou and D. J. H. Cockayne, "Misfit dislocations generated from inhomogeneous sources and their critical thicknesses in a InGaAs/GaAs heterostructure grown by molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 70, pp. 3134–3136, 1997.
- [9] Y. Uchida, H. Kakibayashi, and S. Goto, "Electrical and structural properties of dislocations confined in a InGaAs/GaAs heterostructure," J. Appl. Phys., vol. 74, pp. 6720–6725, 1993.
- [10] P. Y. Wang et al., "Transition of carrier distribution from a strained to relaxed state in InGaAs/GaAs quantum well," J. Appl. Phys., vol. 85, pp. 2985–2897, 1999.
- [11] J. F. Chen *et al.*, "Carrier depletion by defects in relaxed In<sub>0.2</sub>Ga<sub>0.8</sub>As/GaAs Schottky diodes," *J. Appl. Phys.*, vol. 87, pp. 1369–1373, 2000.
- [12] M. Missous and E. H. Rhoderick, "A simple method of modeling the C-V profiles of high-low junctions and heterojunctions," *Solid-State Electron.*, vol. 28, pp. 233–237, 1985.
- [13] J. Y. Marzin, M. N. Charasse, and B. Sermage, "Optical investigation of a new type of valence-band configuration in In<sub>x</sub> Ga<sub>1-x</sub> As-GaAs strained superlattices," *Phys. Rev. B*, vol. 31, pp. 8298–8301, 1985.

**Jenn-Fang Chen** received the B.S. and M.S. degrees in electronic engineering from the National Chiao Tung University (NCTU), Hsinchu, Taiwan, R.O.C., in 1979 and 1981, respectively, and the Ph.D. degree in electrical engineering from the State University of New York at Buffalo, in 1989.

In 1989, he joined AT&T Bell Laboratories, Murray Hill, NJ, where he worked on MBE growth of compound semiconductors. In 1991, he joined the Electrophysics Department, NCTU. His current research interest is in the field of photoelectronic devices.

 $\mbox{\bf Nie-Chuan Chen},$  photograph and biography not available at the time of publication.

Jiin-Shung Wang, photograph and biography not available at the time of publication

Y. F. Chen, photograph and biography not available at the time of publication.