Characterization of Hot-Hole Injection Induced SILC and Related Disturbs in Flash Memories

Cherng-Ming Yih, Zhi-Hao Ho, Mong-Song Liang, *Member, IEEE*, and Steve S. Chung, *Senior Member, IEEE*

***Abstract*—In this paper, we have proposed a new method for the study of disturb failure mechanisms caused by stress induced leakage current (SILC) in source-side erased flash memories. This method is able to directly separate the individual components of SILC due to either carrier charging/disharging in the oxide or the positive charge/trap assisted electron tunneling into the floating gate. In addition, the present method is very sensitive with capability of measuring ultralow current ($<10^{-19}$ A). Results show that, at *low oxide field*, the disturb is mainly contributed by the so-called charging/disharging of carriers into/from the oxide due to the capacitance coupling effect. While at *high oxide field*, the positive charge/trap assisted electron tunneling induced floating-gate charge variation is the major cause of disturb failure.**

***Index Terms*—Flash memory, gate-disturb, read-disturb, SILC.**

I. Introduction

FOR THE scaling of tunnel oxide in flash memories, the most critical reliability issue is the disturb failure which is caused by stress-induced oxide leakage current (SILC) [1]–[6]. SILC is due to the oxide damage generation after program/erase cycles. Several conduction mechanisms for SILC have been reported recently, such as sequential electron tunneling via trapped positive charge [7], [8], thermal-assisted electron tunneling via weak spot of interface [9], sequential electron tunneling via neutral electron traps [10]–[14], and carrier charging and discharging of stress generated oxide traps [15], [16].

In a certain design of flash memory using source erase, band-to-band tunneling (BBT) induced hot-hole injection during erase has been recognized as the major cause of disturb failure. The hot-hole injection in the vicinity of source junction will generate both positive oxide charges (Q_{ox}) and neutral oxide traps (Q_t) in the oxide. These oxide damage will result in disturb failure in two ways. One is the oxide charge fluctuation due to carrier charging and discharging in the oxide. The other one is the floating gate charge fluctuation due to sequential electron tunneling via neutral traps (trap-assisted tunneling, TAT) or trapped positive charges (charge-assisted tunneling, PCAT). For the tunnel oxide scaling study, the verification of disturb failure mechanisms becomes indispensable. However, there is still in lack of an efficient method to achieve this goal so far. There are two major difficulties. One is the extremely small current level of SILC ($<10^{-10}$ A/cm^2 for $T_{ox} = 100$ Å) which cannot be measured directly on flash memory cells. Although capacitors are widely used for the study of SILC, it cannot reflect the actual leakage currents occurring during the operation of small size flash cells. The other one is in lack of a method to separate the individual effects of carrier charging/disharging and PCAT/TAT on the cell disturb characteristics.

In this paper, the mechanisms of disturb failure due to band-to-band tunneling induced hot-hole injection in source-side erased flash memories are investigated. Section II describes the cell specifications. Basic mechanisms associated with the SILC is introduced in Section III. A new method to characterize SILC and its correlation with read/gate disturb will be described in Section IV. This method is based on the measurement of device threshold voltage (V_{TH}) and gate-induced drain leakage (GIDL) before and after the disturb. Section V are the results and discussion. A summary and conclusion are given in the final section.

II. Device Preparation

A conventional stacked-gate flash memory cell was used in this study which was fabricated by 0.35 μm CMOS technology. The test cells have gate length $L = 0.5$ μm, gate width $W = 0.7$ μm, tunnel oxide thickness $T_{ox} = 100$ Å, and effective interpoly dielectric thickness with ONO structure $T_{ono} = 185$ Å. The source and drain with MDD structure is performed by phosphorus implant with dosage of 2.5E15 cm^{-2} and energy of 35 KeV. Moreover, the n+ source and drain are formed by arsenic implantation with dosage of 5E15 cm^{-2} and energy of 60 KeV. The gate coupling ratio is calculated to be about 0.6. In addition, dummy cells (width $= 20$ μm, and $L = 0.5$ μm) with connected control gate and floating gate are also used for characterization purpose.

III. Mechanisms of Stress-Induced Leakage Current

SILC is an increase in gate oxide leakage current resulting from the application of a stress voltage or current. It is the most important issue for the scaling of gate oxide thickness since it will limit the scaling of flash memory cell tunnel oxide. Fig. 1 shows an example of the SILC effect for thin gate oxide devices. After the stress, a significant increase in gate oxide leakage current appears. This current increase is primarily observed when the applied oxide field is less than the field E_{FN} as labeled, where the FN current starts. It can be seen that the relative increase in current is not strongly dependent on the oxide field (gate oxide field less than E_{FN} which is about 3 MV/cm for a

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C.-M. Yih, Z.-H. Ho, and S. S. Chung are with the Department of Electronic Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

M.-S. Liang is with TSMC, Hsinchu, Taiwan, R.O.C.

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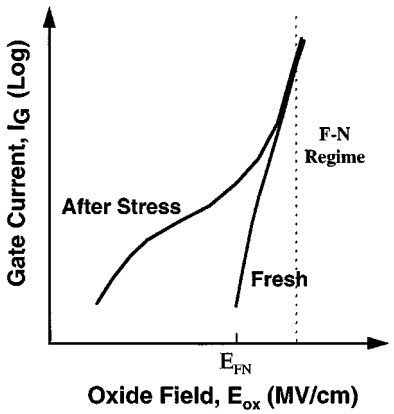

Fig. 1. Stress induced leakage currents before and after the hot carrier stress. After the stress, a significant increase in gate oxide leakage current appears.

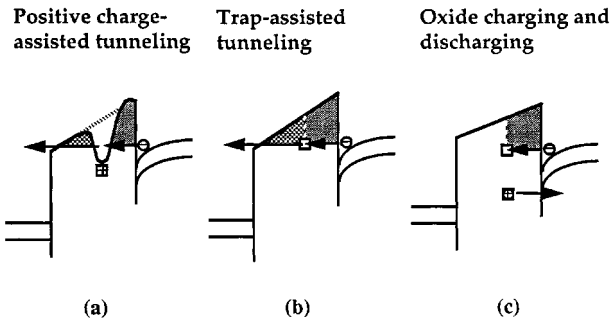

Fig. 2. Carrier conduction mechanisms of stress-induced leakage current for source-side erased flash cells after program/erase cycles. (a) Positive charge-assisted electron tunneling (PCAT). (b) Trap-assisted electron tunneling (TAT). (c) Oxide charging and discharging of stress generated oxide traps.

MOSFET in Fig. 1). The SILC effect diminishes as the device enters F-N conduction.

In the past, several conduction mechanisms for SILC have been proposed. Fig. 2 illustrates three major possible mechanisms. First, Fig. 2(a) shows the mechanism of sequential electron tunneling via trapped positive charges [7]. The trapped positive charges can be caused either by the hole generation due to electron impact ionization in the oxide or by the hot-hole injection initiated by band-to-band tunneling. These generated positive charges in the oxide will reduce the tunneling barrier and enhance the tunneling probability.

Fig. 2(b) is the sequential electron tunneling via neutral electron traps [10]–[14]. As the trap density generated within the oxide increases with stress time duration, there is a higher probability for direct electron tunneling into trap sites near the cathode. For thin oxides, there is also a high probability of direct tunneling out of trap sites into the anode and steady-state current flows when there is an equilibrium between trap filling and emptying processes. As the oxide thickness increases, the initial SILC is higher than the steady-state value since a large fraction of the traps remain filled for long periods of time. For even thicker oxides, the probability for field emission out of traps is extremely low. Therefore, SILC gradually decays as the trap-filling process is completed.

Fig. 2(c) shows the carrier charging and discharging of stress generated traps inside the oxide [16]. For a device after high-voltage or hot-hole stress, SILC is due to some sort of trap-assisted conduction process [11]. However, following the removal of a low-voltage pretunneling voltage pulse, a discharging current is produced that flows in the opposite direction to the low-level leakage current. This discharging current contains the same number of charges as does the SILC. The SILC can be better explained by a model in which stress-generated traps are being tunnel charged during the application of low-voltage pretunneling voltages and discharged following the removal of the voltages. Hence, the traps responsible for the transient charging and discharging currents appear to exist near both oxide interface in approximately equal numbers.

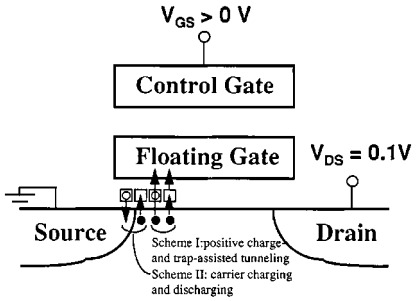

Fig. 3. Two different physical schemes responsible for the steady state and transient components of SILC.

For a source erased flash cell, according to the previous study [6], SILC is contributed by the transient component due to electron trapping into the oxide and trapped hole emission from the oxide, as well as by the steady-state component due to trap-assisted electron tunneling and positive charge-assisted electron tunneling. Therefore, based on the above three different mechanisms, as shown in Fig. 3, we categorize the above three leakage current components into two schemes. Scheme I includes case a) PCAT and case b) TAT (corresponding to the steady-state component) in Fig. 2. Scheme II includes the oxide charging and discharging (corresponding to the transient component). Both schemes will induce a certain amount of SILC in the tunnel oxide of flash memory cell depending on the applied oxide field.

IV. New Characterization Method for SILC and Disturb Study

To study the mechanisms of SILC-induced disturb in the source-side erased memory cell, the method to separate the contributions of SILC due to either scheme I or scheme II will be introduced in this section.

The measurement steps of a new method can be explained in Fig. 4(a) and (b). Fig. 4(a) is the measurement condition. In Fig. 4(b), the I_{DS}–V_{GS} characteristics of dummy and flash memory cells were measured before and after the disturb, from which V_{th} can be determined. Here, the threshold voltage is defined as the gate voltage required to achieve drain current of 1 μA at $V_{DS} = 0.1$ V. For the disturbed flash cell, the cell V_{th} increases since carriers trapped/detrapped (electrons/holes) in the oxide and/or electrons are tunneled into the floating gate by PCAT/TAT. In addition, the increase of V_{th} for dummy cells is due to the flat-band voltage shift by carrier charging/disharging or due to the mobility degradation by the generation of interface states. The difference of the threshold voltage before and after

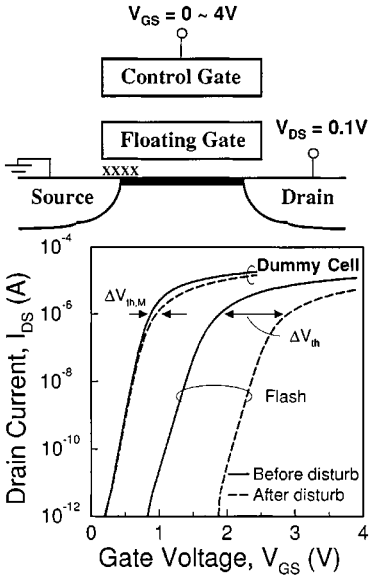

Fig. 4. (a) Measurement conditions for flash memory cells. (b) Measured I_{DS}–V_{GS} characteristics before and after disturb for a dummy cell and a flash memory cell. The dummy cell has the connected control gate and floating gate.

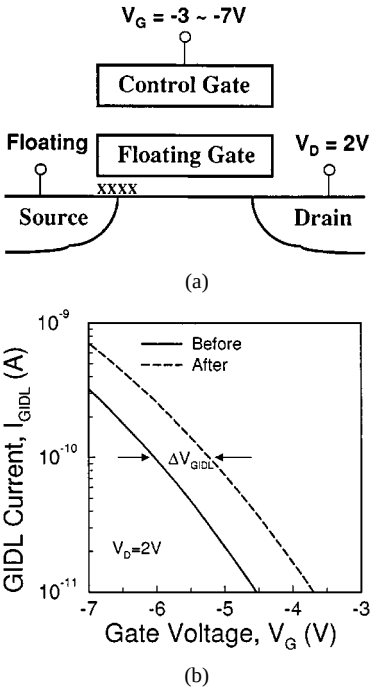

Fig. 5. (a) Bias conditions for GIDL measurement. (b) Measured GIDL currents at the drain side before and after disturb for determining the source-side SILC-induced threshold voltage shift.

disturb is denoted as ΔV_{th} for flash memory cells and $\Delta V_{th,M}$ for dummy cells as given in Fig. 4(b).

In order to separate the effect of carrier charging/disharging and PCAT/TAT on the threshold voltage shift of flash memories, the drain-side GIDL currents [Fig. 5(b)] of flash memories before and after disturb are also measured with measurement condition given in Fig. 5(a). During GIDL current measurement, the source electrode is floating [as illustrated in Fig. 5(a)] and therefore the charging/disharging effect in the vicinity of source junction during disturb can be ignored (since only oxide trap charge exits at the source side due to the hot hole injection during erase). The voltage shift of GIDL current is only due to the effects of floating gate charge variation caused by PCAT/TAT. The voltage shift of GIDL currents is denoted as $\Delta V_{\rm GIDL}$. That is, the PCAT/TAT gives rise to an increase of negative floating gate charges.

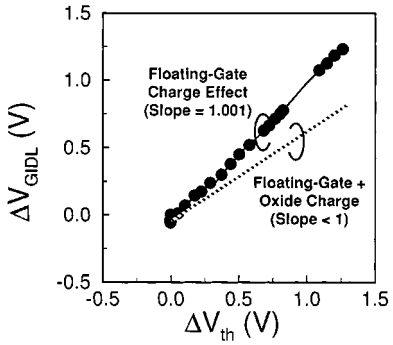

Fig. 6. Correlation between $\Delta V_{\rm GIDL}$ and ΔV_{th} measured in Figs. 4(b) and 5(b), respectively.

If there is no oxide trap charge generated in the oxide near the source, the ΔV_{th} versus $\Delta V_{\rm GIDL}$ slope equals to one (shown in solid circles in Fig. 6). In other words, the floating gate charge variation has the same effect on ΔV_{th} and $\Delta V_{\rm GIDL}$. From the charge-balance equation, the correlation between the floating gate charge variation, ΔQ_{FG}, and the two voltage variations, ΔV_{th} and $\Delta V_{\rm GIDL}$, can be expressed as follows:

$$\Delta V_{\rm GIDL} = \frac{\Delta Q_{FG}}{C_{ono}} = \Delta V_{th}. \tag{1}$$

If ΔV_{th} is unequal to $\Delta V_{\rm GIDL}$ (with slope less than 1, dashed line) after the disturb, the difference between ΔV_{th} and $\Delta V_{\rm GIDL}$ is the contribution of disturb due to the effect of carrier charging/disharging (scheme II) at the source side. Therefore, from the threshold voltage shift (ΔV_{th}) and the drain-side GIDL current measurement $(\Delta V_{\rm GIDL})$ before and after the disturb, the individual components of SILC due to carrier charging/disharging in the oxide and PCAT/TAT for a flash memory cell can be separated.

V. Hot-Hole Injection Induced Disturb Failure

For a negative-erased memory cell, erase is generally achieved by applying a negative bias at the control gate and a positive bias at the source. Electrons are tunneled from the floating gate through the tunnel oxide region into the source [17]. In this gated-diode configuration during source Fowler–Nordheim erase (SFN), holes are generated unavoidable by surface-field-induced band-to-band tunneling (BBT) in the source-to-gate overlap region. A significant amount of these holes become energetic while traveling in the deep-depletion region and is injected into the oxide [18]. The hot-hole injection will cause interface state (N_{it}) and oxide charges/traps (Q_{ox}/Q_t). These hot-hole injection induced oxide damage will give rise to severe reliability problems, such as disturbance [2]–[6], overerasing [19], and operation window opening.

The disturb is the change of memory content during read or program operation. The degradation of disturb characteristics is mainly due to the increase of oxide leakage current after

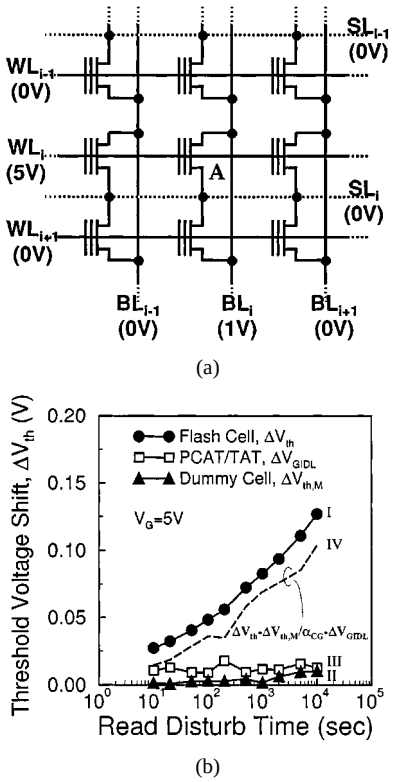

Fig. 7. (a) Cell array structure during read. (b) Individual threshold voltage shift components during disturb at low oxide field.

program/erase cycling of a flash memory cell (stress induced leakage current, SILC). These oxide leakage currents increase with decreasing tunnel oxide thickness. This section deals with the discussion on the characterization of SILC induced read and gate disturbs. Different components of SILC due to scheme I or scheme II will be analyzed.

A. Read Disturb (Low Oxide Field)

Fig. 7(a) shows the read-disturb of a cell A under the read condition, $V_{GS} = 5$ V and $V_{DS} = 1$ V ($E_{ox} = 3$ MV/cm). Prior to the disturb measurement, 10^4 program/erase cycles were performed for cell A by using channel-hot-electron programming (CHE, at $V_{DS} = 5$ V, $V_{GS} = 10$ V) and source-side F–N erase (at$V_S = 7$ V, $V_G = -7$ V, and drain floating) respectively. Fig. 7(b) shows the read disturb characteristics, where curve I is the total ΔV_{th} of flash cells during disturb. Curves II and III are the threshold voltage shift due to flat-band voltage shift/electron mobility degradation ($\Delta V_{th,M}$) and PCAT/TAT (ΔV_{GIDL}) obtained from Figs. 4(b) and 5(b), respectively. Curve IV is obtained by subtracting curves II and III from I. Results in Fig. 7(b) show that, the total ΔV_{th} (curve I) increases with the increase of disturb time and reaches about 0.14 V after the disturb time of 10^4 s. ΔV_{th} is larger than $\Delta V_{th,M}$ and ΔV_{GIDL}.

Based on the observed results, we proposed a new effect, called charge capacitance coupling effect, to explain the disturb failure in such low oxide field regime (read disturb). The mechanism can be illustrated in Fig. 8, where the carrier charging/disharging effect on the flash memory will mainly cause the threshold voltage shift (curve IV) through the capacitive coupling effect, while PCAT/TAT will induce only a

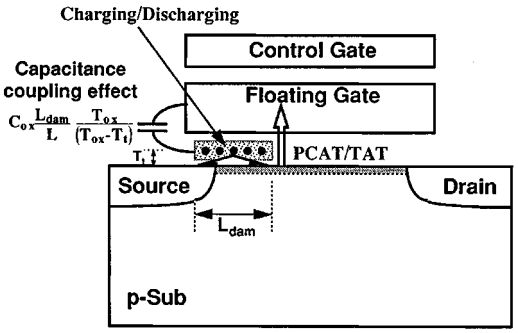

Fig. 8. Schematic illustration of the capacitance coupling effect which is responsible for the disturb failure in low oxide field regime (read disturb).

small amount of V_{th} shift, i.e., curve III (ΔV_{GIDL}) in Fig. 7(b). In Fig. 7(b), we see that the threshold voltage shift due to the capacitance coupling effect is much larger than $\Delta V_{th,M}$ and ΔV_{GIDL}. Therefore, the carrier charging/disharging (scheme II) is the dominant factor for the disturb failure in low oxide field regime (read disturb), while this charging/discharging is made possible by the capacitance coupling effect.

According to the proposed capacitance coupling effect and the charge-balance equation, the threshold voltage shift can be derived quantitatively as follows:

$$\Delta V_{th,ox} = \frac{C'_{ox} + C_{ono}}{C'_{ox} C_{ono}} \Delta Q_{ox} \tag{2}$$

and

$$\Delta V_{th,fg} = \frac{\Delta Q_{fg}}{C_{ono}} \tag{3}$$

respectively. $\Delta V_{th,ox}$ represents curve IV (due to carrier charging/disharging), while $\Delta V_{th,fg}$ represents curve III (due to PCAT/TAT) in Fig. 7(b). Also, ΔQ_{ox} and ΔQ_{fg} are the charge fluctuation *in the oxide and in the floating gate*, respectively. C_{ono} is the capacitance between the control gate and the floating gate. C'_{ox} represents the capacitance in the damage region and can be expressed by

$$C'_{ox} = C_{ox} \frac{L_{dam}}{L} \frac{T_{ox}}{(T_{ox} - T_t)}. \tag{4}$$

Here, C_{ox} is the capacitance in the tunnel oxide of flash memory. L_{dam} and T_t represent the length of damage region and the depth of generated oxide traps above the Si/SiO_2 interface. The value of L_{dam} can be extracted from the gated-diode measurement technique that we developed in [20] (e.g., Fig. 9), where value of $L_{dam} = 0.1$ μm is used. The value of T_t is referred from [21], where $T_t = 3$ nm is used.

Since $\Delta V_{th,ox}$ and $\Delta V_{th,fg}$ can be obtained from the results in Fig. 7(b), the charge variation ΔQ_{ox} and ΔQ_{fg} can then be calculated from (2) and (3). Fig. 9 shows the calculated results of ΔQ_{ox} and ΔQ_{fg} versus disturb time. Obviously, Q_{ox} increases as a function of disturb time but Q_{fg} almost keeps constant. According to previous study [11], it can be explained that at low oxide field regime, electron will tunnel into traps with high probability but with low probability tunnel out of traps. Furthermore, SILC current component due to carrier charging/disharging can be obtained from $\partial Q_{ox}/\partial_t$ as shown in Fig. 10. Due to the weak time dependence of floating

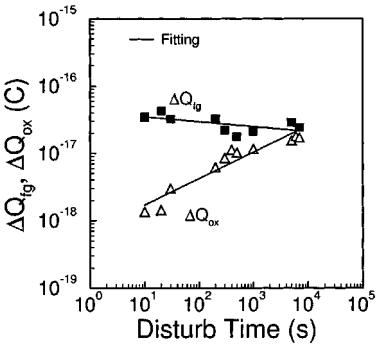

Fig. 9. Time evolution of the calculated floating-gate charges and oxide charges during disturb at low oxide field.

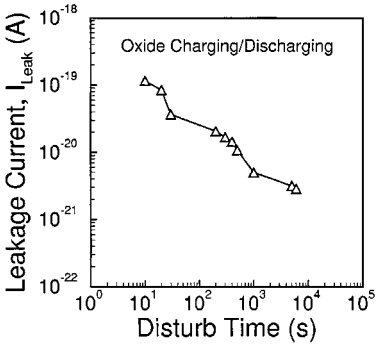

Fig. 10. Time evolution of the calculated SILC component due to oxide charging/disharging at low oxide field.

gate charges (ΔQ_{fg} in Fig. 9), SILC component caused by the PCAT/TAT (scheme I) can be neglected. Therefore, we conclude that the dominant mechanism for the disturb at low oxide field is due to the carrier charging/disharging (scheme II) through the capacitance coupling effect.

B. Gate Disturb (High Oxide Field)

Gate disturb occurs in unprogrammed or erased cells (cell B, C) which are connected to the same word line as the cell that is being programmed (cell A) as shown in Fig. 11. These cells have a low cell threshold voltage initially. During the programming operation, the common word line is connected to a high voltage. The electric field across the bottom oxide becomes high, and may cause tunneling of electrons into the floating gate from the substrate. The threshold voltage of B or C cell will increase, and in serious cases the cell is programmed unintentionally.

For the gate disturb measurements, gate voltage of 8.5 V ($E_{ox} = 5$ MV/cm) is applied and source, drain, and substrate are grounded. The disturb characteristics at high oxide field is shown in Fig. 12. A tremendous increase of ΔV_{th} about 1.3 V (curve I) is observed after disturb time of 10^4 s. From the individual contributions of ΔV_{th} in Fig. 12, we see that PCAT/TAT induced floating gate charge variation (ΔV_{GIDL}, curve II) is responsible for disturb failure at high oxide field. This is quite different from the previous results in Fig. 7(b). Moreover, it is also observed that ΔV_{th} due to carrier charging/disharging (curve III) also increases as a function of disturb time. Based on (2) and (3), the floating-gate and oxide charge fluctuation as a function of disturb time can be calculated as given in Fig. 13. The SILC currents contributed

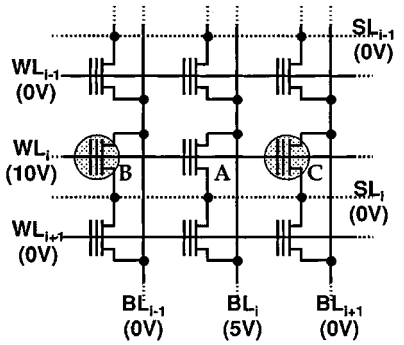

Fig. 11. Cell array structure during programming. Cells B and C are disturbed when high gate bias at word line is applied.

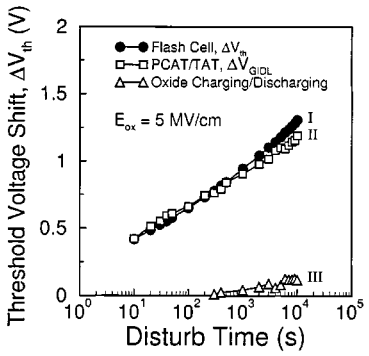

Fig. 12. Individual threshold voltage shift components during disturb at high oxide field.

by oxide charging/disharging and PCAT/TAT are given in Fig. 14. Both SILC components decay with the disturb time. The trap-assisted tunneling component is about two orders higher than the oxide charging/disharging one. Therefore, we conclude that the dominant mechanism for the disturb at high oxide field is due to the PCAT/TAT(scheme I).

C. Discussion

By further looking into the results of Fig. 10, it shows that the observed slope is less than -1. This is different from that of the tunneling front model [16] that people usually used. In the well-known tunneling front model, a fixed gate voltage is applied at the gate of a conventional MOS device such that SILC current is measured. So, the slope of a respective plot in Fig. 10 for an MOS device is equal to -1. In our case of Fig. 10, the simple tunneling front model can not apply since the gate voltage across the tunnel oxide is changing. The cell V_T increases during disturb. In other words, during the disturb, the tunnel oxide field is decreasing as a result of the increase in V_T since floating gate is left floating and there are electron traps as illustrated in Fig. 8. Therefore, the voltage across the tunnel oxide is changing with time such that conventional tunneling front model for a MOS device can not be applied to a flash cell. This is why the present SILC behavior is different from that of simple tunneling front model.

Again, we see that for the case in Fig. 14, where a larger electric field is applied across the tunnel oxide, this high field is considered to be favored for electrons to tunnel through the

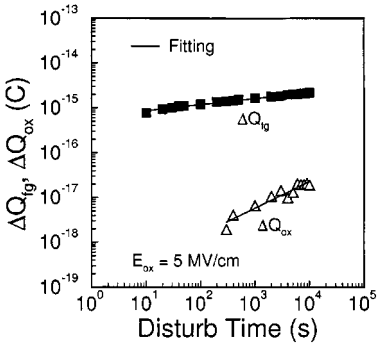

Fig. 13. Time evolution of the calculated floating-gate charges and oxide charges during disturb at high oxide field.

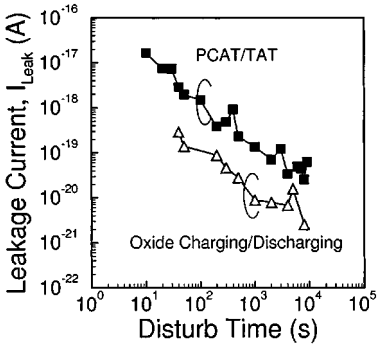

Fig. 14. Time evolution of the calculated SILC component due to oxide charging/disharging and PCAT/TAT at high oxide field.

tunnel oxide via the oxide traps. Therefore, we see a much larger leakage component due to PCAT/TAT as compared to the oxide charging/disharging. On the other hand, owing to a reduction of the tunnel oxide field with time as mentioned, the leakage current decreases with time via the electron traps and the SILC does not have a steady-state component. In contrast, for those measurements of the SILC for MOS devices in reported papers, a fixed gate voltage across the tunnel oxide is used such that normally we see a steady-state component of the SILC when the oxide traps are completely filled after an enough long time.

Valuable information from the comparison of Figs. 10 and 14 can be described as follows. The PCAT/TAT current depends largely on the E_{ox}, while the charging/disharging current depends weakly on E_{ox} [11]. Also, the charging/disharging current is dominant at low oxide field ($E_{ox} = 3$ MV/cm in Fig. 10), while the PCAT/TAT current is dominant at high oxide field ($E_{ox} = 5$ MV/cm in Fig. 14). This implies that there is a critical field between 3 MV/cm and 5 MV/cm, where I_{Leak} of both PCAT/TAT and charging/disharging equals to each other. This critical field, E_{cr}, is a field limit for doing accelerating test of flash cells without causing read-disturb of the cells. The value of E_{cr} depends on the tunnel oxide thickness as well as the P/E cycling conditions. In other words, a field near or larger than 5 MV/cm is not appropriate for the lifetime prediction of read-disturb immunity test since this large field will induce large PCAT/TAT current or large read-disturb, which will give rise to an underestimate of the device lifetime.

VI. Summary and Conclusion

In summary, the oxide-field dependent SILC as well as its related disturbance on source-erased flash memory has been studied by using a new approach. Two mechanisms, the carrier charging/disharging and trap assisted tunneling, will contribute to the stress induced leakage current. Both current components can be clearly identified from the measurement of threshold voltage and GIDL measurements. Two major conclusions can be drawn from this study: 1) The individual contributions of SILC and disturb characteristics due to either carrier charging/disharging in the oxide or PCAT/TAT of electrons into the floating gate can be separated, and 2) a very sensitive measurement of leakage current with ultra-low capability ($<10^{-19}$ A) can be achieved. Moreover, it has been demonstrated that, at *low oxide field*, the disturb is mainly contributed by the so called charging/disharging of carriers into/from the oxide due to the capacitance coupling effect. While at *high oxide field*, the trap-assisted electron tunneling induced floating-gate charge variation is the major cause of disturb failure. This implies that for the accelerating test of flash cells with read-disturb immunity, a large tunnel oxide field (e.g., $E_{ox} = 5$ MV/cm in this work) is not allowed since it will generate large PCAT/TAT current which makes the lifetime prediction be underestimated.

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Cherng-Ming Yih was born in Taiwan, R.O.C., in 1969. He received the B.S. degree in electrical engineering from the National Cheng-Kung University, Taiwan, in 1992, and the Ph.D. degree from the Department of Electronic Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 1999.

Currently, he is a Senior Engineer with the Flash Technology Department, Macronix Inc., Hsinchu, Taiwan. His work is on process technology development for nonvolatile memories.

Zhi-Hao Ho was born in Taiwan R.O.C., in 1975. He received the B.S. degree in electrical engineering from the National Chung-Hsing University, Taiwan, in 1997, and the M.S. degree from the Department of Electronic Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 1999. His M.S. degree was on the modeling and reliability study of flash memory cells.

Mong-Song Liang (S'81–M'84) received the B.S. and M.Sc.degrees from the National Cheng-Kung University, Taiwan, R.O.C., in 1975 and 1977, respectively, and the Ph.D. degree in 1983 from the University of California (UC), Berkeley, all in electrical engineering and computer science. While at UC Berkeley, his research was on the scaling of ultra-thin gate dielectrics, and device reliability physics.

In 1983, he jointed Advanced Micro Devices, Sunnyvale, CA, where he worked on nonvolatile memory technologies (EEPROM and EPROM). From 1988 to 1992, he was with Mosel Electronics Corp, Sunnyvale, where he worked on SRAM technology development. In 1992, he joined Taiwan Semiconductor Manufacturing Company (TSMC). He worked on DRAM and embedded memory technology (Emb-DRAM, Emb-SRAM, and Emb-Flash) development. He was the Director of Memory Division of R&D until 1998. His current assignment is Senior Director of Advanced Module Technology Division of R&D. He is responsible for all advanced modules development, including, etching, thin-film, diffusion, CMP, International Sematech Project, and Cu/low-K interconnect.

Steve S. Chung (S'83–M'85–SM'95) received the B.S. degree (with highest honors) from National Cheng-Kung University, Taiwan, R.O.C., in 1973, the M.Sc. degree from National Taiwan University in 1975, and the Ph.D. degree from the University of Illinois at Urbana-Champaign (UIUC) in 1985, all in electrical engineering. From 1983 to 1985, he was a Research Assistant at the Solid State Electronics Laboratory of Prof. C. T. Sah's group in the Department of Electrical and Computer Engineering, UIUC.

Since August 1987, he has been with the Department of Electronic Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, and has been a Full Professor since 1989. Prior to that, he had ten years of teaching and working experience in both academia and industry. Since 1993, he has also been a Consultant to major semiconductor companies in Taiwan, including Tsmc and MOSEL-Vitellic Inc., Hsinchu. His current teaching and research interests are in the areas of deep-submicron CMOS VLSI technology; Spice device modeling, (TCAD) numerical simulation and modeling of CMOS, SOI, flash EEPROM, and TFTs; characterization and reliability study of state-of-the-art CMOS, and flash EEPROM. He has published more than 120 technical papers in international journals and conferences. He has more than a dozen U.S. and Taiwanese patents.

Dr. Chung has served on various technical program committees of IEEE ASIC Conference, IEEE Symposium on VLSI Technology, International Electron Devices and Materials Symposium (IEDMS, Taiwan), and HPC (High Performance Computing)-ASIA'95. He is the recipient of 1991–1996 Excellent Research Award, and the 1996–1998 Distinguished Research Award from the National Science Council, Taiwan. Currently, he is the Chair of the IEEE EDS Taipei Chapter.