Interface Induced Uphill Diffusion of Boron: An Effective Approach for Ultrashallow Junction

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***Abstract*—This paper investigates anomalous diffusion behavior for ultra low energy implants in the extension or tip of PMOS devices. Transient enhanced diffusion (TED) is minimal at these low energies, since excess interstitials are very close to the surface. Instead, interface induced uphill diffusion is found, for the first time, to dominate during low temperature thermal cycles. The interface pile-up dynamics can be taken advantage of to produce shallower junctions and improve short channel effect control in PMOS devices. Attempts to minimize TED before spacer deposition by inclusion of extra RTA anneals are shown to be detrimental to forming boron ultra shallow junctions.**

***Index Terms*—MOS devices, transient enhanced diffusion, ultrashallow junction, up-hill diffusion.**

I. Introduction

ONE OF THE necessary conditions for sub-0.15 μm CMOS device design is the formation of low resistivity ultrashallow junctions (USJs). Transient enhanced diffusion (TED) of boron induced by ion implantation damage has detrimental effect in USJ's formation. Ultralow energy (ULE) implant reduces TED by placing the dopant and excess interstitials closer to the surface, which is a sink of interstitials [1]. However, extrinsic boron TED can be induced by heavy ion pocket implant, which is required for short channel effect (SCE) control. High concentration [2] or boron-enhanced diffusion (BED) [3] effects are reported to be deleterious for USJs. For ULE implants, high concentration and BED effects are more pronounced because of steep gradient and high concentration of boron. In this work, the influence of these anomalous diffusion behaviors on the extension junction depth is investigated. A new phenomenon, interface induced up-hill diffusion, is observed to play a major role in ultrashallow junctions formation.

II. Interface Induced Uphill Diffusion of Boron

As shown in Fig. 1, a low temperature process on the order of hours at 700 °C (characteristic of a spacer deposition process) shows no TED in the tail region of a 2 KeV, 1×10^{15} cm^{-2} BF_2 implant. This reduction of TED at low energies has been observed before [1]. Instead, a dramatic uphill diffusion occurs because of interface pile-up of dopant during the spacer thermal cycle, leading to a shallower junction after spacer deposition. A large quantity of dopant can be piled-up in a single monolayer at the interface [4], which may be driven there by damage induced point defect gradients [5] or by strain [6] in these extremely high-concentration near-surface profiles.

We used two different CMOS process flows to investigate how this new phenomenon could be used to improve PMOS device characteristics. Both process flows include extra damage from deep arsenic pocket or halo implants before BF_2 extension or tip implantation. Process flow A uses an RTA anneal after pocket and extension implantation to attempt to alleviate TED which might be expected to occur during the low temperature spacer deposition [7]. Process flow B has no RTA anneal after the arsenic pocket and BF_2 extension. Both processes continue with a low temperature spacer deposition and deep source/drain (S/D) RTA anneal.

The attempt to remove the TED induced by pocket and extension damage by a high temperature RTA anneal prior to the low temperature spacer process in process A is shown in Fig. 2. It causes significant thermal diffusion in the high concentration region of the profile. This will be shown to be detrimental to the final junction depth. After RTA, there is minimal diffusion during subsequent spacer deposition, indicating implant damage has been annealed by RTA.

As also shown in Fig. 2, the addition of extra damage by the arsenic pocket implant does give rise to TED in process B during the spacer deposition step. Significant TED occurs only in the tail region below 1×10^{18} cm^{-3}. Even with extra damage present, the formation of boron-interstitial clusters (BIC's) above 1×10^{18} cm^{-3} eliminates the transient diffusion that normally occurs [8]. Interface induced uphill diffusion still occurs above 1×10^{18} cm^{-3} in the near surface region in process B and significantly reduces junction depth in the high concentration region.

Fig. 3 shows final boron profiles after S/D RTA anneals. Process B yields a 425 Å junction depth (determined at 1×10^{18} cm^{-3}) as compared with 507 Å in process A. As is evident, boron in process B does exhibit a shallower junction in spite of the fact that its diffusion distance during the S/D RTA is larger than that in process A. This is due to high concentration or BED effects caused by the steeper gradient existing in process B just before S/D RTA. This larger gradient was in turn created by the uphill diffusion during spacer deposition. It is worth to note that

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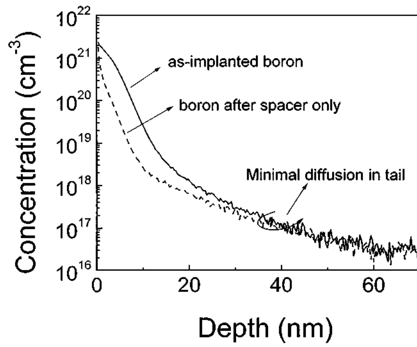

Fig. 1. Boron profiles as-implanted and after spacer deposition.

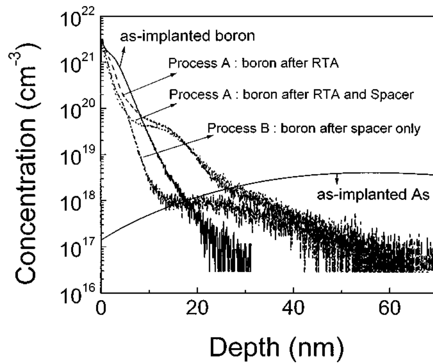

Fig. 2. Boron profiles after each major step for process A and B. The as-implanted arsenic is also shown.

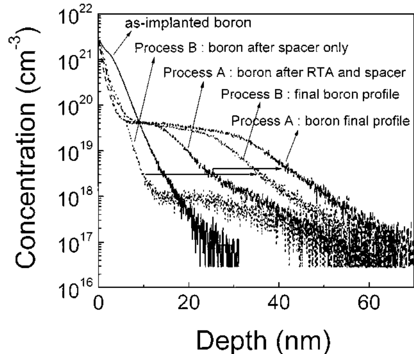

Fig. 3. Boron final profiles after each major step for process A and B.

the diffusion distance due to all the RTA processes alone is the same for both process A and B. Therefore, the reason for final shallower junction in process B is entirely attributed to uphill diffusion. Thus, shallower boron junctions can be fabricated by taking advantage of the anomalous interface-induced uphill diffusion during spacer deposition thermal cycle prior to S/D RTA. The TED that did occur in process B below 1×10^{18} cm^{-3} had no effect on the final junction depth. Consequently, RTA prior to spacer deposition in process A is detrimental to the final junction depth.

III. Device Results

In order to check the effect of interface induced uphill diffusion on device characteristics, devices A and B are fabricated

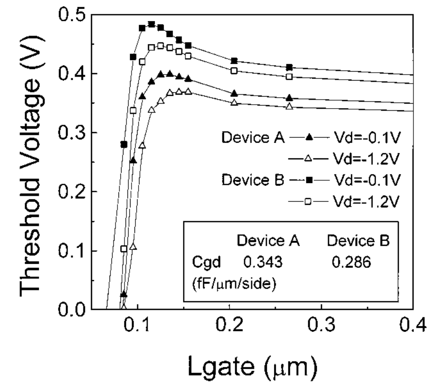

Fig. 4. Threshold voltage roll-off characteristics for device A and B.

by process flow A and B, respectively. The gate oxide thickness is 2 nm, and supply voltage is 1.2 V [9]. Threshold voltage (Vth) roll-off characteristics are compared for device A and B in Fig. 4. Improvement of the short channel effect is achieved by the shallower junction in device B. The gate-drain capacitance (Cgd) is used as an indicator of the amount of lateral diffusion under the gate [10]. In the inset of Fig. 4, Cgd is reduced by the shallower junction in device B, revealing a shallower junction. To improve $Idsat$-$Ioff$ characteristics, reoptimization by higher extension dose and lower pocket dose was done for device B. Given similar Vth roll-off characteristics, substantial series resistance reduction is obtained. As a consequence of the lower series resistance, significant improvement of $Idsat - Ioff$ characteristics is attained in device B. The result is not shown here.

IV. Conclusion

This paper investigates several anomalous diffusion behaviors of ultrashallow junction for ultralow energy implant. TED of boron by ultralow energy BF_2 implant itself is minimal. Arsenic pocket implantation damage does induce boron TED, but it has no impact on the final junction depth. Attempts to minimize TED before spacer deposition by inclusion of extra RTA anneals are shown to be detrimental to forming boron ultra shallow junctions. Interface induced uphill diffusion is found, for the first time, to dominate during low temperature thermal cycles. It can be taken advantage of to produce shallower junctions and consequently improve short channel effect control and $Idsat - Ioff$ characteristics in PMOS devices.

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