# High Quality Interpoly-Oxynitride Grown by  $NH<sub>3</sub>$ Nitridation and  $N_2O$  RTA Treatment

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*Abstract—***In this letter, a method to grow high quality interpolysilicon-oxynitride (interpoly-oxynitride) film is proposed.** Samples, nitridized by  $NH<sub>3</sub>$  with additional  $N<sub>2</sub>O$  annealing and **CVD TEOS deposited on poly-oxynitride (poly-I) with RTA N**2**O oxidation, show excellent electrical properties in terms of very high electric breakdown field, low leakage current, high charge to breakdown, and low electron trapping rate. This novel film is a good candidate for an interpoly dielectric of future high density EEPROM and flash memory devices.**

*Index Terms—***N**2**O, NH**3**, nitridation, oxidation, oxynitride, RTA.**

#### I. INTRODUCTION

**T** HE SCALING down of interpoly dielectrics is critical for next generation nonvolatile memories with a small cell size and low programming voltage. For EEPROM and flash memory devices, the inter-polysilicon oxide demands a high breakdown field and low leakage current to obtain good data retention characteristics. Recently,  $N<sub>2</sub>O$  grown polyoxide film show excellent electrical properties due to its incorporation of nitrogen at the polyoxide/poly-I interface [1]. However, the nonuniform polyoxide film and rough surface morphology of polysilicon/polyoxide interface in inter-polysilicon oxide cause a lower dielectric breakdown field and higher leakage current. It is previously reported using a CVD TEOS oxide deposited on the phosphorus *in-situ* doped polysilicon and  $N_2O$  RTA improves the electrical quality of polyoxide due to smoother interface morphology and incorporation of nitrogen into the polyoxide [2]. In addition, the CMP process achieves a planar surface polysilicon film for polyoxide with a higher electron barrier height and lower electron trapping rate [3]. Therefore, how to reduce the roughness of polysilicon/polyoxide interface and the density of interface defects in the polyoxide become very important topic. However, the  $Si<sub>3</sub>N<sub>4</sub>/polysilicon$  interface is not yet as good as the  $SiO_2$ /polysilicon interface and the density of interface defects is also relatively high. An additional  $N<sub>2</sub>O$  treatment can reduce this interface state and bulk trap densities [4], [5]. In this paper, an interpoly-oxynitride is grown

Manuscript received July 24, 2000. This work was supported by the National Science Council Taiwan, R.O.C., under Contract NSC89-2215-E009-306. The review of this letter was arranged by Editor D. Dumin.

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Publisher Item Identifier S 0741-3106(01)01207-1.



Fig. 1. Cross-sectional view of interpolysilicon-oxynitride film nitridized by  $NH<sub>3</sub>$  and TEOS.

by nitridizing the polysilicon film (poly-I) in  $NH<sub>3</sub>$  with an additional  $N_2O$  treatment, then a CVD TEOS is deposited on poly-oxynitride and applied with  $N_2O$  RTA. Excellent electrical and reliability characteristics are found for this interpoly-oxynitride film.

## II. EXPERIMENTAL

Samples were fabricated on 4-in p-type (100)-oriented silicon wafers. A 5000 Å buffer oxide was thermally grown on the silicon substrate. The poly-Si-I film of 3000 Å thickness was deposited on an oxide in low pressure chemical vapor deposition (LPCVD) system and doped with POCl<sub>3</sub> at 900  $^{\circ}$ C for 30 min, which resulted in a resistivity of 30 to 40  $\Omega/\square$ . A  $Si<sub>3</sub>N<sub>4</sub>$  film was first grown by  $NH_3$  (flow rate is 105 sccm, pressure is 500 mtorr) nitridation of the poly-Si-I layer in LPCVD system at 800  $\degree$ C for 2 h. All samples were immediately annealed in a N<sub>2</sub>O rapid thermal annealing (RTA) treatment at 800  $^{\circ}$ C for 20 s (NO treatment). Then, an inter-polyoxide layer of 65 Å was deposited on the poly-Si-I by tetra-ethyl-ortho-silicate (TEOS) in LPCVD. These samples were rapid annealed in the rapid thermal reactor (950 °C, 30 s, in N<sub>2</sub> or N<sub>2</sub>O ambient). Subsequently, a poly-Si-II of 3000 Å was deposited and doped to obtain a 30 to 40  $\Omega/\square$  resistivity. After the poly-Si-II layer was defined, the samples were thermally grown to 1000 Å by wet oxidation. Contact holes was defined and opened, and Al film was deposited and patterned. Then the wafers were again sintered at 350 °C for 30 min in  $N_2$  ambient, and the capacitor fabrication was finished. A cross-sectional view is shown in Fig. 1. The equivalent oxide thickness  $(E_{OT})$  of an 85 Å interpoly-oxynitride film was obtained from high frequency ca-

 $10<sup>2</sup>$  $10<sup>2</sup>$  $10<sup>1</sup>$  $10<sup>1</sup>$ Positive gate bias Negative gate bias N<sub>2</sub>O Anneal (Control sample)  $10<sup>0</sup>$  $10<sup>0</sup>$ N<sub>2</sub>O Anneal (Control sample) As-deposited  $10<sup>°</sup>$ Current Density  $(A/cm<sup>2</sup>)$ As-deposited Current Density  $(A/cm<sup>2</sup>)$  $10^{-1}$ N<sub>2</sub> Anneal  $N_2$  Anneal  $10^{-2}$  $10^{-2}$ N<sub>2</sub>O Anneal N<sub>2</sub>O Anneal  $10<sup>2</sup>$  $10^{-3}$  $10<sup>°</sup>$  $10^{-4}$  $10^{-5}$  $10<sup>°</sup>$  $10^{-6}$  $10<sup>°</sup>$  $10^{-7}$  $10<sup>°</sup>$  $10^{-5}$  $10<sup>°</sup>$  $10<sup>°</sup>$  $10<sup>°</sup>$  $10<sup>°</sup>$  $10<sup>°</sup>$  $\boldsymbol{0}$  $\overline{c}$  $10<sub>10</sub>$ 12  $16$  $18\,$ 20 8  $\overline{4}$ 6 8 14  $\pmb{0}$  $\overline{\mathbf{c}}$ 4 6 10  $12 \,$ 14 16 18 Electric Field (MV/cm) Electric Field (MV/cm)  $(b)$  $(a)$ 

Fig. 2. The  $J-E$  characteristics of NH<sub>3</sub>-nitridation poly-Si-I film without NO treatment then deposited TEOS with RTA N<sub>2</sub>O anneal (control sample), and films with NO treatment then deposited TEOS with RTA  $N_2$  or  $N_2O$  anneal, with (a) positive bias and (b) negative bias applied to the top gate.

pacitance–voltage (*C–V*). The electrical properties and reliability characteristics of MOS capacitors were measured by using the Hewlett–Packard (HP) 4156B semiconductor parameter analyzer.

#### III. RESULTS AND DISCUSSION

Fig. 2(a) shows positive  $J-E$  characteristics of NH<sub>3</sub>-nitridation poly-Si-I film for control sample (without NO treatment) or with NO treatment, and then deposited TEOS with RTA  $N_2$ or N<sub>2</sub>O annealed at 950 °C for 30 s. It is found that the sample with  $N_2O$  oxidation after  $NH_3$ -nitridation poly-Si-I film with NO treatment shows the highest electric breakdown field among these samples. This leakage current density for capacitors with NO treatment is lower than that of control sample. This result can be attributed to the smoother surface of polysilicon films (AFM not shown, the roughness of  $NH_3$ -nitridation poly-Si-I without NO and with NO treatment are 4.72 nm and 3.98 nm, respectively). In addition, the effective barrier height of the control sample is 2.25 eV and sample with  $N_2O$  oxidation after NH<sub>3</sub>-nitridation poly-Si-I film with NO treatment has an effective barrier height of 3.08 eV. However, from Fig. 2(b), capacitors with TEOS deposited and  $N_2O$  oxidation after NO treatment also exhibit a higher electric breakdown field in the negative  $J-E$ curves than the control sample.

Fig. 3(a) and (b) demonstrate Weibull plots of charge to breakdown  $(Q_{bd})$  of capacitors for control sample, TEOS deposited samples under constant current stress of  $\pm 1$  mA/cm<sup>2</sup>, and deposited TEOS with  $N_2$  annealed or  $N_2O$  oxidation under constant current stress of  $\pm 100$  mA/cm<sup>2</sup>. The deposited TEOS with  $N<sub>2</sub>O$  oxidation after NO treatment has a larger Weibull distribution than control sample for both polarities. This can be explained by the relative difference of roughness between the bottom and top polyoxide/poly-Si interface. The rough interface enhances the localized electric field resulting in a higher leakage current and a lower  $Q_{bd}$ . On the other



Fig. 3. Weibull plots of charge-to-breakdown  $(Q_{bd})$  of control sample, and samples of  $NH_3$ -nitridation poly-Si-I layer with NO treatment and then deposited TEOS with RTA  $N_2$  or  $N_2O$  annealed at 950 °C. with (a) positive bias and (b) negative bias applied to the top gate.

hand, nitrogen atoms are piled-up at the polyoxide/poly-Si-I interface and form a nitrogen-rich layer. Therefore, strained Si–O bonds are replaced with un-strained Si–N bonds and bring about a stronger interface. The charge trapping characteristics of deposited TEOS oxide with and without NO treatment was investigated. Fig. 4 depicts the curves of gate voltage shift versus stress time of the interpoly-oxynitride for both stress types of the control sample and deposited TEOS oxide under a constant  $\pm 1$  mA/cm<sup>2</sup> current stressing, and deposited TEOS oxide with N<sub>2</sub> or N<sub>2</sub>O treatment under a constant  $\pm 100$  $mA/cm<sup>2</sup>$  current stressing. All increase in the gate voltage is examined to be due to electron trapping. In spite of a 100 times larger stressing current, the NO treatment with RTA  $N<sub>2</sub>O$ oxidation of oxynitride shows a much small electron trapping rate than control sample for both polarities. Moreover, the capacitor with NO treatment and RTA  $N_2O$  oxidation exhibits a significantly lower electron trapping rate when electrons are



Fig. 4. Curves of gate voltage shift versus stress time of control sample and deposited TEOS under  $\pm 1$  mA/cm<sup>2</sup> stressing, and deposited TEOS with RTA  $N_2$  or  $N_2$ O annealed at 950 °C under 100 mA/cm<sup>2</sup> stressing on both types.

injected from the poly-Si-I. This means that NO treatment with RTA  $N<sub>2</sub>O$  oxidation of interpoly-oxynitride has fewer electron traps, which may be ascribed to a smoother interface and more nitrogen incorporation at the polyoxide/poly-Si-I interface.

### IV. CONCLUSION

In this paper, we reported a very promising method to obtain a thin interpoly-oxynitride film by NH<sub>3</sub>-nitridation and with a  $N<sub>2</sub>O$  RTA treatment. This interpoly-oxynitride film exhibits excellent reliability properties in terms of high electric breakdown field and barrier height, low leakage currents and low trapping rate. This novel dielectric film appears to be very promising for future EEPROM and flash memory devices.

## ACKNOWLEDGMENT

The authors would like thank all the staff of Semiconductor Research Center, National Chiao Tung University.

#### **REFERENCES**

- [1] C. S. Lai, T. F. Lei, and C. L. Lee, "The characteristics of polysilicon oxide grown in pure N<sub>2</sub>O," IEEE Trans. Electron Devices, vol. 43, pp. 326–331, Feb. 1996.
- [2] C. H. Kao, C. S. Lai, and C. L. Lee, "The TEOS oxide deposited on phosphorus in-situ/POCl<sub>3</sub> doped polysilicon with rapid thermal annealing in N<sub>2</sub>O," *IEEE Trans. Electron Devices*, vol. 45, pp. 1927–1933, Sept. 1998.
- [3] T. F. Lei *et al.*, "Characterization of polysilicon oxides thermally grown and deposited on the polished polysilicon films," *IEEE Trans. Electron Devices*, vol. 45, pp. 912–917, 1998.
- [4] S. C. Song *et al.*, "Ultra thin high quality stack nitride/oxide gate dielectrics prepared by in-situ rapid thermal  $N_2O$  oxidation of  $NH_3$ -nitride Si," in *VLSI Tech. Symp. Dig.*, 1999, pp. 137–138.
- [5] T. M. Pan, T. F. Lei, and T. S. Chao, "Robust ultra-thin oxynitride dielectrics by NH<sub>3</sub> nitridation and N<sub>2</sub>O RTA treatment," IEEE Electron *Device Lett.*, vol. 21, pp. 378–380, Feb. 2000.