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Effect of rapid-thermal-annealed TiN barrier layer on the Pt/BST/Pt capacitors prepared by RF magnetron co-sputter technique at low substrate temperature

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Abstract

This investigation reports the effect of rapid-thermal-annealing (RTA) on metallic barrier TiN against the inter-diffusions of Ti and Si into barium strontium titanate (BST) in Pt/BST/Pt/TiN/Ti/Si capacitors. In the integration of BST capacitors, the thermal budget of the BST deposition would cause the inter-diffusions of Ti and Si from Ti adhesion layer and Si plug respectively. This event would degrade the BST capacitors. To address this issue, rapid-thermal-annealed TiN barriers were deposited between the bottom electrode Pt and adhesion layer Ti. Optimal RTA condition for TiN were found in this experiment. Excellent electrical characteristics of Pt/BST/Pt/TiN/Ti/Si capacitors, including high dielectric constant ($\varepsilon_r = 320$), low leakage current (1.5×10^{-8} A/cm^2) under 0.1 MV/cm, and greater than 10 year lifetime under 1.6 MV/cm were obtained with $Ar + O_2$ mixed ambient at a low substrate temperature (300°C).

Keywords: Barium strontium titanate (BST); Inter-diffusion; Barrier layer; Rapid-thermal anneal (RTA); Low substrate temperature

1. Introduction

One of the most crucial issues for giga era dynamic random access memory (DRAM) has long been maintaining sufficient storage charge in the small memory cell. The adoption of high dielectric constant materials simplifies the cell structure [1–4] and maintains immunity against soft error [5]. Therefore, thin barium strontium titanate (BST) film with a high dielectric constant has attracted great attention for practical use in DRAM capacitors. In addition, the most promising DRAM cell structure for Gbit and greater is the capacitor over bit-line (COB) [2,3,6–8]. Capacitors of COB structure are making use of simple capacitor structures comprised of a high dielectric constant material such as BST with platinum electrodes. This structure, which has the potential to store a sufficient charge for operation as a DRAM memory cell, requires very few fabrication steps and occupies a small area compared to traditional capacitor fabrication processes. Among several deposition methods, RF magnetron co-sputter system was chosen to deposit BST thin films in this work because it is a mature and easily controlled technology for thin film deposition.

In general, to improve the adhesion and the contact properties via $TiSi_x$ formation, the Ti layer was deposited between the bottom electrode Pt and the Si

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substrate [3,9,10]. However, higher leakage current density will be found if the diffusion of Ti atoms from the Ti adhesion layer cannot be suppressed, and the work function of bottom electrode materials decreases due to the interaction of the bottom electrode and the Ti layer. In addition, the Ti adhesion layer may diffuse up to the BST film to react with oxygen and change the chemical composition of BST films. To prevent the electrodes and dielectrics from chemical reaction with poly-Si plug and Ti adhesion layer during BST deposition and post processes, a diffusion barrier was also required. The diffusion barrier TiN has been extensively used in the past. However, the inter-diffusions of Ti and Si are still produced due to the elevated thermal process of BST deposition. While excellent properties have been previously reported for BST films, a systematic study of the effect of rapid-thermal-annealing (RTA) treated TiN on the dielectric and electrical properties of BST capacitor should be required to optimize the process.

In this study, we have investigated the effect of RTA on TiN barrier layer on the resultant BST capacitors. The effect of RTA-treated TiN against the inter-diffusion between Si and Ti atoms has also been extensively examined via electrical and material analyses.

2. Experimental procedure

The major concern of this investigation is to find a proper condition for the TiN barrier layer in order to prevent the inter-diffusion of Si, Pt, Ba, Sr, Ti and O atoms. The structure of Pt/BST/Pt/TiN/Ti/Si was employed to simulate the practical COB DRAM's capacitor structure. The starting p-type silicon wafer was cleaned by the standard Radio Corporation of America (RCA) cleaning process and chemically etched in dilute HF solution. A 50 nm thick adhesion Ti layer was deposited by dc sputtering. Ti was performed by the RTA process at 765°C for 50 s. Each 100 nm TiN layer was then deposited by dc sputtering and treated by RTA for 90 s at 450°C, 525°C, 600°C, and 700°C, respectively. At room temperature, a 200 nm thick metallic Pt was deposited by sputtering, as the bottom electrode. Thus, a Pt/TiN/Ti/Si substrate for the deposition of BST film was prepared.

$(Ba_{0.7}Sr_{0.3})TiO_3$ was deposited by RF magnetron co-sputter system with $Ar + O_2$ mixed ambient at 300–400°C. To control the Ba/Sr ratio of thin BST films by tuning the RF power, $BaTiO_3$ and $SrTiO_3$ targets 4 in. in size were used simultaneously. The sputtering chamber was evacuated to a base pressure of 2×10^{-7} Torr. The deposition pressure of 6.8 mTorr which was maintained by a mixture of argon and oxygen ratio 76:4 with a total flow rate of 80 sccm. The RF powers for the deposition of $BaTiO_3$ and $SrTiO_3$ were 175 and 230 W, respectively. For the study of electric properties, Pt top electrode with a diameter of 150 μm patterned by shadow mask process was deposited on BST film by dc sputtering at room temperature.

Scanning electron microscopy (SEM) was employed to examine the surface morphology, cross-section, and thickness of the BST film. In addition, atomic force microscopy (AFM) was applied to inspect the surface roughness. Also, X-ray diffraction (XRD) analyzed the crystallinity of the barrier layer treated with varying RTA processes, and a four-point probe measured the conductance. The Auger electron spectroscopy (AES) was also conducted to compare the barrier capability of a TiN layer against inter-diffusion during BST deposition. To investigate the impact of inter-diffusion to dielectric properties, the capacitance and the leakage current characteristics were measured.

3. Results and discussion

Fig. 1 illustrates the XRD patterns of thin BST films deposited on (a) Pt/Si, (b) Pt/Ti/Si, as well as (c) and (d) Pt/TiN/Ti/Si, where the TiN layer treated both with and without RTA processing. Serious inter-diffusion occurred in the absence of a TiN barrier, and many undesirable compounds such as the Pt silicides were formed, as can be seen from Fig. 1(a) and (b). Moreover, both Si and Ti atoms diffused from the Si substrate and the Ti adhesion layer to both the BST and Pt layers. The Si and Ti atoms reacted with the bottom electrode Pt, and formed the alloy, which decreased the work function of the bottom electrode. In addition, when the Si and Ti atoms diffused into to BST films, the dielectric characteristics of thin BST films were remarkably degraded. Furthermore, Si atoms reacted with BST to

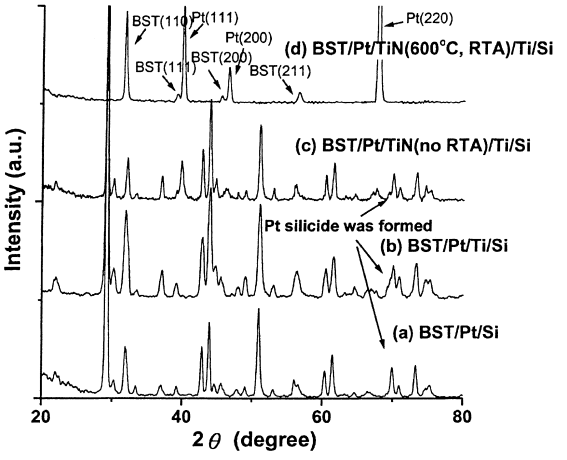

Fig. 1. XRD patterns of thin BST films deposited on (a) Pt/Si, (b) Pt/Ti/Si, as well as (c) and (d) Pt/TiN/Ti/Si with the TiN layer without and with RTA process.

form SiO_2. Ti atoms reacted with the oxygen in BST and altered the chemical composition of BST films. We also observed that the inter-diffusions nevertheless occurred in the TiN barrier that had not received RTA treatment. Fig. 1(c) demonstrates that many undesired compounds were still formed. Only the samples with RTA-treated TiN barrier confirmed no significant $PtSi_x$ peak or other undesirable compounds. Hence, the RTA-treated TiN barrier layer can effectively suppress Si and Ti diffusion.

Fig. 2(a) and (b) demonstrate the AES depth profiles of the BST/Pt/TiN/Ti/Si samples both with and without RTA treatment after the TiN deposition, correspondingly. The TiN barrier layer without RTA treatment depicts serious inter-diffusion of Si, Ti and also Pt atoms, after the thermal budget (400°C, 27 min) of the BST deposition. In addition, only extremely low Ti content is observed on the RTA-treated TiN film. Material analyses can clarify this phenomenon. Fig. 3 depicts that the sheet resistances of the TiN barrier layers are approximately 1.47, 1.42, and 1.40 Ω/square for RTA treatments at 525°C, 600°C, and 700°C, accordingly. RTA treatment on TiN at higher temperatures created better conductive properties. Fig. 4 presents the XRD patterns of TiN annealed at different RTA temperatures. Higher TiN peak can be found in TiN treated with a higher temperature RTA. This implies that high temperature RTA treatment effectively improves the crystallinity of TiN film and thereby enhances the resistance of TiN barrier against inter-diffusion.

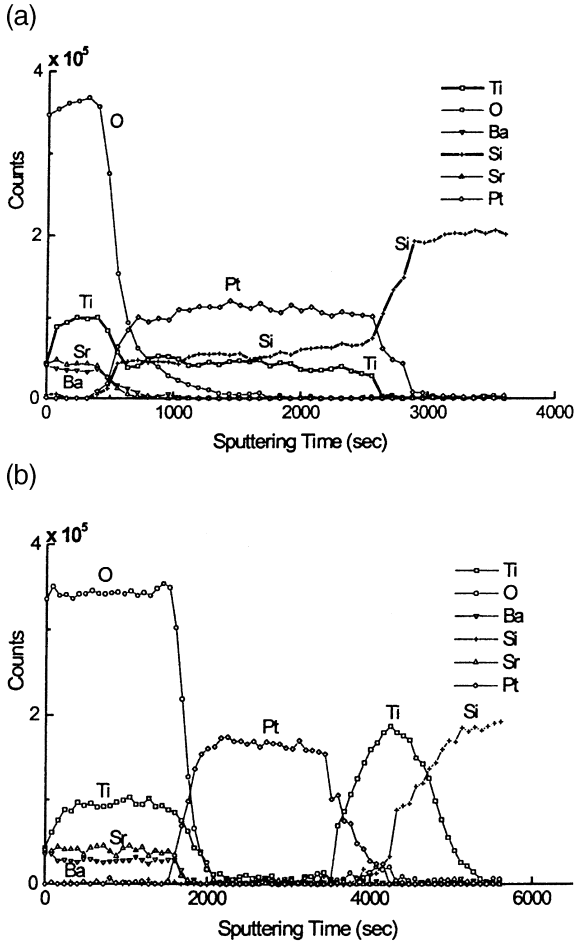

Fig. 2. AES depth profiles for BST/Pt/TiN/Ti/Si structure, where TiN was (a) without RTA and (b) annealed with RTA at 600°C.

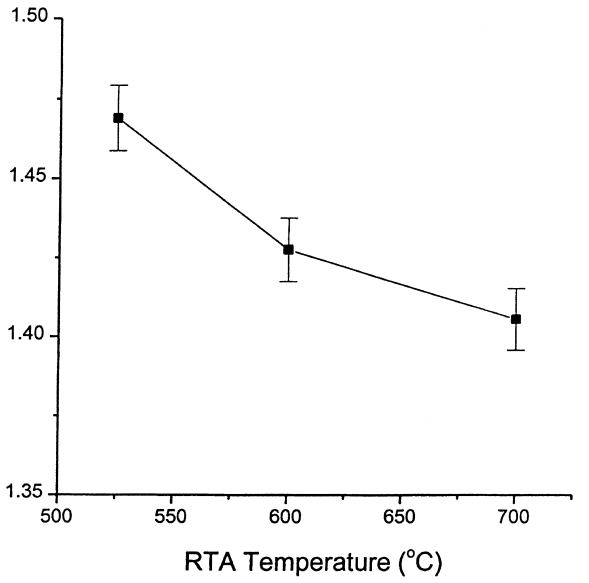

Fig. 3. The sheet resistances of the TiN barrier layers for RTA treatments at 525°C, 600°C, and 700°C.

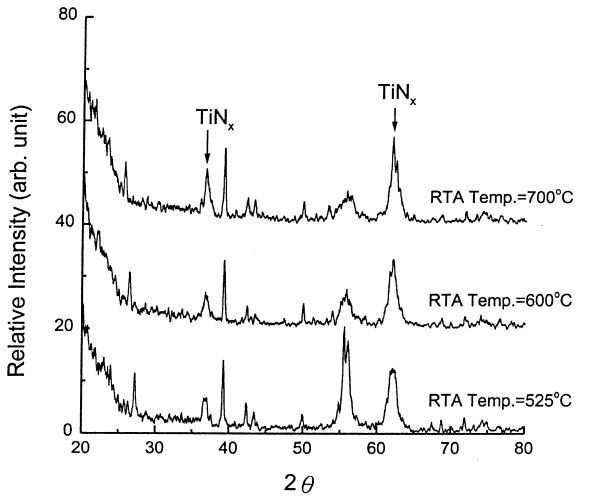

Fig. 4. XRD patterns of TiN annealed at different RTA temperatures.

Furthermore, one unexpected diffraction peak which occurs at the diffraction angle of about 56° (2θ) is suppressed with higher temperature RTA. This peak is conjectured to come from the oxidation of as-deposited Ti before TiN barrier deposition.

Figs. 5 and 6 confirm that both the analyses of crystallinity and conductance corresponded to the results of electrical measurements. Fig. 5 presents the capacitance of the Pt/BST/Pt/TiN/Ti/Si samples with various RTA treated TiN barrier layers. Notably this increases with increasing RTA temperature, and when the RTA temperature is above 600°C the capacitance also becomes saturated. Fig. 6 displays the current–voltage characteristics. For the sample with RTA treatment at 700°C, a higher leakage current was proved. The electrical characteristics were interpreted by AFM observation. The surface morphology of the TiN diffusion barriers with RTA treatments of 600°C and 700°C was also measured by AFM, shown in Fig. 7(a) and (b). These figures confirm that higher leakage current may come from higher surface roughness at 700°C RTA. From these analyses, the root mean square asperity was approximately 6.644 and 8.723 nm for the samples treated by RTA at 600°C and 700°C, respectively. Previous documents [11–13] reported that large surface roughness results in higher leakage current of capacitors. Notably, this is consistent with our electrical measurements. Fig. 8 demonstrates that lifetime extrapolation using constant voltage stress time dependent

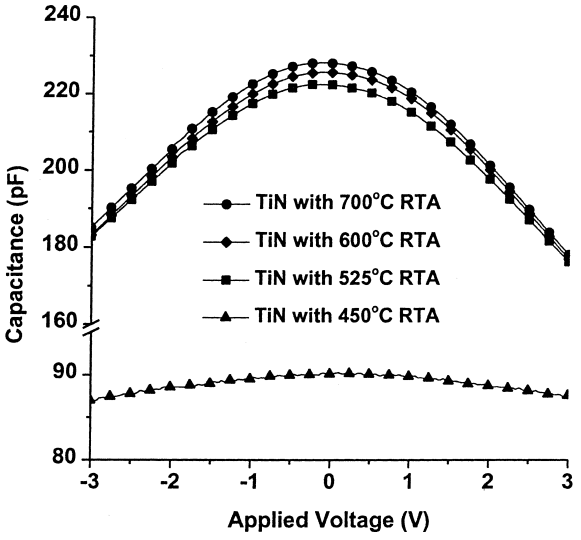

Fig. 5. The relation of capacitance vs. voltage of Pt/BST/Pt with TiN annealed at different RTA temperatures.

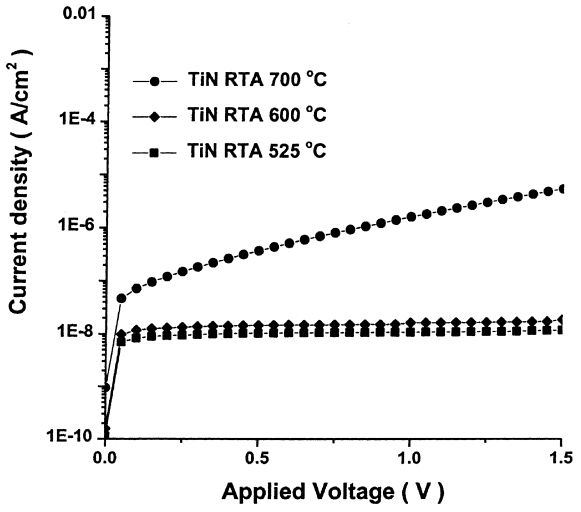

Fig. 6. The relation of leakage current vs. voltage of Pt/BST/Pt with TiN treated by different RTA temperatures.

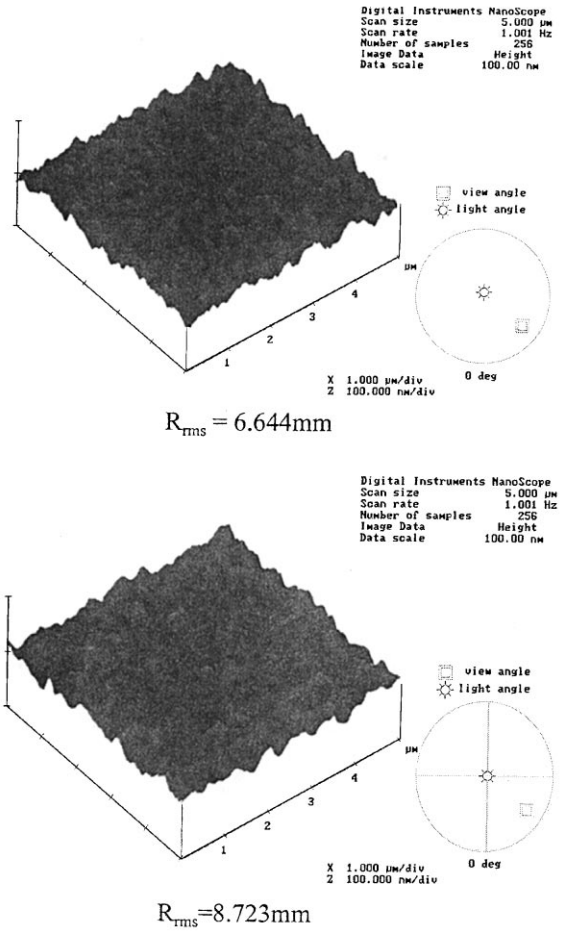

Fig. 7. The surface roughness of Pt bottom electrodes on TiN annealed at (a) 600°C, RTA and (b) 700°C, RTA after BST deposition.

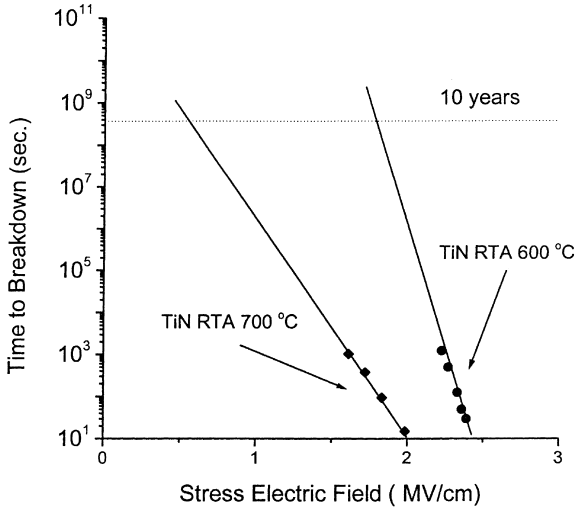

Fig. 8. TDDB characteristic of BST films on Pt/TiN/Ti/Si with TiN treated with different temperature.

dielectric breakdown (TDDB) studies predicts the 10 year lifetime. The leakage current of the RTA-treated samples at 700°C is higher than those at 600°C. The increased leakage current accelerates the electrical degradation of the capacitors. It is shown that the BST films on substrate with smooth surface show greater TDDB, which is similar to that previously reported by Parker and Tasch and Cha et al. [14,15].

Therefore, the 600°C RTA-treated samples have a longer lifetime. However, the temperature of 700°C accelerates degradation than the TiN sample treated with RTA at 600°C.

Consequently, the condition of RTA at 600°C for 90 s may be properly used to treat the TiN barrier layer in order to obtain a thermally, physically stable diffusion barrier with lower leakage current.

4. Conclusions

In this work the RTA effect on the TiN barrier for the Pt/BST/Pt/Ti/Si capacitors was investigated. By annealing the TiN barrier layer, good barrier properties, that is, displaying no serious inter-diffusion and under accurate RTA conditions were obtained. The RTA treatment at 600°C for 90 s improved the crystallinity of TiN and suppressed the formation of unexpected materials. Hence, the resistance of TiN barrier layers against inter-diffusion was effectively enhanced. In contrast, the TiN barrier was not suited for excessively elevated RTA treatments (>700°C). Owing to high roughness asperity of the Pt/TiN surface, which formed during RTA treatment at 700°C, the leakage current increased significantly and dielectric degradation was thereby accelerated.

Acknowledgements

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