Analysis of Temperature Effects on High-Frequency Characteristics of RF Lateral-Diffused Metal–Oxide–Semiconductor Transistors

2008 Jpn. J. Appl. Phys. 47 2650

(http://iopscience.iop.org/1347-4065/47/4S/2650)

Japanese Journal of Applied Physics
Vol. 47, No. 4, 2008, pp. 2650–2655

Analysis of Temperature Effects on High-Frequency Characteristics of RF Lateral-Diffused Metal–Oxide–Semiconductor Transistors

Hsin-Hui HU, Kun-Ming CHEN[1], Guo-Wei HUANG[1], Alex CHIEN[2], Eric CHENG[2], Yu-Chi YANG[2], and Chun-Yen CHANG

Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan
[1]*National Nano Device Laboratories, Hsinchu 300, Taiwan*
[2]*United Microelectronics Corporation, Hsinchu 300, Taiwan*

(Received October 1, 2007; accepted November 16, 2007; published online April 25, 2008)

In this work, the effects of temperature on the DC and RF characteristics of lateral-diffused metal–oxide–semiconductor (LDMOS) transistors were studied. Devices with different layout structures were fabricated using a 40 V LDMOS process. The temperature coefficients of the threshold voltage and channel mobility are negative and their values are similar for devices with fishbone and ring structures. In addition, we found that both the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) decrease with increasing temperature. The variations of f_T with different temperatures are not only affected by the change in transconductance but also affected by the drain resistance. Finally, the temperature behaviors of *S*-parameters were measured, and the ring structure showed less S_{22} variation with different temperatures than the fishbone structure. We extracted the model parameters of the devices to explain this observation. [DOI: 10.1143/JJAP.47.2650]

KEYWORDS: cutoff frequency, layout structure, LDMOS, maximum oscillation frequency, *S*-parameters, temperature

1. Introduction

Lateral-diffused metal–oxide–semiconductor (LDMOS) transistor technology has played a predominant role in wireless base-station applications for frequencies ranging from 450 MHz to 2.7 GHz owing to its advantages in performance, cost, reliability, and power capability.[1)] For high-power applications, temperature is an important issue. The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are critical figures of merit for evaluating the performance of RF transistors. For conventional MOS transistors in RF applications, the temperature effect was investigated by studying the temperature dependence of f_T, which is proportional to the transconductance.[2)] With an increase in temperature, the f_T and f_{max} have been shown to decrease. According to its structure, the parasitic drain resistance of the LDMOS becomes more important than that of the conventional MOS field-effect transistor (MOSFET) for the present drift region. However, in most of the studies, the effect of the parasitic resistance was not considered when analyzing the temperature effect on the device characteristics.[2–4)] By de-embedding the effect of the parasitic source and drain resistors from the measured *S*-parameters, the temperature dependence of the intrinsic f_T can be analyzed. Several researchers have investigated the effects of temperature on the reliability and dc performances of LDMOS transistors.[5–7)] However, the temperature effects on the high-frequency characteristics of LDMOS have seldom been addressed.

In this work, the DC and high-frequency characteristics of LDMOS transistors with different layout structures were studied at various temperatures. From the DC characteristics, we found that fishbone and ring structures have similar variations in threshold voltage and channel mobility for different temperatures. However, the measured *S*-parameters of the two structures show different temperature behaviors. Electrical parameters have been extracted to describe the temperature behavior of the transistors. In addition, the variations of f_T and f_{max} with different temperatures were also investigated. The LDMOS transistors with different layout structures have different drain resistances.[8)] In order to eliminate the effect of drain resistance, the intrinsic f_T was extracted from the de-embedded *S*-parameters. The results of extrinsic and intrinsic f_T variations with temperature are compared.

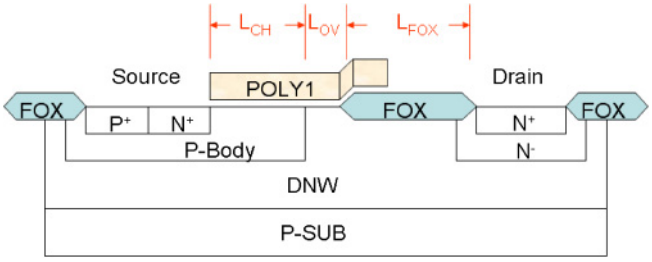


Fig. 1. (Color online) Schematic cross section of an LDMOS transistor.

2. Experiments

The RF LDMOS transistors used in this study were fabricated using a 40 V LDMOS process. The schematic cross section of the device is shown in Fig. 1. The drain region was extended under the field oxide (FOX) and consisted of a lightly doped N-well drift region and an N^- region with higher doping doses for on-resistance control. The source region and the p-body were tied together to eliminate extra surface bond wires to reduce the source inductance and improve the RF performance in a power amplifier configuration.[9)] The gate oxide thickness was 135 Å and the mask channel length (L_{CH}) was 0.5 µm. The drift length ($L_{Drift} = L_{OV} + L_{FOX}$) was fixed at 3.6 µm in this investigation. The LDMOS transistors were designed with two types of layout structures, as shown in Fig. 2. In the "fishbone" structure, all the gate fingers are divided into several subcells, in each of which 6 gate fingers are grouped together with a finger width (L_F) of 10 µm. To achieve a lower on-resistance and a more compact device, we adopted a "ring" structure in the layout design. All the rings were arranged as a 3 × 3 array in one device. In each ring, the source region was surrounded by the drain region, while the

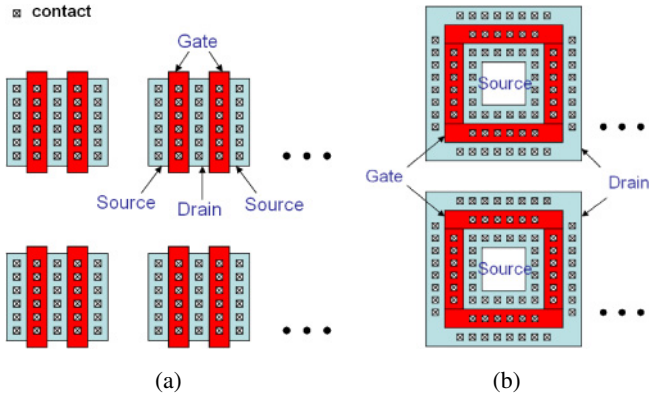


Fig. 2. (Color online) LDMOS layout structures: (a) fishbone and (b) ring.

gate was located between the source and the drain. The width of each gate ring, which is defined at the center of the channel region, was $4 \times 10\,\mu\text{m}$. To compare the performances of the fishbone and ring structures fairly, both structures had the same total channel width ($W = 360\,\mu\text{m}$). Additionally, the contact placement in the ring structure corresponded to that in the fishbone structure. Because the effective width of the drift region in the ring structure is larger than that in the fishbone structure, the ring structure has a lower drain resistance.[8)]

The DC characterization of the test devices was performed using an HP4156 semiconductor parameter analyzer. To characterize the high-frequency performance, the *S*-parameters were measured on-wafer from 0.1 to 10 GHz for different temperatures using an HP8510 network analyzer and then de-embedded by subtracting the OPEN dummy. Different control biases were applied from an HP4142B source measure unit.

3. Results and Discussion

3.1 DC characteristics

The DC characteristics of the LDMOS transistor with different layout structures at 0 and 50 °C are compared in Fig. 3. At low gate voltages ($V_{GS} < 1\,\text{V}$), the transconductance (g_m) and drain current at 50 °C are higher those that at 0 °C owing to the decrease in the threshold voltage. At high gate voltages, because the channel mobility decreases with increasing temperature, the g_m and drain current at 50 °C become lower than that at 0 °C. In low- and medium-bias regions, the ring structure showed a higher drain current and g_m than the fishbone structure. For a high drain bias ($V_{DS} = 28\,\text{V}$), the drain current and extrinsic g_m had zero-temperature-coefficient biases near $V_{GS} = 1.3\,\text{V}$ and $V_{GS} = 1\,\text{V}$, respectively. The zero-temperature-coefficient bias point results from the negative temperature coefficients of both the effective mobility and threshold voltage.[6)]

Figure 4 shows the threshold voltage plotted against temperature. The threshold voltage variations are -1.66 and $-1.68\,\text{mV/°C}$ for the fishbone and ring structures, respectively. The values in the literature vary from -1 to $-4\,\text{mV/K}$ with the most frequently noted value of $-2\,\text{mV/K}$ for the conventional complementary MOS (CMOS).[10)] For the LDMOS transistors, the threshold voltage variation in our study is smaller than the proposed values of $-5.2\,\text{mV/°C}$,[6)] $-3.2\,\text{mV/K}$,[11)] and $-2.8\,\text{mV/°C}$.[12)] This results from the lighter doping in the double-diffused channel.

The extracted channel mobility for different temperatures is shown in Fig. 5. The LDMOS channel mobility was deducted from the first-order one-dimensional model in the

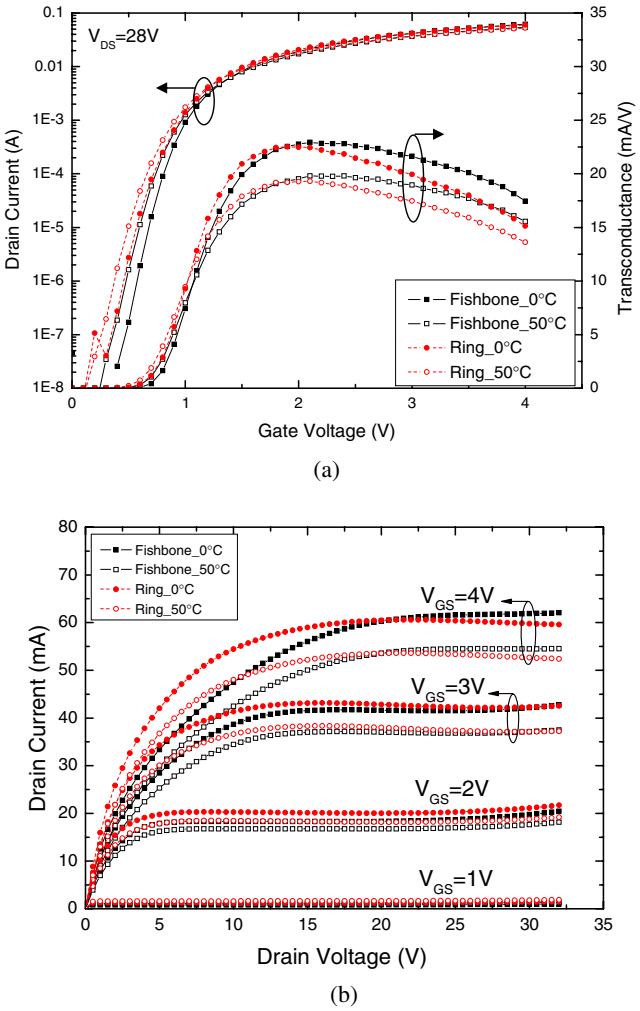


Fig. 3. (Color online) (a) Subthreshold and (b) output characteristics of LDMOS transistors with different layout structures at 0 and 50 °C.

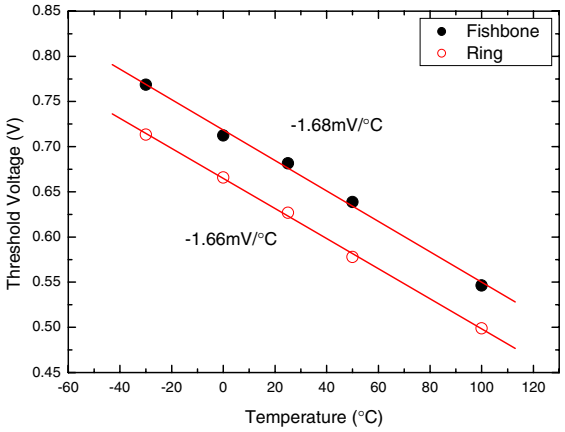


Fig. 4. (Color online) Threshold voltage variation with temperature for different layout structures.

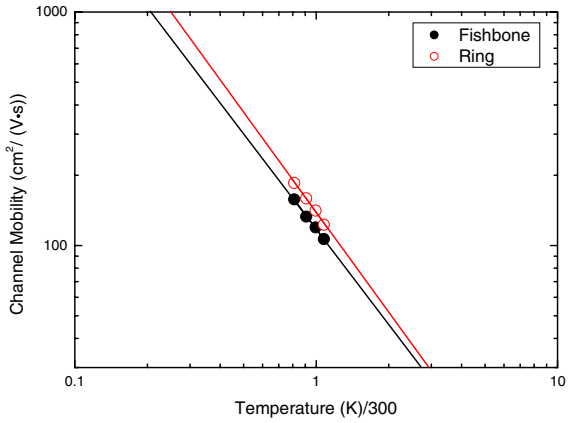


Fig. 5. (Color online) Temperature dependence of channel mobility for different layout structures.

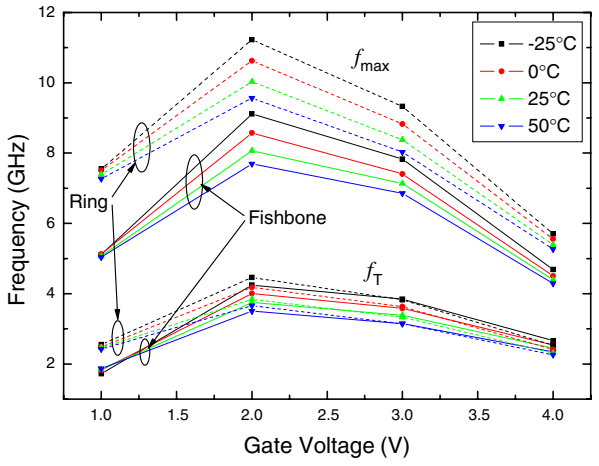


Fig. 6. (Color online) Cutoff frequency and maximum oscillation frequency versus gate voltage at various temperatures.

linear mode.[6] This method is applicable for low drain voltages. The temperature dependence of the channel mobility can be modeled as $\mu = \mu_0 \times (T/T_0)^{-m}$, where $m = -1.35$ for the fishbone structure and -1.36 for the ring structure. For intermediate inversion layer concentrations $[N = (0.5–5) \times 10^{12}\,\mathrm{cm}^{-3}]$ at room temperature, the phonon-scattering-limited channel mobility has been observed to be dependent on N and T ($\mu_{ph} \propto T^{-n}N^{-1/\gamma}$), where $\gamma = 3–6$ and $n = 1–1.5$.[13] Therefore, the mobility in our devices is dominated by the phonon scattering.

3.2 *Cutoff frequency and maximum oscillation frequency*

The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) versus the gate voltage for the LDMOS transistors at various temperatures are shown in Fig. 6. We calculated the maximum stable gain/maximum available gain (MSG/MAG) and short-circuit current gain (h_{21}) from the S-parameters. The f_T and f_{max} were determined to be the frequencies at which the current gain was 0 dB and the MAG was 0 dB, respectively. As shown in Fig. 6, the ring structure has better high-frequency performance than the fishbone structure owing to a lower drain resistance.[8] In addition, both f_T and f_{max} decrease with increasing temperature for the two structures. The degradations of f_T and f_{max} are attributed to the lower g_m, as shown in Fig. 7. The variations in f_T and intrinsic g_m are 17 and 20%, respectively at $V_{GS} = 2\,\mathrm{V}$, as temperature changes from -25 to 50 °C. Because the temperature dependence of f_{max} is also affected by the drain resistance (R_d) and drain–substrate junction capacitance (C_{jdb}), the variation in f_{max} is approximately 15%. It should be noted that the f_T and g_m have zero-temperature-coefficient bias points near $V_{GS} = 1\,\mathrm{V}$. In Fig. 7, at a higher gate voltage, both the intrinsic and extrinsic g_m values of the ring structure are lower than those of the fishbone structure owing to the self-heating effect. Owing to the series resistance, the intrinsic g_m for the two

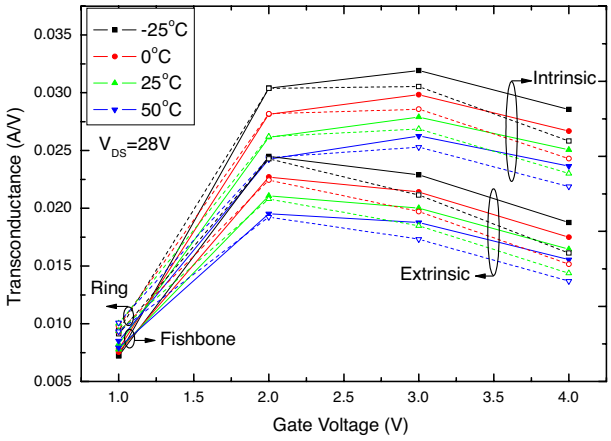


Fig. 7. (Color online) Extrinsic and intrinsic transconductances versus gate voltage at various temperatures for different layout structures.

structures was higher than the extrinsic g_m. The variation in both the intrinsic and extrinsic g_m values are approximately 20% at $V_{GS} = 2\,\mathrm{V}$ as temperature changes from -25 to 50 °C. However, the variation changes to 17% for the fishbone structure and 15% for the ring structure at a high gate voltage ($V_{GS} = 4\,\mathrm{V}$). The higher gate voltage leads to severe surface scattering and lowers the effective mobility. As the gate voltage increases, the effect of surface scattering is more prominent resulting in smaller changes in g_m and also in f_T and f_{max} with temperature.

Figure 8 shows the variations in extrinsic and intrinsic f_T values versus the variation in intrinsic g_m at $V_{GS} = 2\,\mathrm{V}$ when temperature changes from 25 °C. The usual approximate relation of extrinsic f_T and intrinsic g_m can be expressed as follows:[14]

$$f_T = \frac{g'_{m0}}{2\pi\sqrt{(C'_{gs}+C_{gd})^2\left(1+\dfrac{r_d}{R'_{ds} \parallel R'_{sub}}\right)^2 - (g'_{m0}C'_{gs}R'_{gs} - C_{gd})^2}}, \quad (1)$$

where $g'_{m0} = g_{m0}/(1 + g_{m0}R_s)$. The extrinsic f_T in eq. (1) was extrapolated assuming a -20 dB/decade roll-off for the short-circuit current gain $|h_{21}|$. R_{gs} refers to the channel resistance and leads to an additional term related to the g_m in the denominator. The sign of this term in the denominator is negative, making the slope of the extrinsic f_T variation versus the intrinsic g_m variation larger than 1. This is contradictory to our measured results in Fig. 8(a). Moreover, in eq. (1), the small-signal equivalent circuit can be viewed as a dual-feedback circuit in which R_s is the local series–series feedback element and C_{gd} is the local shunt–shunt feedback element.[14] Even though R_s makes the extrinsic g_m smaller than the intrinsic g_m by a factor of $1/(1 + g_mR_s)$, it also decreases C_{gs} and C_{gd} by the same factor and thus should not affect f_T.

In LDMOS, however, the effect of drain parasitic resistance is also important, which is ignored in eq. (1). Tasker and Hughes reported a more rigorous derivation for the short-circuit current gain of a FET that takes source and drain resistance into account:[15]

$$f_T = \frac{g_m}{2\pi\{(C_{gs} + C_{gd}) \cdot [1 + (R_S + R_d)/R_{ds}] + C_{gd} \cdot g_m \cdot (R_S + R_d)\}}, \quad (2)$$

According to eq. (2), the sign of the term related to the g_m in the denominator is positive, making the slope of the f_T variation versus the intrinsic g_m variation smaller than 1. In Fig. 8(a), the extrinsic f_T includes the effects of source and drain resistances and the values of the curve slope are smaller than 1. This might be attributed to the effect of $(R_s + R_d)$ being more prominent than the effect of R_{gs}. Furthermore, the fishbone and ring structures we studied here have difference drain resistances, resulting in the distinct values of the curve slopes in Fig. 8(a). To eliminate the effect of parasitic resistance, the intrinsic f_T was extrapolated after de-embedding the effect of the parasitic resistors from the measured *S*-parameters. As shown in Fig. 8(b), the curve slopes of the intrinsic f_T variation versus the intrinsic g_m variation for the fishbone and ring structures are quite similar (0.95 for fishbone and 0.94 for ring) and approach 1.

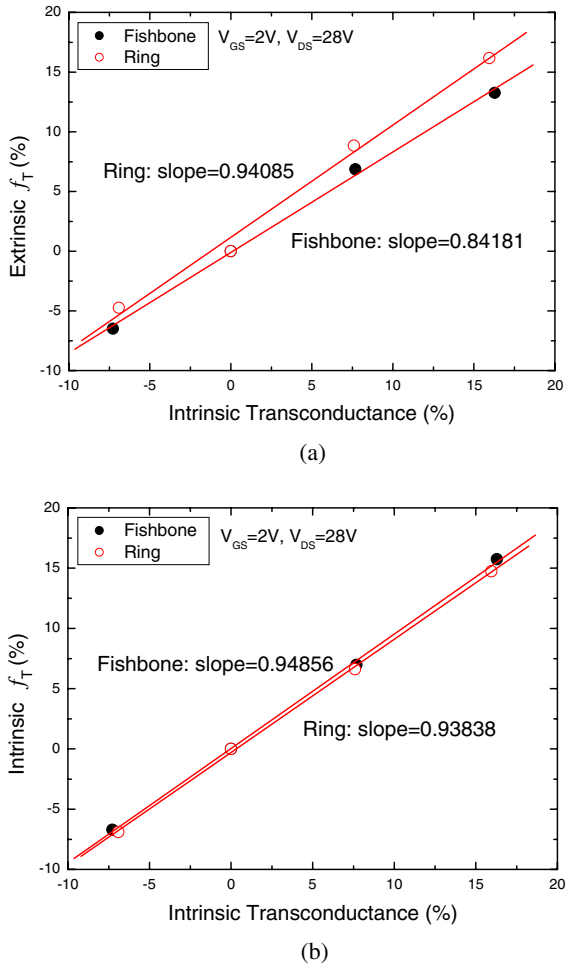


Fig. 8. (Color online) (a) Extrinsic f_T and (b) intrinsic f_T variations versus intrinsic transconductance variation when temperature changes from 25 °C.

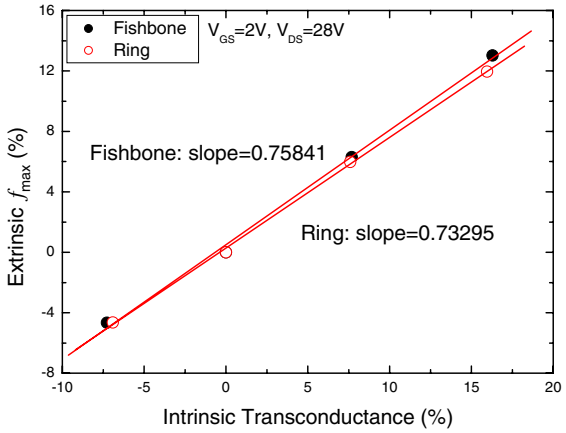


Fig. 9. (Color online) Extrinsic f_{max} variation versus intrinsic transconductance variation when temperature changes from 25 °C.

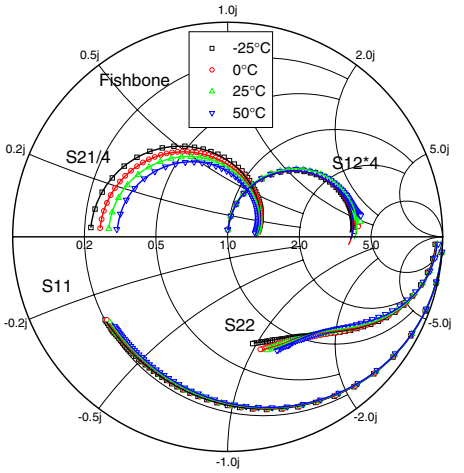
Figure 9 shows the variation in the extrinsic f_{max} versus the variation in the intrinsic g_m at $V_{GS} = 2$ V when temperature changes from 25 °C. The approximate relation of the extrinsic f_{max} and intrinsic g_m can be expressed as follows:[16]

$$f_{max} \sim \frac{f_T}{\sqrt{4g_{DS}R_g + 8\pi f_T C_{gd}(R_g + \alpha R_d)}}, \quad (3)$$

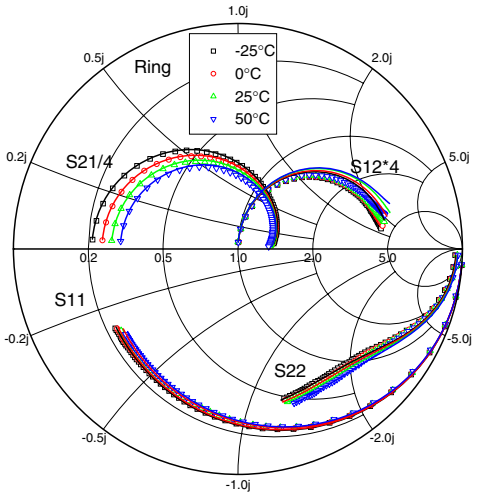
The intrinsic g_m dependence of f_{max} comes about through the f_T we mentioned above. The positive relation of f_T in the denominator results in a lower value for the curve slope in Fig. 9 than that in Fig. 8(a). In addition, the parasitic drain resistance in the denominator indicates that the R_d has a larger effect on f_{max}. Therefore, the ring structure, which has a lower drain parasitic resistance, shows more improvement on f_{max} than f_T.

3.3 *S-parameters characteristics*

Figure 10 shows the measured and simulated *S*-parameters of the fishbone and ring structures at various temper-



(a)



(b)

Fig. 10. (Color online) Measured (open symbols) and simulated (solid line) *S*-parameters of transistors with (a) fishbone and (b) ring structures from 0.1 to 10 GHz.

atures. The transistors were measured at $V_{GS} = 2\,V$ and a drain voltage (V_{DS}) of 28 V for the maximum value of f_T. In order to demonstrate the temperature dependence of the *S*-parameters, the model parameters of the small-signal equivalent circuit of the LDMOS transistors were extracted. The simulated results are also shown in Fig. 10. As illustrated in Fig. 10, the deviation of S_{11} with temperature is not marked. This suggests that the input impedance is affected by temperature slightly. Because the g_m decreases with increasing temperature, both S_{21} and S_{22} change significantly. At low frequencies, S_{21} can be approximated by[17)]

$$S_{21} = -2 \cdot g'_m \cdot R_L \cdot \frac{Z_O}{Z_O + R_d}, \qquad (4)$$

where $Z_O = 50\,\Omega$ and $R_L = R_{DS} \parallel (R_d + Z_O)$. It is proportional to g_m. However, at low frequencies, $S_{12} = 2sC'_{gd} \cdot Z_O$ is only related to the gate-to-drain capacitance (C_{gd}). Therefore, S_{21} changed significantly owing to the decrease in g_m, and S_{12} showed minor changes owing to the slight variation in C_{gd} with increasing temperature. It is interesting that the temperature-induced variation in S_{22} in the ring

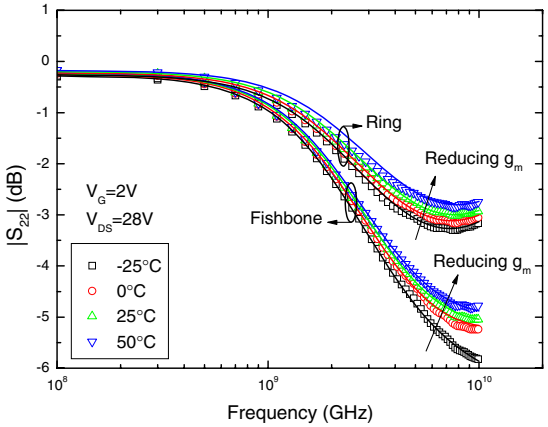


Fig. 11. (Color online) Measured (open symbols) and simulated (solid line) $|S_{22}|$ of transistors for different layout structures from 0.1 to 10 GHz.

structure is lower than that in the fishbone structure. Figure 11 shows the measured and simulated results of $|S_{22}|$ for the fishbone and ring structures. The extracted R_d and C_{jdb} of the ring structure are 7.8 Ω and 149 fF, respectively, which are lower than those of the fishbone structure (the extracted R_d and C_{jdb} are 18 Ω and 244 fF, respectively).[8)] This is a possible reason for the lower S_{22} variation in the ring structure with different temperatures.

4. Conclusions

The effects of temperature on the DC and high-frequency characteristics of RF LDMOS transistors were investigated in this study. The transconductance, threshold voltage, and channel mobility decrease with increasing temperature. The decrease in transconductance degrades the f_T and f_{max} at high temperatures. Owing to the higher drain resistance in the LDMOS transistors, the f_T is also affected by drain resistance. After de-embedding the effect of drain resistance, the temperature-induced f_T variation is almost proportional to the g_m variation. In addition, we found that the temperature dependence of f_{max} is also affected by the drain resistance and drain–substrate junction capacitance. Finally, we discussed the measured *S*-parameters at various temperatures. Because the LDMOS transistors with the ring structure have a lower drain resistance and a lower drain–substrate junction capacitance, the variation in S_{22} with temperature is smaller than that in the fishbone structure.

Acknowledgements

The authors would like to thank the staff of UMC for their helpful comments and the staff of the High Frequency Technology Center in NDL for measurement support. This work was supported in part by the R.O.C.'s National Science Council through contract NSC96-2221-E-492-014.

1) A. Wood, C. Dragon, and W. Burger: IEDM Tech. Dig., 1996, p. 87.
2) S. M. Nam, B. J. Lee, S. H. Hong, C. G. Yu, J. T. Park, and H. K. Yu: Proc. Int. Conf. VLSI and CAD (ICVC), 1999, p. 174.
3) Y. S. Lin: Microwave Opt. Technol. Lett. **44** (2005) 180.

4) J. G. Su, S. C. Woni, C. Y. Chang, K. Y. Chiu, T. Y. Huang, C. T. Ou, C. H. Kao, and C. J. Chao: Proc. IEEE Hong Kong Electron Devices Meet., 2000, p. 40.
5) M. A. Belaïd, K. Ketata, K. Mourgues, M. Gares, M. Masmoudi, and J. Marcon: Microelectron. J. **38** (2007) 164.
6) G. M. Dolny, G. E. Nostrand, and K. E. Hill: IEEE Trans. Electron Devices **39** (1992) 990.
7) Z. Radivojevic, K. Andersson, J. A. Bielen, P. J. van der Wel, and J. Rantala: Microelectron. Reliab. **44** (2004) 963.
8) H. H. Hu, K. M. Chen, G. W. Huang, C. Y. Chang, Y. C. Lu, Y. C. Yang, and E. Chen: Jpn. J. Appl. Phys. **46** (2007) 2032.
9) F. M. Rotella, G. Ma, Z. Yu, and R. W. Dutton: IEEE Trans. Microwave Theory Tech. **48** (2000) 991.
10) I. M. Filanovsky, A. Allam, and S. T. Lim: Analog Integrat. Circuits Signal Process. **27** (2001) 227.
11) Y. S. Koo, M. S. Kang, C. Choi, and C. An: J. Korean Phys. Soc. **39** (2001) 352.
12) M. Kodama, T. Sugiyama, and T. Uesugi: Electron. Commun. Jpn., Part II **84** (2001) No. 5, 55.
13) D. S. Jeon and D. E. Burk: IEEE Trans. Electron Devices **36** (1989) 1456.
14) Y. S. Lin: IEEE Trans. Electron Devices **52** (2005) 1442.
15) P. J. Tasker and B. Hughes: IEEE Electron Device Lett. **10** (1989) 291.
16) T. C. Lim and G. A. Armstronga: Solid-State Electron. **50** (2006) 774.
17) S.-S. Lu, T.-W. Chen, H.-C. Chen, and C. Meng: IEEE Trans. Microwave Theory Tech. **49** (2001) 333.