A Reverse-Voltage Protection Circuit for MOSFET Power Switches

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***Abstract*—When MOSFET is used as a power switch, it is essential to prevent reverse current flow through the parasitic body diodes under reverse voltage condition. A new built-in reverse voltage protection circuit for MOSFETs has been developed. In this design, an area-efficient circuit is used to automatically select the proper well bias voltage to prevent reverse current under the reverse-voltage condition. This built-in reverse protection circuit has been successfully implemented in a high-side power switch application using a 0.6-μm CMOS process. The die area of the protection circuit is only 2.63% of that of a MOSFET. The latch-up immunity is greater than +12 V and −10 V in voltage triggering mode, and greater than ±500 mA in current triggering mode. The protection circuit is not in series with the MOSFET switch, so that the full output swing and high power efficiency are achieved.**

***Index Terms*—CMOS, latch-up, power switch.**

I. Introduction

IN THE firewire bus interfaces (e.g., USB, IEEE 1394, PCMCIA, and Card Bus), intelligent MOSFET protection switches [1]–[4] are desired to protect the power buses not only from bursts, surges, and short circuits during plug or unplug, but also from reverse current. This is to say, when the peripheral device has a higher supply voltage, the MOSFET switch must be able to isolate the power buses. In a MOSFET, there are inherent parasitic diodes formed by the drain–well and source–well junctions. Under the reverse voltage condition, the parasitic diodes will be turned on if the well or the substrate is not properly biased. Excessive current flow may destroy devices. To eliminate the reverse current problem, reverse battery protection (RBP) structure [5] and floating-well circuits [6]–[10] were proposed. The RBP structure, shown in Fig. 1(a), consumes large die area because a huge MOSFET M2 is needed to reduce voltage drop. The floating-well protection circuits [see Fig. 1(b)] are more cost-effective and power-efficient. However, the floating well is more susceptible to noise coupling which may cause latch-up due to increased junction leakage current. To improve latch-up immunity, a deep implant process and large guard-ring spacing were used [6], [7].

In this paper, an area-efficient circuit is proposed to resolve these problems. This circuit automatically selects the proper n-well biasing voltage to prevent reverse current. The area of the protection circuit is only 2.63% of that of the MOSFET switch. The protection circuit is not in series with the MOSFET switch, so that the output swing and power efficiency are not affected. It also has robust electrostatic discharge (ESD) and latch-up performance. The proposed protection circuit is incorporated in an intelligent power switch IC, which is fabricated using a 0.6-μm standard digital CMOS process.

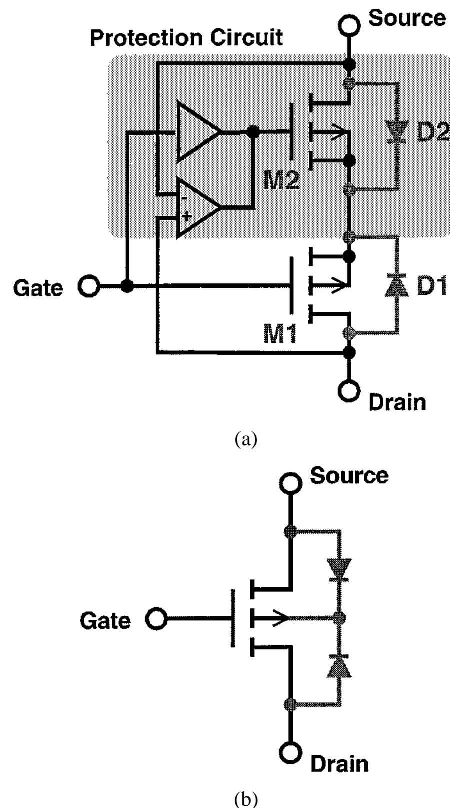

Fig. 1. Circuit structures for reverse voltage protection.

II. Built-In Reverse-Voltage Protection Circuit

The circuit diagram of the built-in reverse-voltage protection (BRVP) method is shown in Fig. 2. It improves the disadvantages of floating-well method and RBP method. As mentioned previously, the floating-well method is more area-efficient than RBP method. However, it is susceptible to latch-up problems and cannot isolate the two power sources. The problem could be resolved by dynamically biasing the well to the higher voltage one between the drain terminal and source terminal. The principle of the dynamical well-biasing circuit in Fig. 2 is similar to that of the RBP method, except that the additional large MOSFET in the supply path is moved to the well pick-up path. Therefore, the sizes of MOSFET MP1 and MP2 for well biasing are small because the current needed for biasing the well is very small. Hence, the total area of MOSFET with BRVP method is almost the same as that of the floating-well method. Thus, it is cost-effective and latch-up free. Under reverse-voltage conditions, the well and gate of the MOSFET are connected to the

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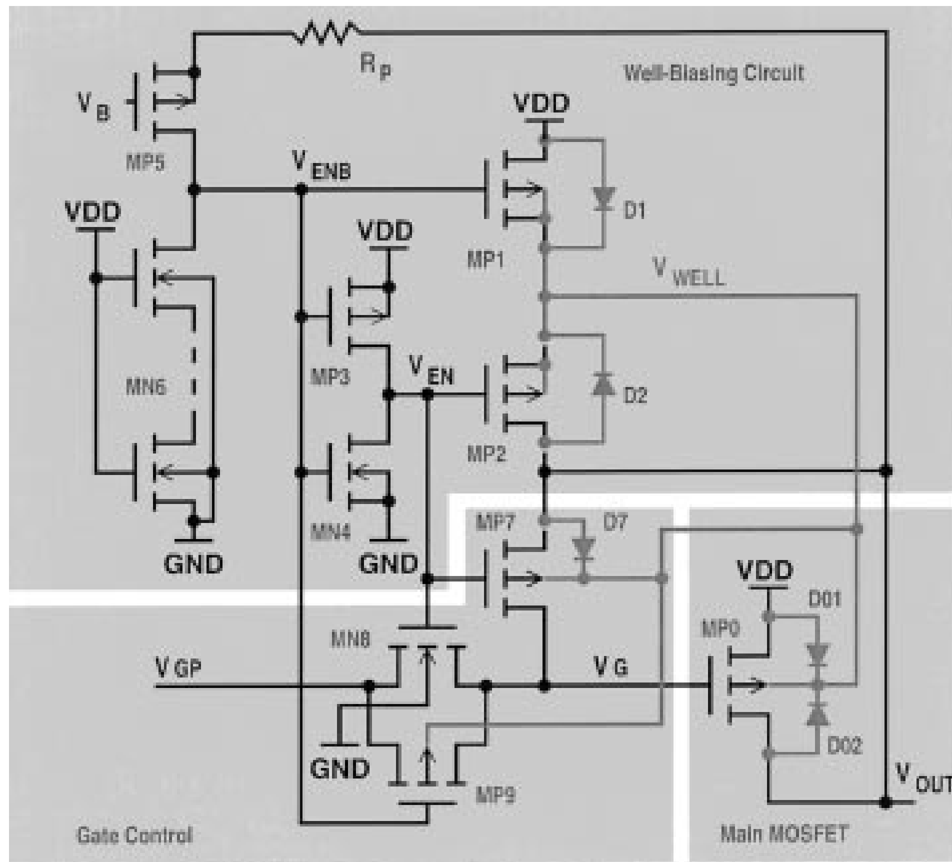

Fig. 2. Proposed BRVP circuit.

drain, so that the MOSFET and parasitic diodes are turned off to isolate the two power sources. The details of circuit operations with BRVP method are described below.

Referring to Fig. 2, as long as $V_{\rm OUT} < V_{\rm B} + |V_{tp}|$, the transistor MP5 is turned off, where V_{tp} and $V_{\rm B}$ are the threshold and gate voltages of MP5, respectively. Thus, $V_{\rm ENB} = {\rm GND}$ and $V_{\rm EN} = V_{DD}$. Therefore, MP1 is turned on and MP2 is turned off. The well voltage, $V_{\rm WELL}$, of the main MOSFET MP0 is equal to V_{DD}. The transmission gate (MN8 and MP9) in the main MOSFET MP0's gate-drive path is turned on, i.e., MP0 is directly driven by the gate-drive signal, $V_{\rm GP}$. If $V_{\rm OUT}$ is not connected to another voltage source, then $V_{\rm OUT}$ is always smaller than V_{DD}. Therefore, for the MOSFET switch to function correctly, it is required that $V_{\rm B} + |V_{tp}| \geq V_{DD}$. Under these conditions, transistor MP5 is always turned off, and the MOSFET MP0 behaves like a conventional MOSFET. Note that there is no dc current in the well-biasing circuit under these conditions.

If a voltage source is connected at the output node so that $V_{\rm OUT} > V_{\rm B} + |V_{tp}|$, then MP5 is turned on. Note that, in this case, $V_{\rm OUT}$ is greater than V_{DD}, because $V_{\rm B} + |V_{tp}| \geq V_{DD}$. A very small W/L ratio is used for MN6 so that once MP5 is turned on, the following is true: $V_{\rm EN} \cong V_{\rm OUT}$ and $V_{\rm ENB} = {\rm GND}$. With these two voltage levels, MP1 is turned off and MP2 is turned on. The well voltage $V_{\rm WELL}$ is connected to $V_{\rm OUT}$ by MP2. Since $V_{\rm OUT}$ is greater than V_{DD}, the parasitic diodes D01 and D1 are reverse biased and no reverse current will flow through these diodes. In the meantime, MN8 and MP9 are turned off and MP7 is turned on. The gate voltage of MP0, $V_{\rm G}$, is equal to $V_{\rm OUT}$, which ensures the MOSFET MP0 is turned off independent of the voltage $V_{\rm GP}$. Thus, when $V_{\rm OUT} > V_{\rm B} + |V_{tp}| \geq V_{DD}$, this circuit can prevent the reverse current by turning off the main MOSFET and keeping all the body diodes reverse biased. This circuit works well even if the power is turned off, i.e., $V_{DD} = {\rm GND}$ or V_{DD} is floating.

The choice of the value of $V_{\rm B}$ is important. To bias the well correctly and keep all the parasitic diodes turned off, there is another constraint: $V_{DD} \leq V_{\rm B} + |V_{tp}| \leq V_{DD} + V_d$, where V_d is the forward bias voltage of parasitic diode. Note that for $V_{\rm OUT}$ in the range of $V_{\rm B} + |V_{tp}| \geq V_{\rm OUT} \geq V_{DD}$, the well voltage $V_{\rm WELL}$ is still connected to V_{DD}. In this case, if $V_{\rm B} + |V_{tp}| \geq V_{DD} + V_d$, then for $V_{\rm OUT}$ in the range of $V_{\rm B} + |V_{tp}| \geq V_{\rm OUT} \geq V_{DD} + V_d$, the diode D02 will be turned on. Therefore, the value of $V_{\rm B}$ should be bounded by $V_{DD} - |V_{tp}| \leq V_{\rm B} \leq V_{DD} + V_d - |V_{tp}|$. Typically, $|V_{tp}|$ is larger than V_d, i.e., $V_{\rm B}$ should be smaller than V_{DD}. For example, let $V_{DD} = 5$ V, $|V_{tp}| = 0.8$ V, and $V_d = 0.6$ V, then ideally $V_{\rm B}$ should be in the range of 4.2 to 4.8 V. Generally, creating a voltage that is slightly less than the supply voltage is not too difficult. However, it requires additional circuits and dc currents. To avoid these penalties, $V_{\rm B}$ is directly connected to V_{DD} in this design. In this case, when $V_{DD} + |V_{tp}| \geq V_{\rm OUT} \geq V_{DD} + V_d$, a reverse current will flow from $V_{\rm OUT}$ through parasitic diodes D02 and D2 to $V_{\rm WELL}$, then through MP1 to V_{DD}. To minimize this reverse current, a small W/L ratio should be used for MP1. Since the diodes D02 and D2 are forward biased, the reverse current will flow in the n-well and into the substrate. To prevent latch-up, proper

guard rings are required for these transistors. Note that these guard rings are needed even if a proper value is used for $V_{\rm B}$. For example, let $V_{DD} = 5$ V, $|V_{tp}| = 0.8$ V, $V_d = 0.6$ V, and $V_{\rm B} = 4.5$ V, then for $V_{\rm OUT}$ in the range of 5 to 5.3 V, $V_{\rm WELL}$ is 5 V, i.e., the diodes D02 and D2 are slightly forward biased. Thus, guard rings are still needed to prevent latch-up.

For the ESD concern, when $V_{\rm B}$ is directly connected to V_{DD}, the ESD protection poly resistor $\rm R_p$ shown in Fig. 2 is needed to protect MP5. For the main MOSFET switch MP0, because it is used in hot-plug applications, the concerns about latch-up and ESD/electrical overstress (EOS) must be taken carefully. They are stated as followed. First, because MP0 is formed within an isolated n-well, it inherently has a better latch-up current blocking capability. However, as mentioned previously, double guard rings, inserted between MP0 and other nMOS circuits to block the latch-up current path, are still needed for latch-up prevention. Second, because the well of MP0 is automatically connected to the higher voltage between V_{DD} and $V_{\rm OUT}$, the ESD behavior of MP0 is like a reverse-biased diode, when a positive or negative voltage is stressed at pad with V_{DD} connected to ground. Because the minimum snapback holding voltage of pMOS is almost the same as the breakdown voltage, the phenomenon of snapback does not tend to occur. The ESD current of MP0 is discharged through the reverse junction breakdown. No ballast resistance is required. In the nMOS power switch case, the snapback characteristic is apparent. Inserting a ballast resistance to make ESD current discharged uniformly is necessary for nMOS to avoid ESD failures. With a ballast resistance, the drain-contact-to-gate spacing rule must be followed carefully in circuit layout. Under the constraint of this rule, to achieve the same ESD zapping level, nMOS requires much more area. Besides, if the substrate is grounded, the parasitic vertical bipolar p-n-p device (pad to n-well to p-substrate for diffusion well process only) also helps to bypass the ESD current, when an ESD voltage is stressed. Hence, using pMOS as a switch has more advantages in terms of ESD concerns. Third, the breakdown voltage of pMOS is higher when compared with nMOS. In a 0.6-μm process, the breakdown voltage of pMOS is about 13 V; however, the breakdown of nMOS is only about 11 V. For burst and surge current concerns of hot-plug interfaces, pMOS could meet the requirement of robust EOS reliability due to its higher breakdown voltage.

III. Experimental Results

Based on the proposed reverse-current prevention design, a MOSFET with the BRVP circuit has been successfully implemented in a dual-channel intelligent high-side power switch using a 0.6-μm CMOS logic process. Fig. 3 is the microphotograph of this power switch, where the main MOSFETs and reverse-voltage protection circuits are marked. It can be seen that the areas of BRVP circuits are small. The chip area including pads is 2547 μm $\times$ 2453 μm. The size of the MOSFET is 180 mm/0.8 μm. Its on-resistance is 70 mΩ. Its die area is 920 μm $\times$ 1623 μm. The die area of a BRVP circuit is 333 μm $\times$ 118 μm, which is only 2.63% of a MOSFET.

Fig. 4 shows the reverse-current measurement results with $V_{DD} = 3.3$ V, GND, and opened, when a reverse voltage is applied to $V_{\rm OUT}$. The three curves show that the reverse currents are small. When $V_{DD} = 3.3$ V, a peak reverse current of 1.119 mA occurs at $V_{\rm OUT} = 3.85$ V. As discussed in the previous section, with $V_{\rm B} = V_{DD}$, when $V_{DD} + V_d \leq V_{\rm OUT} \leq V_{DD} + |V_{tp}|$, transistor MP1 will not be turned off. Reverse current will flow from $V_{\rm OUT}$ through D2 and D02, and Mp1 to V_{DD}. When V_{DD} exceeds 4.1 V, MP1 is turned off; the reverse current reduces to 1 μA. When $V_{DD} =$ GND, because MN6 is OFF, $V_{\rm ENB} = V_{\rm OUT}$, if $V_{\rm OUT} \geq |V_{tp}|$. Hence, the measured leakage is larger when $V_{\rm OUT} < 0.8$ V, with a peak current of 4 nA. When V_{DD} is floating, as $V_{\rm OUT}$ is increased from 0 V, V_{DD} is slowly charged by the reverse current so that its voltage also rises. Thus it takes a larger $V_{\rm OUT}$ (1.2 V) to turn on MP5, when compared with the V_{DD}-grounded case. The peak reverse current is 0.8 μA. No latch-up occurs for all these static tests. Dynamic latch-up tests were performed according to JEDEC 17 standard, with V_{DD} fixed at 5 V. For the voltage triggering mode, up to +12 and -10 V, in 1 V steps, with respect to V_{DD} were performed without latch-up. For the current triggering mode, up to ± 500 mA, in 25 mA steps, were performed without latch-up. For the ESD protection, a filed-oxide

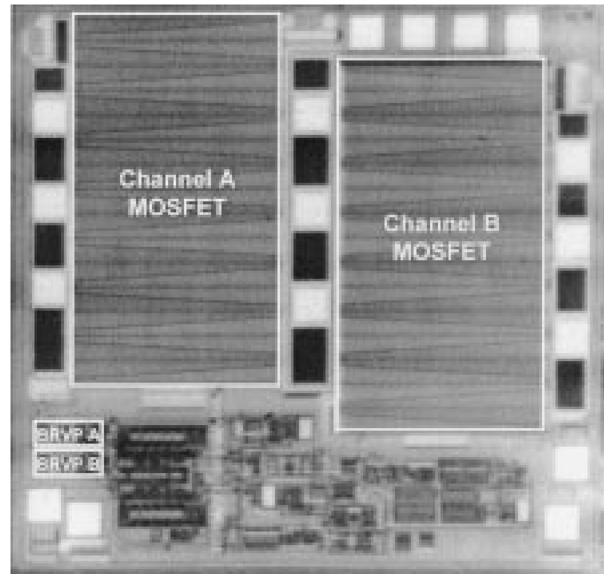

Fig. 3. Microphotograph of a dual-channel MOSFET power switch.

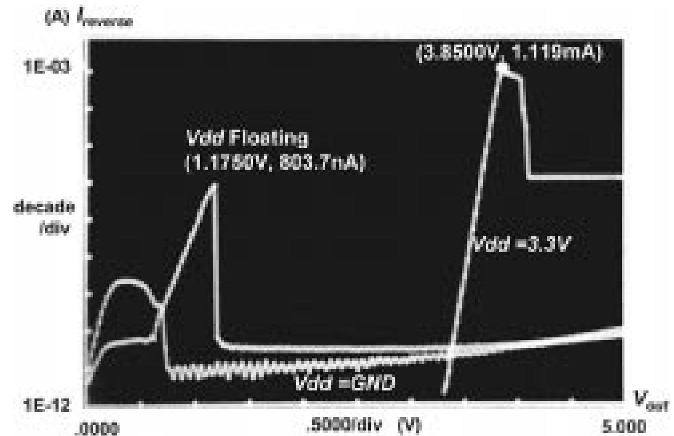

Fig. 4. Reverse current versus reverse voltage ($I_{\rm reverse}$ versus $V_{\rm out}$)

device (FOD) has been added for providing a ground discharge path. Based on the MIL-STD-883C 3015.7 Human Body Model (HBM) testing standard, the V_{OUT} pin passes 8 kV ESD test in all four modes zapping.

Compared with the RBP circuits shown in Fig. 1(a), the proposed BRVP circuit has the advantages of full output voltage swing and smaller die area, due to the removal of the series-connected pMOS M2. Although the floating-well circuit shown in Fig. 1(b) does not have series-connected pMOS, its MOSFETs die area is larger than that of the BRVP for the same turn-on resistance. The reason is that a large distance (55 μm) is needed between the source–drain junctions and the well edges to improve latch-up immunity [6]. It also needs an additional deep implant to construct a more effective guard ring for latch-up prevention. On the other hand, the proposed BRVP circuit is fabricated using standard digital CMOS process and standard layout design rules.

IV. Conclusion

A BRVP circuit for MOSFET used as power switch was proposed. A MOSFET with this BRVP circuit was incorporated in an intelligent power switch IC with diagnostics. It was implemented in a 0.6-μm CMOS logic process. The well of the pMOS is automatically connected to its source or drain depending on which voltage is higher. Thus, the parasitic source–drain junction diodes are always reverse-biased to prevent reverse current and latch-up. Under reverse-voltage conditions, the gate of MOSFET is connected to V_{OUT} to isolate V_{DD} and V_{OUT}. This protection circuit does not require any external control signals, thus it is also applicable for conventional three-terminal MOSFETs. By moving the protection devices in the supply path into the well-biasing circuit, small devices can be used so that this circuit occupies very small areas. In our test chip, its area is only 2.63% of that of a MOSFET switch. The area penalty is small. With only one main MOSFET in the supply path, the reverse-voltage protection circuit has the same advantages of full output voltage swings and higher power efficiency than a floating-well circuit does. However, by always connecting the n-well to the higher voltage between source and drain voltages, this circuit has better latch-up robustness than floating-well circuits. Besides, a special deep-implant process is needed for the floating-well circuits. The measured results show the reverse-voltage protection circuit works well, even if the supply voltage is zero or is floating. The ESD protection is > 8 kV. The latch-up immunity is greater than $+12$ and -10 V in voltage triggering mode, and greater than ± 500 mA in current triggering mode.

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