A Novel Thin-Film Transistor with Self-Aligned Field Induced Drain

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***Abstract*—In this letter, a novel thin-film transistor with a self-aligned field-induced-drain (SAFID) structure is reported for the first time. The new SAFID TFT features a self-aligned sidewall spacer located on top of the drain offset region to set its effective length, and a bottom gate (or field plate) situated under the drain offset region to electrically induce the field-induced-drain (FID). So, unlike the conventional off-set-gated TFTs with their effective FID length set by two separate photolithographic masking layers, the new SAFID is totally immune to photomasking misalignment errors, while enjoying the low off-state leakage as well as high turn-on characteristics inherent in the FID structure. Polycrystalline silicon TFTs with the new SAFID structure have been successfully fabricated with significant improvement in the on/off current ratio.**

***Index Terms*—Field-induced drain, leakage current, thin-film transistor.**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (poly-Si TFTs) have been intensively investigated for high-performance large-area active matrix liquid-crystal display (AMLCD) applications. Unlike the conventional amorphous silicon TFTs, the poly-Si TFTs exhibit higher drive current. This, together with the availability of both n- and p-channel TFTs, has facilitated the integration of high-performance CMOS peripheral drivers with the active switching elements on the same substrate, drastically reducing the number of external connections for better reliability and reduced cost [1], [2].

However, conventional poly-Si TFTs suffer from an anomalous off-state leakage current, which increases with drain voltage and gate voltage [3]. This undesirable off-state leakage current prohibits the use of poly-Si TFTs in many high-performance circuit applications. For example, off-state leakage current less than 1 pA per pixel is required for gray-scale active matrix liquid crystal displays [4]. The dominant off-state leakage current is known to be field emission via grain boundary traps due to high electric field in the drain depletion region [3]. Thus, an effective method to suppress the off-state leakage current is to reduce the electric field near the drain by incorporating an undoped or lightly-doped offset region near the heavily-doped drain. Two approaches have been previously proposed to achieve such an offset region. The first approach employs a self-aligned sidewall spacer, similar to that used in forming the lightly doped drain (LDD) metal-oxide-semiconductor (MOS) transistors [5]–[7]. The LDD approach normally requires an LDD implant step in order to achieve reasonable turn-on characteristics. The second approach, which was originally proposed by one of the present authors [8], [9], employs a field plate or sub-gate to create a field-induced-drain (FID) region. In the FID approach, the lightly-doped implant required in the LDD approach can be skipped. The FID approach has been shown to be very effective in reducing the off-state leakage, while maintaining good turn-on characteristics. The excellent off-state leakage is believed to be due to the combined effects of a reduced drain electric field and the excellent damage-free junction inherent in the FID structure [10]. This is because, unlike the LDD approach, the implant damage inherent in the implanted region is completely eliminated in the field-induced drain structure. This implant-damage-free feature is especially important for low-temperature and mid-temperature poly-Si TFT technologies employing glass-compatible substrates. However, one major drawback of the FID approach is that the length of its FID region is determined by two masking layers during its formation process, and is therefore susceptible to misalignment errors [8]–[10]. Since both the off-state leakage current and the turn-on characteristics are known to be sensitive to the length of the FID region, the misalignment susceptibility could represent a big manufacturability issue in mass production [9]. This is especially serious for large area applications where the alignment errors usually get worse because of the large-area substrate and the normally looser alignment accuracy that can be achieved with the large-area steppers. In contrast, the LDD approach is self-aligned in nature, and is therefore immune to the above-mentioned misalignment errors.

In this letter, we propose for the first time a novel TFT structure that retains the low off-state leakage and high on-current features characteristic of the FID approach, while also possesses the self-aligned misalignment-free nature characteristic of the LDD approach. Poly-Si TFTs with the new self-aligned field-induced-drain (SAFID) structure have been successfully demonstrated.

II. Experiments

The key process flow for the SAFID TFT is shown in Fig. 1. Briefly, a 100 nm highly-doped poly-Si layer was first deposited on an oxidized silicon substrate by low pressure chemical vapor deposition (LPCVD). The doped poly-Si film was then patterned to form individual subgates (or field plates). Next, a 100

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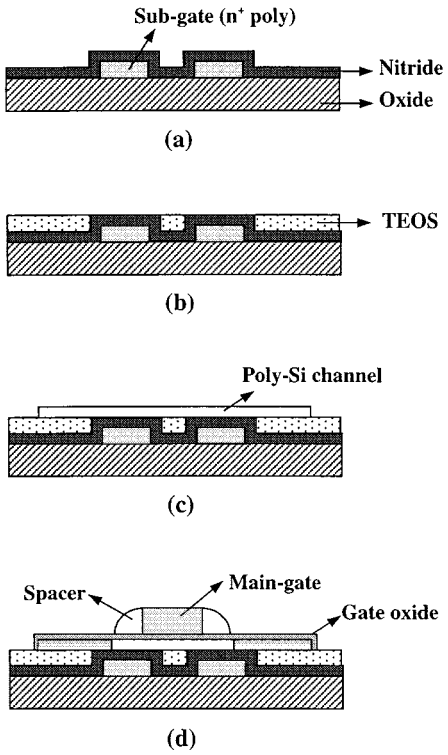

Fig. 1. Key process flow of the SAFID TFTs.

nm CVD nitride was deposited by LPCVD [Fig. 1(a)], followed by the deposition of a thick LPTEOS (550 nm) oxide layer. Chemical mechanical polishing (CMP) was then applied to planarize the wafer surface and expose the nitride layer on top of the subgate [Fig. 1(b)]. The nitride layer thus serves not only as the dielectric separation between the field plate (i.e., subgate) and the active device layer in the final device structure, but also as a stopping layer for better process control during CMP polishing. It should be noted, however, that the CMP step can actually be skipped for process simplicity, especially for devices with large dimensions typically found in large-area applications. Afterwards, a 50 nm CVD amorphous thin Si film was deposited at 550 °C, and subsequently transformed into polycrystalline phase by a solid-phase recrystallization (SPC) treatment at 600 °C for 24 h [Fig. 1(c)] to serve as the active device layer. A 20 nm CVD oxide layer was then deposited to form the gate insulator. A third poly-Si film was deposited and patterned to form the top-gate (i.e., main-gate). Next, a self-aligned sidewall spacer was formed by the deposition of an oxide layer and subsequent reactive-ion-etching. Finally, self-aligned source/drain regions were formed by a heavy-dose implant [Fig. 1(d)]. For n-channel transistors, As^+ implant with a dosage of $5 \times 10^{15}\,\mathrm{cm}^{-2}$ at 20 KeV was used. The implanted dopants were subsequently activated in N_2 at 600 °C for 12 h. Wafers then followed a standard back-end processing to form the contact pads, and received a plasma treatment at 250 °C in NH_3 for 1 h before measurements. Poly TFTs with conventional structure (e.g., without the subgate) were also fabricated alongside to serve as the control.

The main feature of the novel SAFID TFT is that the field plate (or the subgate) for creating the field-induced-drain is located underneath the offset drain region. While the effective length of the offset drain region is set by the self-aligned sidewall spacer, which is formed abutting the top-gate (i.e., the main gate) of the SAFID TFT. These combinations provide, for the first time, a self-aligned field-induced-drain with the length of its FID region immune to misalignment errors. It should be noted that although both drain and source offset regions are shown in the figure for process simplicity and device symmetry, the source-side offset region can be easily eliminated by selectively removing the sidewall spacer on the source side before performing the heavily-doped source-drain implant.

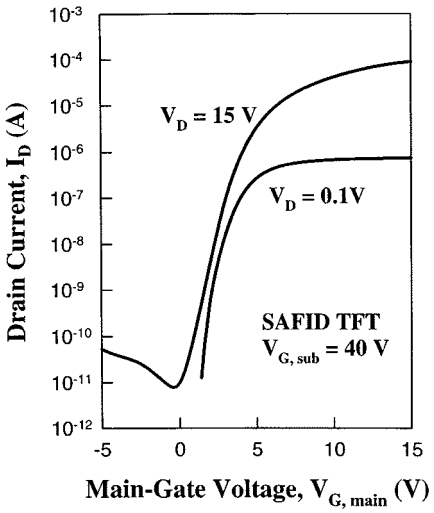

Fig. 2. Subthreshold characteristics of the SAFID TFT. L/W of the device is $2/10\,\mu$m/μm.

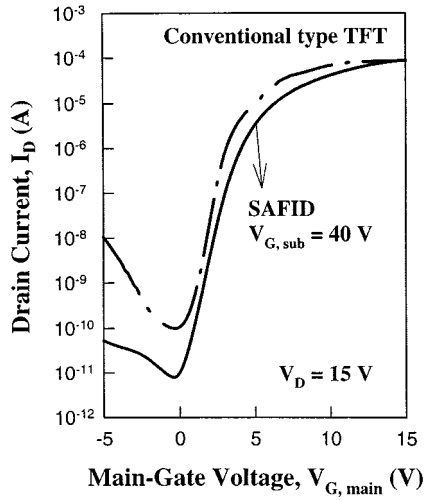

Fig. 3. Comparison of subthreshold characteristics between SAFID and conventional TFT devices. L/W of the device is $2/10\,\mu$m/μm.

III. Results and Discussion

Fig. 2 shows typical subthreshold characteristics of the SAFID TFT devices with a subgate voltage of 40 V. Well-behaved transfer characteristics and high on/off current ratio ($\sim 10^7$) are achieved in the SAFID TFT. As shown in Fig. 3, the off-state current of the SAFID TFT is much lower than that of the conventional TFT control. Specifically, the leakage current is ten

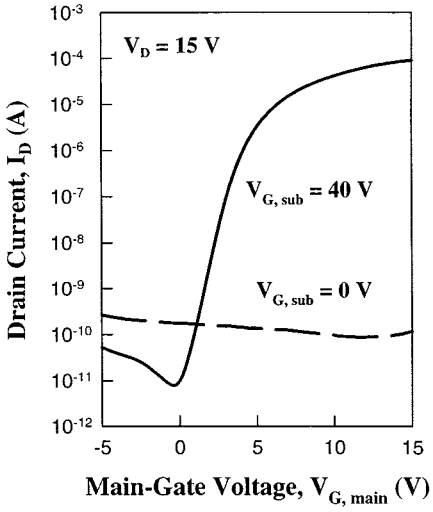

Fig. 4. Effects of subgate bias on the transfer characteristics of the SAFID TFT. L/W of the device is $2/10\,\mu$m/μm.

times smaller at $V_G = 0$ V and 100 times smaller at $V_G = -5$ V, compared to the conventional TFT control. Nevertheless, good drive current capability, comparable to that of the conventional TFT control, is still retained for the SAFID TFT. These features are similar to those reported in previous works [8], [9]. It is worthy to note here that there exists a separation between the top-gated conduction channel and the bottom field-induced drain in the SAFID structure. This is similar to the case in the popular inverted-staggered bottom-gated thin film transistors structure [11]. Although the separation could cause some additional source-drain series resistance, resulting in a slightly higher threshold voltage and lower subthreshold leakage, its effect appears to be minimal and could be further reduced with the use of a thin active device layer so that the separation is minimized. This is indeed confirmed by the excellent turn-on characteristics of the SAFID devices.

The effects of subgate bias on the device operation are shown in Fig. 4. It can be seen that when no subgate bias is applied, the SAFID TFT cannot be effectively turned on even when proper main-gate voltage is applied. This is because under such conditions, the field-induced source and drain are not formed, and thus the switching behavior of the device is prohibited. It is interesting to note here that the leakage current at negative main-gate voltage region can even be lowered when the subgate bias is applied. The cause of this phenomenon is still not very clear at this moment, and is presumably related to the defects present at the channel/nitride interface induced during the CMP stage.

IV. Conclusion

In this work, we have proposed and successfully demonstrated a novel self-aligned field-induced-drain (SAFID) thin-film transistor structure. The new SAFID TFT features a bottom subgate (or field plate) for inducing the field-induced-drain and a top self-aligned sidewall spacer for setting the effective length of the FID region. So, unlike previous versions of TFTs with FID, the new SAFID TFT is therefore not susceptible to photomasking misalignment errors, while preserving the good off-state leakage and turn-on characteristics inherent in the FID structure. SAFID transistors with excellent on/off current ratio have been succesfully demonstrated. The new SAFID TFT therefore appears to be a very attractive device structure for future high-performance large-area device applications.

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