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High-Performance Solid-Phase Crystallized Polycrystalline Silicon Thin-Film Transistors with Floating-Channel Structure

Chia-Wen CHANG, Chih-Kang DENG, Che-Lun CHANG, Ta-Chuan LIAO, and Tan-Fu LEI

Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan

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High-performance solid-phase crystallized polycrystalline silicon thin-film transistors with a floating-channel active region (FC poly-Si TFTs) are proposed in this study. A high-quality poly-Si channel film accompanied by a larger grain size and fewer microstructural defects could be obtained. Compared with the conventional poly-Si TFTs (CN poly-Si TFTs), the fabricated FC poly-Si TFTs exhibit superior electrical characteristics, including lower threshold voltage, higher field-effect mobility, and lower trap state density. These electrical performance improvements could be attributed to the fact that the α-Si film with a floating-channel structure can relieve the stress generated from the crystallization process accompanying the trap state density reduction and grain size enhancement. In addition, the FC poly-Si TFTs also exhibit improved hot-carrier stress immunity due to the reduced weak Si–H bonds from fewer grain boundaries in the poly-Si channel. Therefore, the proposed FC poly-Si TFTs can be easily fabricated by conventional solid-phase crystallization, and suitable for future high-performance flat-panel display applications. [DOI: 10.1143/JJAP.47.3024]

KEYWORDS: floating-channel structure, surface nucleation, solid-phase crystallization (SPC), thin-film transistor (TFT)

1. Introduction

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used for active matrix liquid crystal displays (AMLCDs). High-performance and superior-reliability poly-Si TFTs have the potential to realize the integration of peripheral driving circuits and pixel switching elements on a single glass substrate.[1,2] To fabricate poly-Si TFTs on an inexpensive glass substrate, low-temperature technology is required for realizing flat-panel displays (FPDs) owing to the maximum process temperature of being lower than 600 °C. The solid-phase crystallization (SPC) process is widely used for phase transformation from amorphous to polycrystalline due to its low fabrication cost and good grain-size uniformity. However, the electrical characteristics of SPC poly-Si TFTs are strongly correlated to the microstructure of poly-Si channel film. It is well known that the presence of a large number of grain boundaries and intragranular defects acting as scattering centers and midgap traps in the poly-Si film degrades the electrical properties of poly-Si TFTs.[3,4] Therefore, the SPC process plays an important role in determining the device performance. Unfortunately, the traditional SPC process is an interface-nucleation mechanism generating too many nucleation sites at the amorphous silicon/underlying oxide (α-Si/SiO_2) interface, resulting in a smaller poly-Si grain size and many grain boundary defects.[5,6] Various techniques have been employed to improve the device performance either by reducing the trap state density[7,8] or increasing the grain size of SPC poly-Si film.[9–12] The hydrogen plasma treatment is widely used to reduce the trap state density due to the passivation of trap states. Although hydrogen plasma treatment can improve the electrical performances, it is difficult to control the optimal processing time for satisfactory performance improvements. In addition, the hydrogenated poly-Si TFTs also suffer from a serious instability in their electrical characteristics under long-term electrical stress due to the easy breaking of weak Si–H bonds at the grain boundaries.[13] Recently, many SPC processes associated with the surface-nucleation scheme were proposed to improve the microstructure of poly-Si film by utilizing oxygen doping at the α-Si/SiO_2 interface.[9–11] It has been known that oxygen atoms retard the crystallization process of an oxygen-implanted α-Si film during solid-phase epitaxial regrowth.[12] As interface nucleation is effectively suppressed by the incorporation of oxygen atoms at the α-Si/SiO_2 interface, the nucleation process will initiate at another preferable nucleation site on the top free surface of the α-Si film. Because of fewer nucleation sites at the top free surface of the α-Si film, a larger poly-Si grain size can be obtained. However, these surface-nucleation methods mentioned previously require relatively complicated fabrication procedures, and they are not practical for TFT applications.

In this paper, we take advantage of the SPC surface-nucleation scheme proposed by Bo *et al.*,[14] and then design the self-aligned formation of a floating channel structure without any additional sacrificial pattern to form the air gap. Experimental results also confirm that the grain size and trap state density of the floating-channel poly-Si film are markedly improved; moreover, relatively better electrical characteristics are also achieved. Therefore, the proposed fabrication procedure for floating-channel poly-Si TFT (FC poly-Si TFT) is very simple and low cost. It is also reproducible and compatible with existing poly-Si TFT manufacturing processes.

2. Experimental Procedure

Figures 1(a) and 1(b) schematically depict bird's eye and cross-sectional views of the proposed FC poly-Si TFT. The fabrication processes of the FC poly-Si TFT are exhibited as follows. First, a 150 nm silicon nitride (Si_3N_4) layer, a 20 nm tetraethooxysilane (TEOS) oxide, and a 50 nm α-Si film were successively deposited by low-pressure chemical vapor deposition (LPCVD) to serve as the buffered layer, dummy oxide, and channel film, respectively. After the individual α-Si active regions were anisotropically patterned and defined, an isotropic wet etching was performed using buffer oxide etchant (BOE) solution with a constituent ratio of HF : $NH_4F = 7 : 1$ to remove the dummy TEOS oxide to form the floating-channel α-Si region, as shown in Fig. 1(a). The etching rates of BOE for dummy TEOS oxide and α-Si

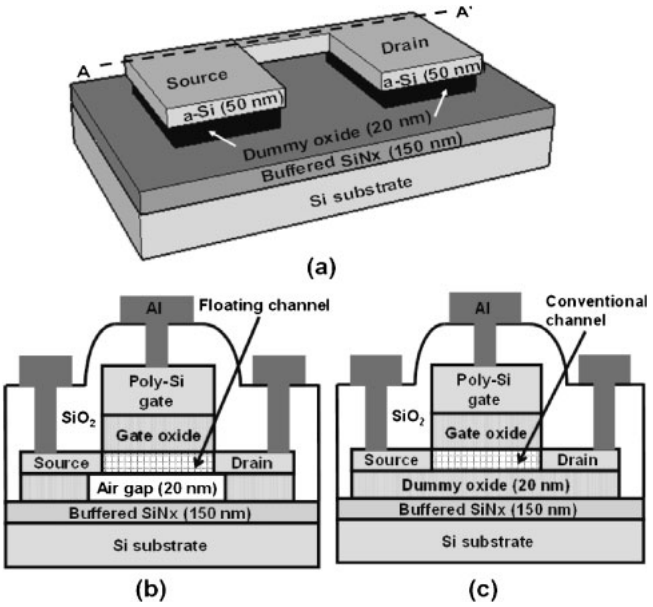

Fig. 1. (a) Bird's eye view of the FC poly-Si TFT. (b) Cross-sectional view of the FC poly-Si TFT along the AA′ line shown in (a). (c) Cross-sectional view of the CN poly-Si TFT.

were 15 nm/s and 0.4 nm/min, respectively. Therefore, the dummy TEOS oxide was etched for 90 s to make sure the floating-channel structure could be easily created between the large areas of source/drain pads. Subsequently, the α-Si film with a floating-channel structure was recrystallized at 600 °C for 24 h in N_2 ambient for phase transformation from amorphous to polycrystalline. After RCA cleaning, a 100 nm TEOS oxide and a 150 nm poly-Si film were deposited to serve as the gate dielectric and gate electrode, respectively. A self-aligned phosphorous ion implantation was performed at dosage and energy values of 5×10^{15} and 15 keV, respectively. A 300 nm passivation SiO_2 layer was deposited by plasma-enhanced CVD (PECVD), followed by the realization of dopant activation at 600 °C for 12 h and the definition of contact holes. Finally, a 400 nm Al electrode was deposited and patterned. An NH_3 plasma treatment was performed at 350 °C for 30 min after the Al electrode formation. For comparison, conventional poly-Si TFT (CN poly-Si TFT) without the removal of dummy TEOS oxide was also fabricated, as shown in Fig. 1(c). Therefore, the distinction between the Si atoms unbounded and bounded to the underlying dummy TEOS oxide could be easily observed from the poly-Si films with floating-channel and conventional structures, respectively.

3. Results and Discussion

A cross-sectional transmission electron microscopy (TEM) image of the proposed FC poly-Si TFT structure is shown in Fig. 2. From the TEM image, it is clearly observed that the thicknesses of the floating-channel poly-Si film and the air gap are 47 and 20 nm, respectively. Thus, there really exists a floating-channel poly-Si film on the air gap. SEM images of poly-Si films used in the FC poly-Si TFT and CN poly-Si TFT after Secco etching are shown in Figs. 3(a) and 3(b), respectively. These images obviously show that the average grain sizes of poly-Si films for the FC poly-Si TFT and CN poly-Si TFT are approximately 150 and 50 nm,

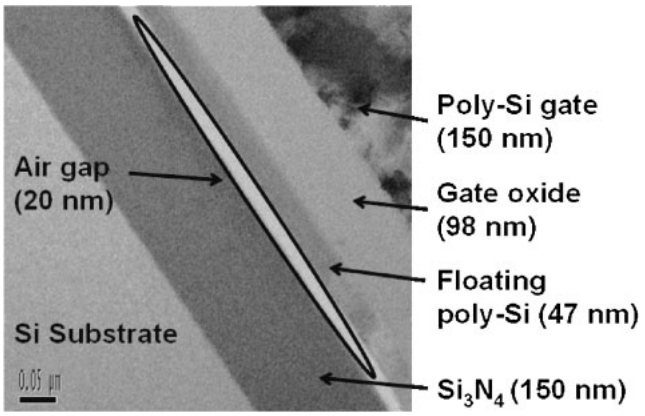

Fig. 2. Cross-sectional TEM image of the FC poly-Si TFT.

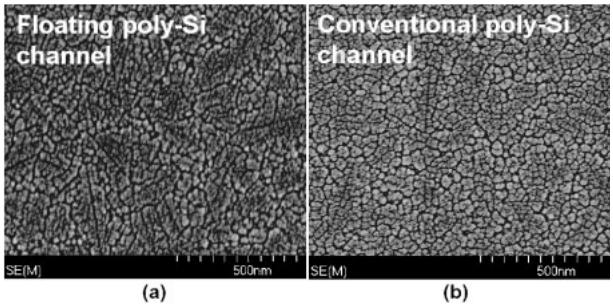

Fig. 3. SEM images of poly-Si films used in (a) the FC poly-Si TFT and (b) the CN poly-Si TFT, after Secco etching.

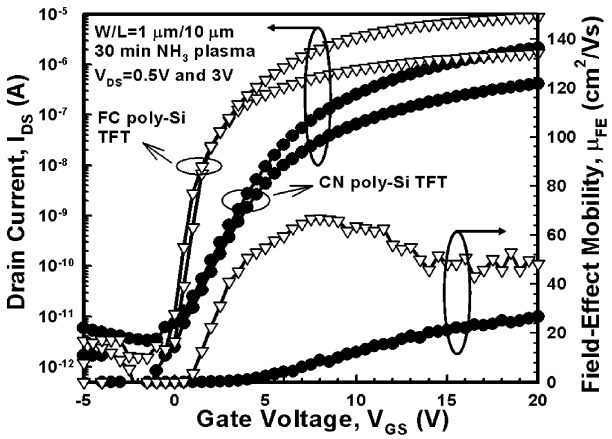

Fig. 4. Transfer characteristics and the extracted field-effect mobility of the FC and CN poly-Si TFTs with dimensions of $W/L = 1\,\mu m/10\,\mu m$.

respectively. The result indicates that a better polycrystalline structure with larger grain size and fewer intragranular defects can be obtained in the floating-channel poly-Si film.

Figure 4 presents the transfer characteristics (I_{DS}–V_{GS}) of the FC poly-Si TFT and CN poly-Si TFT. The measurements are performed at two different drain voltages of $V_{DS} = 0.5$ and 3 V. The drawn channel width (W) and channel length (L) are 1 and 10 μm, respectively. The parameters of the devices, including the threshold voltage (V_{TH}), field-effect mobility (μ_{FE}), and subthreshold swing (SS), are extracted at $V_{DS} = 0.5$ V, whereas the maximum on-state driving current (I_{ON}) is defined at $V_{DS} = 3$ V. The ON/OFF current ratio (I_{ON}/I_{OFF}) is defined as the ratio of the maximum on-state driving current to the minimum off-state leakage current

Table I. Comparison of device characteristics for the FC and CN poly-Si TFTs with dimensions of $W/L = 1\,\mu m/10\,\mu m$.

	FC poly-Si TFT	CN poly-Si TFT
Threshold voltage (V)	1.62	6
Subthreshold swing (mV/dec)	264	971
Field-effect mobility ($cm^2\,V^{-1}\,s^{-1}$)	66.9	21.1
Maximum on-state current (A)	8.9×10^{-6}	1.5×10^{-6}
ON/OFF current ratio	5.8×10^{6}	6.8×10^{5}

at $V_{DS} = 3\,V$. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of $I_{DS} = (W/L) \times 100\,nA$ at $V_{DS} = 0.5\,V$. The measured and extracted device parameters of the FC poly-Si TFT and CN poly-Si TFT are summarized in Table I.

Accordingly, the electrical properties of the FC poly-Si TFT are significantly improved compared with those of the CN poly-Si TFT. The threshold voltage and subthreshold swing of the FC poly-Si TFT are 1.62 V and 264 mV/dec, whereas the CN poly-Si TFT has values of 6 V and 971 mV/dec, respectively. The threshold voltage and subthreshold swing of the FC poly-Si TFT are found to be superior to those of the CN poly-Si TFT. Some studies indicated that the silicon dangling bonds originating from the deep trap states have energy states near the middle of the silicon bandgap, greatly affecting the threshold voltage and subthreshold swing.[3)] The floating-channel poly-Si film with the surface-nucleation scheme can improve the poly-Si crystallinity with fewer trap states at the grain boundaries. In addition, the maximum on-state driving current and ON/OFF current ratio of the FC poly-Si TFTs are better than those of the CN poly-Si TFT. The FC poly-Si TFT exhibits approximately one order of magnitude enhancement in the maximum on-state driving current compared with the CN poly-Si TFT at $V_{GS} = 20\,V$ and $V_{DS} = 3\,V$. Moreover, the ON/OFF current ratio of the FC poly-Si TFT is about eight times larger than that of the CN poly-Si TFT. The result suggests that there must be larger poly-Si grains existing in the floating-channel poly-Si film, and thereby the subthreshold and on-state characteristics can be significantly improved.

Figure 4 also shows the field-effect mobility versus gate voltage for the FC and CN poly-Si TFTs. The field-effect mobility is calculated from the transconductance at $V_{DS} = 0.5\,V$. As can be seen, the maximum field-effect mobility of the FC poly-Si TFT is around three times higher than that of the CN poly-Si TFT. Note that the strain bonds associated with the tail states near the silicon band edge in the poly-Si film, and at the gate oxide/poly-Si interface greatly affect the field-effect mobility. The improvement of field-effect mobility could be attributed to the enhancement of grain size and the reduction of grain boundaries, thereby leading to a better poly-Si grain crystallinity in the floating-channel poly-Si film.

To verify the effect of poly-Si grain enhancement, the effective trap state density (N_{trap}) was extracted from the square root of the slope of the $\ln[(I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ plots according to the grain-boundary trapping model proposed by Levinson *et al.*[15)] Figure 5 shows the $\ln[(I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ characteristics at $V_{DS} = 0.5\,V$ and a high gate voltage for the FC and CN poly-Si TFTs. It can be found that the FC poly-Si TFT exhibits a N_{trap} of $7.1 \times 10^{11}\,cm^{-2}$, whereas the CN poly-Si TFT possesses a N_{trap} of $1.36 \times 10^{12}\,cm^{-2}$. This result further confirms that the floating-channel poly-Si film has much fewer grain boundaries and microstructure defects than the conventional poly-Si film due to the enlarged grain size.

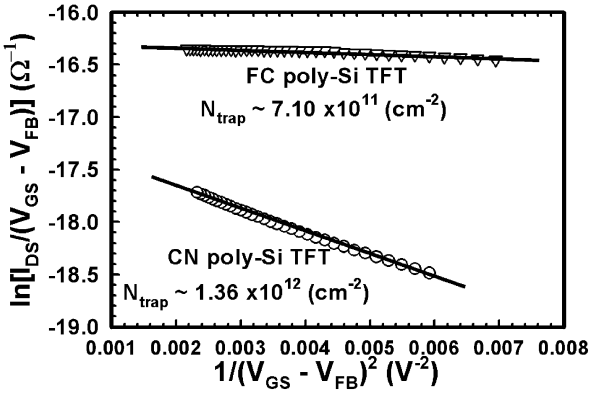

Fig. 5. Plot of $\ln[(I_{DS}/(V_{GS} - V_{FB})]$ vs $1/(V_{GS} - V_{FB})^2$ and the extracted effective trap state density (N_{trap}) for the FC and CN poly-Si TFTs. I_{DS} was measured at $V_{DS} = 0.5\,V$.

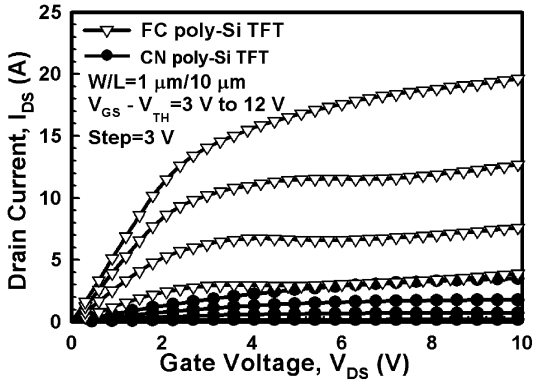

Fig. 6. Output characteristics of the FC and CN poly-Si TFTs with dimensions of $W/L = 1\,\mu m/10\,\mu m$.

Figure 6 shows the output characteristics (I_{DS}–V_{DS}) of the FC and CN poly-Si TFTs. As can be seen, the FC poly-Si TFT exhibits a great enhancement in the driving current at $V_{DS} = 10\,V$ and common-gate driving voltages of $V_{GS} - V_{TH} = 3$, 6, 9, and 12 V. The improvement can be attributed to the field-effect mobility and threshold voltage of the FC poly-Si TFT being higher and lower than those of the CN poly-Si TFT.

These electrical performance improvements strongly related to the crystallinity of poly-Si film could be qualitatively explained as follows. While using the conventional SPC process with the interface-nucleation scheme to crystallize α-Si into poly-Si, the rearrangement of interfacial Si atoms and volume contraction of bulk Si film induce tensile stress at the Si film/underlying oxide interface. Hence, a large number of crystalline defects, such as microtwins and dislocations, are generated to relieve the tensile stress. Following, numerous nucleation sites could be produced to result in smaller poly-Si grain size.[11,14)] Nevertheless, in the case of poly-Si film with a floating-channel structure in this work, the removal of underlying dummy

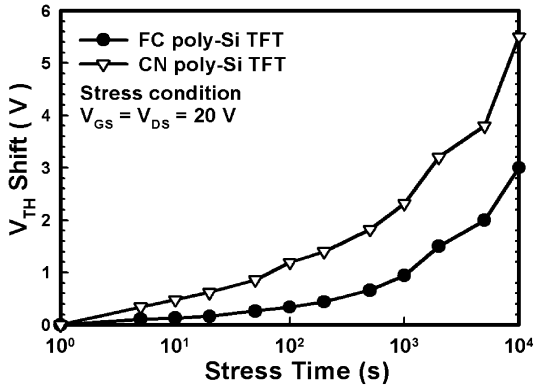

Fig. 7. Variation of threshold voltage versus hot-carrier stress time for the FC and CN poly-Si TFTs.

TEOS oxide makes the silicon atoms barely bound. As a result, the stress formed during the crystallization process could be easily relieved from the free Si surface pursing for fewer nucleation sites, thereby yielding good-quality poly-Si film with lower trap state density and larger poly-Si grain size.

Additionally, hot-carrier stress analysis was applied to investigate the device reliability. The poly-Si TFT devices were bias-stressed at $V_{DS} = 20$ V and $V_{GS} = 20$ V for 10^4 s to examine the hot-carrier stress immunity. The threshold-voltage shifts over hot-carrier stressing time for the FC and CN poly-Si TFTs are shown in Fig. 7. The threshold-voltage shift is defined as $V_{TH,stressed} - V_{TH,initial}$, where $V_{TH,initial}$ and $V_{TH,stressed}$ represent the measured values before and after stress application. Hot-carrier multiplication occurring on the drain side of poly-Si TFT causes the degradation of threshold voltage. The poly-Si TFT with a floating-channel structure shows less degradation in threshold voltage. Notably, the variation of threshold voltage of the FC poly-Si TFT after a stress time of 10^4 s is found to be 3 V, which is superior to that of the CN poly-Si TFT (5.4 V). It has been reported that the degradations of threshold voltage caused by hot-carrier stress could be attributed to two reasons: the generation of interface states at the gate oxide/poly-Si interface and the formation of deep trap states originating from the broken weak Si–H bonds at the grain boundaries.[13] The result indicates that the floating-channel poly-Si film crystallized by SPC is formed with larger grain size accompanied by fewer grain boundaries, exhibiting an improved hot-carrier endurance.

4. Conclusions

In this study, we have demonstrated that the α-Si film with a floating-channel structure crystallized by a solid-phase crystallization process exhibits a better Si grain crystallinity. Poly-Si TFT with the self-aligned formation of the floating-channel active region is firstly proposed. The electrical characteristics, including the threshold voltage, subthreshold swing, field-effect mobility, trap state density, and ON/OFF current ratio, are significantly improved using solid-phase crystallized floating-channel poly-Si film. Superior trap state density and field-effec mobility further confirm that poly-Si with good crystallinity, larger grain size, and fewer micro-structural defects can be realized in the floating-channel structure. In addition, the FC poly-Si TFTs also present higher immunity against the hot-carrier stress owing to the larger poly-Si grain size with fewer grain boundary defects. Therefore, the proposed FC poly-Si TFTs are not only compatible with conventional fabrication processes but also possess superior electrical properties for large flat-panel display applications.

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