Fault Diagnosis for Linear Analog Circuits

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Editor: M. Renovell

Abstract. This paper presents a novel scheme to diagnose single and double faults for linear analog circuits. The scheme first proposes a simple transformation procedure to transform the tested linear analog circuit into a discrete signal flow graph, then constructs "diagnosing evaluators," which model the faulty components, to form a diagnosis configuration to diagnose the faults through digital simulation. This saves much computation time. Furthermore, a simple method to un-power OP's is also proposed to differentiate equivalent faults. The scheme can diagnose faults in passive components as well as active faults in OP's.

Keywords: fault diagnosis, signal flow graph, diagnosing evaluators, un-powered network

1. Introduction

Analog circuit fault diagnosis was studied early from 1962 [2], and lately became a hot research topic because of advent of modern, complex integrated analog circuits and systems. In 1979, Duhamel and Rault presented a review of available analog testing techniques, including the nature of faults and fault models, and various types of tests and diagnosis [6]. In 1985, a review on this topic with 178 references was published [1]. Two basic approaches of analog circuit fault diagnosis are the simulation-before-test (SBT) and the simulation-after-test (SAT) methods [1, 5, 18]. The former approach builds a fault look-up table through simulation and uses the pattern recognition concept to identify and locate faults. The later approach simulates the tested circuit during, or after, the testing time to identify the faulty parameters [8, 9, 11, 15]. In both approaches, the complexity involved and computation time required usually place limit on their applicability. Much research, such as symbolic analysis [7, 16] and sensitivity computation [12, 17], focused on problems of reducing the computational cost. Another approach which treated the signal of the tested circuit in the discrete time domain was presented [12, 13, 19]. For this approach, a discrete time domain tool, DRAFT [13], was developed to map the circuit and faults to the discrete time domain through the bilinear transform and the mapped circuit was then simulated. This saves much computation time.

This work presents a fault diagnosis method which also treats the circuit and signal in the discrete time domain but adopts a new fault diagnosis procedure by creating fault evaluators to compute circuit responses under an appropriate input to locate the fault. The method also uses a simpler relationship in directly mapping the tested analog circuit to the digital circuit. It treats both single and double faults. At the end, it also presents a "power-off" design-for-diagnosibility scheme to help to diagnose the fault(s).

2. Mapping of the Analog Circuit to the Discretized Digital Circuit

A linear analog circuit is usually composed of sub-circuits which themselves are composed of operational amplifiers (OP) in three configurations, i.e., OP with the inverting input, OP with the non-inverting input, and OP with differential inputs. In a linear circuit, each sub-circuit may be connected to each other with several forward or feedback paths. Hence, in considering transforming a linear analog circuit to the discretized digital circuit, we firstly consider the above three sub-circuits.

Fig. 1 shows a sub-circuit with an OP with an inverting input. In the figure, for each path there may exist both resistors and capacitors, and V_1 and V_2 may be outputs fed from the preceding stage or the succeeding stage.

For this sub-circuit, the following circuit equations can be written:

$$\begin{bmatrix} \dfrac{V_1}{R_1} + C_2 \dfrac{dV_{C_2}}{dt} \\ \quad = -\left(\dfrac{V_{\text{out}}}{R_4} + C_6 \dfrac{dV_{C_6}}{dt}\right) \rightarrow \dfrac{V_1(t_n)}{R_1} \\ \qquad + C_2 \dfrac{V_{C_2}(t_n) - V_{C_2}(t_{n-1})}{T} \\ \quad = -\left(\dfrac{V_{\text{out}}(t_n)}{R_4} + C_6 \dfrac{V_{C_6}(t_n) - V_{C_6}(t_{n-1})}{T}\right) \\ V_2 - C_2 R_3 \dfrac{dV_{C_2}}{dt} \\ \quad = V_{C_2} \rightarrow V_2(t_n) - C_2 R_3 \dfrac{V_{C_2}(t_n) - V_{C_2}(t_{n-1})}{T} \\ \quad = V_{C_2}(t_n) \\ V_{\text{out}} - C_6 R_5 \dfrac{dV_{C_6}}{dt} \\ \quad = V_{C_6} \rightarrow V_6(t_n) - C_6 R_5 \dfrac{V_{C_6}(t_n) - V_{C_6}(t_{n-1})}{T} \\ \quad = V_{C_6}(t_n) \end{bmatrix}$$

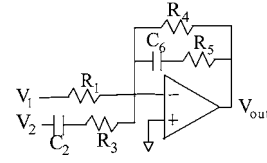*Fig. 1.*   General form of the sub-circuit with the inverting input.

Let $C_1 = \frac{T}{R_1}, C_3 = \frac{T}{R_3}, C_4 = \frac{T}{R_4}$, and $C_5 = \frac{T}{R_5}$, where T is the sampling period of the discretized circuit, then the above equations can be written as:

$$\begin{bmatrix} C_1 V_1(t_n) + C_2\left[V_{C_2}(t_n) - V_{C_2}(t_{n-1})\right] \\ \quad = -\left\{C_4 V_{\text{out}}(t_n) + C_6\left[V_{C_6}(t_n) - V_{C_6}(t_{n-1})\right]\right\} \\ V_2(t_n) - \dfrac{C_2}{C_3}\left[V_{C_2}(t_n) - V_{C_2}(t_{n-1})\right] = V_{C_2}(t_n) \\ V_{\text{out}}(t_n) - \dfrac{C_6}{C_5}\left[V_{C_6}(t_n) - V_{C_6}(t_{n-1})\right] = V_{C_6}(t_n) \end{bmatrix}$$

By z-transformation, they can be transformed to be:

$$\begin{bmatrix} C_1 V_1 + C_2 V_{C_2}(1 - z^{-1}) \\ \quad = -[C_4 V_{\text{out}} + C_6 V_{C_6}(1 - z^{-1})] \\ V_2 - \dfrac{C_2}{C_3}(1 - z^{-1})V_{C_2} = V_{C_2} \\ V_{\text{out}} - \dfrac{C_6}{C_5}(1 - z^{-1})V_{C_6} = V_{C_6} \end{bmatrix}$$

Then

$$V_{\text{out}} = \left[C_1 V_1 + V_2 \dfrac{C_2(1 - z^{-1})}{1 - \left(\frac{-1}{C_3}\right) \times C_2(1 - z^{-1})}\right]$$
$$\times \left\{\dfrac{\left[\frac{-1}{C_6(1-z^{-1})} + \left(\frac{-1}{C_5}\right)\right]}{1 - C_4 \times \left[\frac{-1}{C_6(1-z^{-1})} + \left(\frac{-1}{C_5}\right)\right]}\right\} \quad (1)$$

According to Eq. (1), a signal flow graph in the discrete time domain for the sub-circuit can be drawn as Fig. 2. Comparing Fig. 1 and Fig. 2, we find that R is substituted by $C = T/R$ and the C is substituted by $C(1 - z^{-1})$, and there is a duality relationship between the parallel and series connection.

For the sub-circuit of an OP with a non-inverting input as shown in Fig. 3, a similar procedure can be done to obtain the equivalent transformed signal flow graph as shown in Fig. 4.
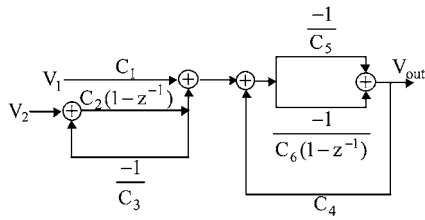
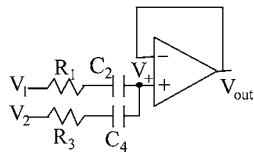Fig. 2. Signal flow of the sub-circuit of Fig. 1

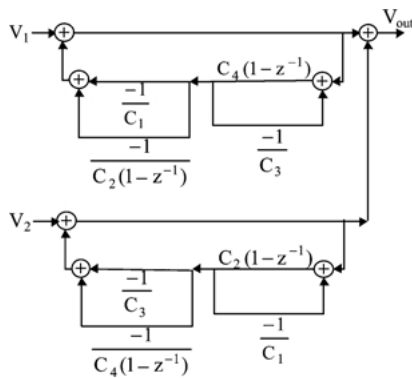Fig. 3. General form of sub-circuit with the non-inverting input.

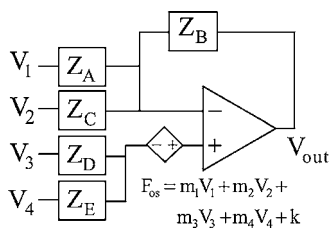Fig. 4. Signal flow graph of the circuit of Fig. 3

Fig. 5. The sub-circuit of the OP with both the differential inputs.

Fig. 5 is a more general sub-circuit with differential inputs, i.e., it is a combination of the sub-circuits of Fig. 1 and Fig. 3. In a similar manner, the signal flow graph of this sub-circuit can be derived to be that of Fig. 6.

In the above sub-circuit circuit, to take into account the fault effects of the OP, an offset voltage is included
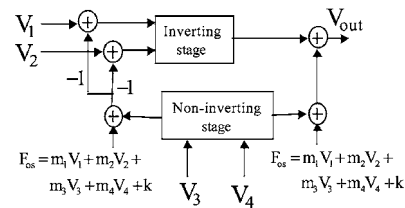

Fig. 6. The transformed signal flow graph of the circuit of Fig. 5.

at the input. This offset voltage represents the fault effects caused by a large percent of catastrophic faults such as transistor "open" and "short" faults and the non-linear max-current-limit fault of the OP [3]. For the offset voltage: $F_{os} = m_1V_1 + m_2V_2 + m_3V_3 + m_4V_4 + k$, $m_1 \sim m_4$ are parameters related with the closed-loop gain [3].

As stated previously, a linear circuit is composed of the above three sub-circuits. Its corresponding transformed signal flow graph in the discrete time domain can be obtained with the derived mapping relationships of the original circuit and the signal flow graphs of the above three sub-circuits. For example, for the benchmark state variable filter circuit [10] of Fig. 7, its discrete signal flow graph is obtained to be that in Fig. 8.

3. Diagnosing Evaluators, Diagnosis Configuration and Selection of Input Stimulus

The faults diagnosed in this work are single parametric faults occurring at passive components such as R's and C's and the transistor faults occurring in OP's. For the passive component faults, they are modeled as a variation, which exceed the specified tolerance, on the values of passive components. The "open" or "short" of a component are treated as that the value of the component is very large or very small respectively. For the
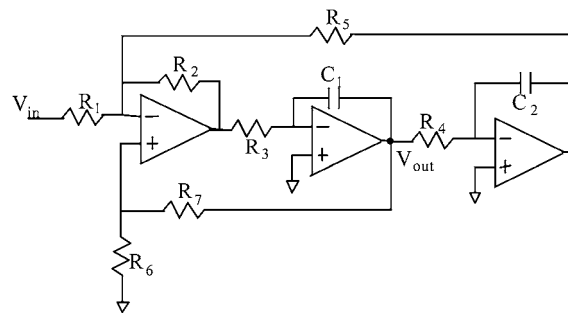

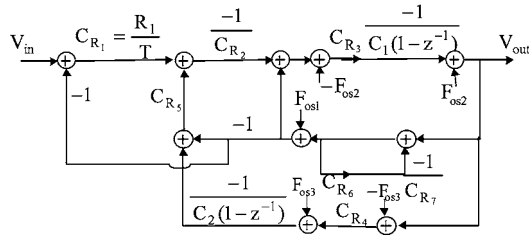Fig. 7. The benchmark state variable filter circuit [10].

Fig. 8. The transformed discrete signal flow graph of the benchmark state variable circuit.

transistor faults occurring within OP's, an offset voltage is put at the input of the OP.

Similar to the conventional diagnosis approach, in this diagnosis scheme, a test input stimulus is applied to the input of the circuit-under-test (CUT), the output response of the CUT is analyzed to find the faulty component. However, the analysis of the faulty response is done in the digital domain with the aid of "diagnosis evaluators," which are to be explained as follows:

When there is a parametric fault occurring at one component, the transformed discretized flow graph of the CUT will be modified to be a "diagnosis evaluator." For the modified flow graph of the faulty CUT, both input stimulus and output response will become inputs of the flow graph, and the faulty component to be diagnosed is the output. If the diagnosed component is the faulty component to be identified, the computed output of the flow graph under the two stimulus and response inputs will be a constant which is the value of the faulty component. If the diagnosed component is not the faulty component to be identified, the output of the flow graph will be a non-constant output. For the computation, the stimulus and response are treated digitally and the computation is performed digitally in the discretized domain. Fig. 9(c) shows a "diagnosis
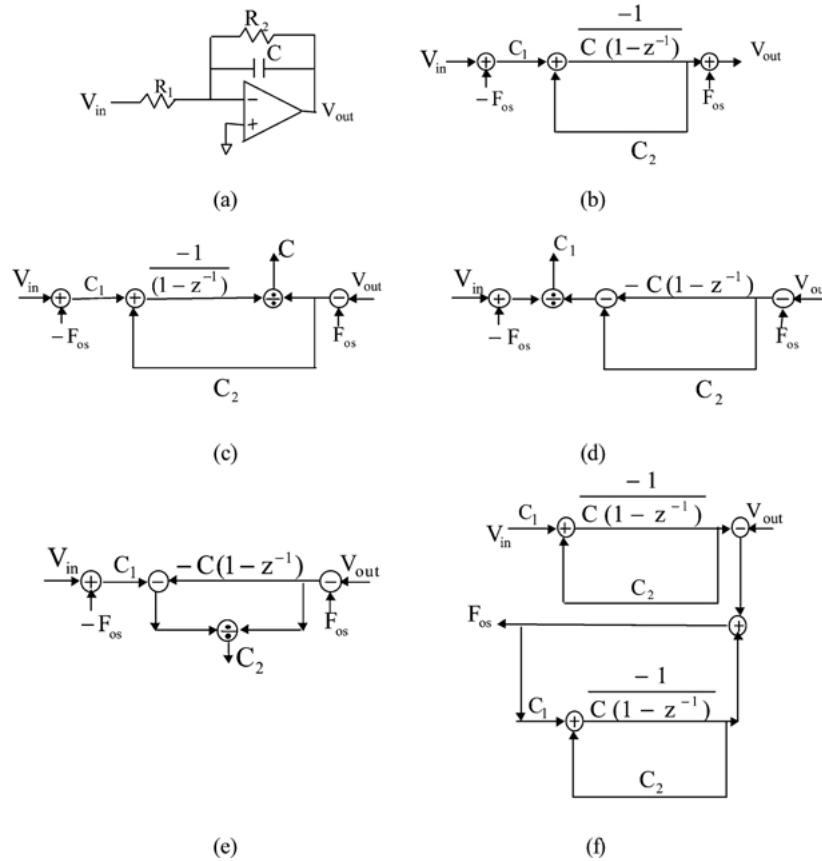

Fig. 9. (a) The low pass filter circuit. (b) The transformed discrete signal graph of low pass filter circuit. (c) The reconstructed "diagnosing evaluator" for the component C. (d) The reconstructed "diagnosing evaluator" for the component C_1. (e) The reconstructed "diagnosing evaluator" for the component C_2. (f) The reconstructed "diagnosing evaluator" for the component F_{OS}.
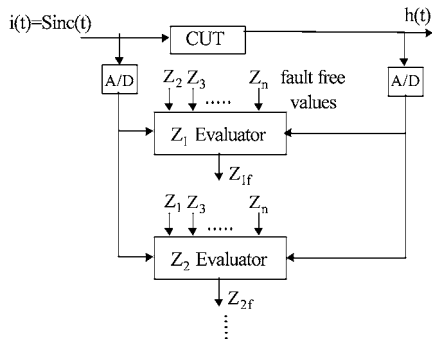
Fig. 10. The diagnosis configuration for single fault diagnosis.

evaluator" for the example circuit of Fig. 9(a) where the passive component C is selected as the diagnosed component. For all the components to be diagnosed, "diagnosis evaluators" can be constructed (Fig. 9) and they are applied the same "discretized" digital stimulus and response inputs to be computed their outputs. The output which shows a constant value is the identified faulty component.

Fig. 10 shows the diagnosis configuration of the scheme, where all the Z_I diagnosis evaluators are connected in parallel and they are fed with both input stimulus $i(t)$ and the output response $h(t)$, which are in the digital form converted from A/D's. For each Z_I evaluator, all components are of fault free values except Z_I which has the faulty value Z_{If}. With $i(t)$ and $h(t)$ as the inputs to each Z_I evaluator, the evaluator

which has the faulty Z_I will give the constant faulty value, Z_{If}, such as that in Fig. 11(a), and the outputs of all other evaluators will give non-convergent values, one example of which is shown in Fig. 11(b).

To reveal a fault in the original circuit, an appropriate test pattern which activates the fault is required. However, there are many different faults, which may require different input stimuli to activate. In this scheme, a signal of Sinc function, $f(x) = \text{sinc}(x) = \frac{\sin(2\pi f x)}{\pi x}$, which has a constant low-pass spectrum, is used as the input test stimulus. The bandwidth, f, of the function is chosen to be an appropriate value to cover the bandwidth of CUT. This insures that all the faults of CUT can be activated by this signal.

4. Diagnosing for Double Faults

This scheme is also able to diagnose multiple faults. However, multiple faults are more difficult to be diagnosed because of the exceedingly large number of fault combinations and the amount of computation efforts involved. In this section, the diagnosis for double faults is presented since it needs relatively affordable computation efforts.

The fault diagnosis configuration for double faults (Z_{af}, Z_{bf}) is shown in Fig. 12. In the figure, the diagnosing evaluators Z_a and Z_b are the same as those of the previous section except that for Z_a evaluator, its Z_b input is not the fault free value but a value of Z_{bf} which is the computed value from the Z_b evaluator, and
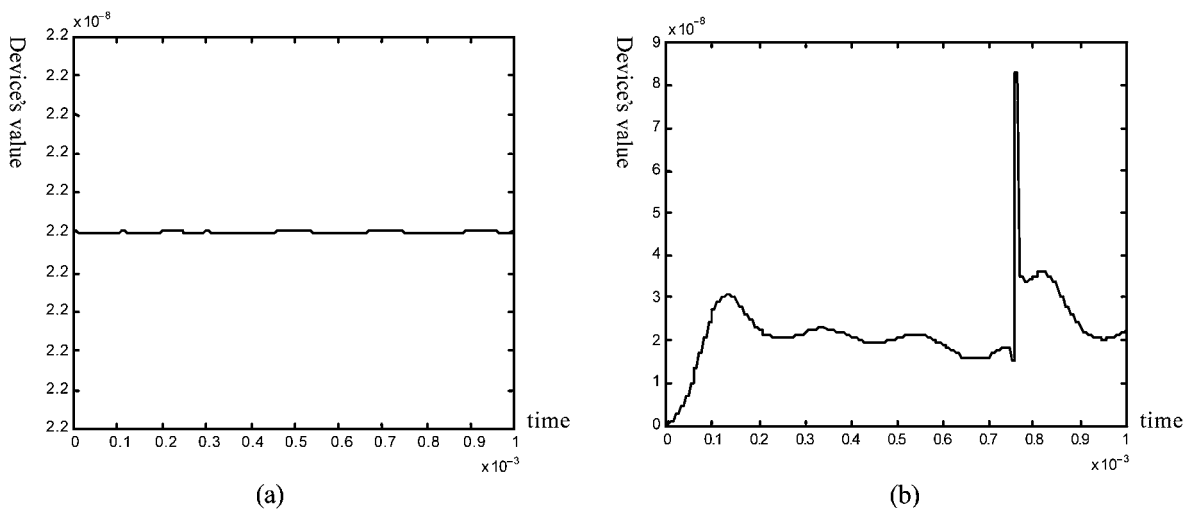

Fig. 11. (a) The matched convergent output waveform at Z_I evaluator, and (b) The unmatched divergent output waveform at other Z evaluators.
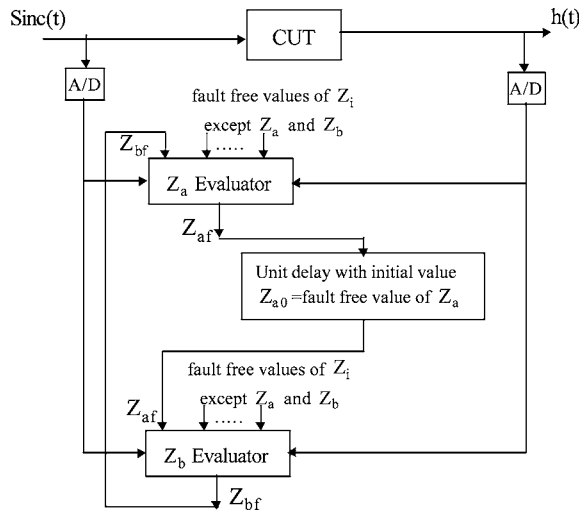
Fig. 12.   Computation configuration for diagnosing double faults.

for Z_b evaluator, its Z_a input is not the fault free value but a value of Z_{af} which is the computed value from the Z_a evaluator. A delay unit is inserted between two evaluators. The computing is an iterative process. At the beginning, when the value of Z_{af} is computed, the fault free value of Z_b is placed at the input of Z_a evaluator. The obtained Z_{af} is then fed to the input of the Z_b evaluator at the next time unit for Z_{bf} computation. The obtained Z_{bf} is again put at the Z_{bf} input of the Z_a evaluator for the next computation. This process is iterated until stable Z_{af} and Z_{bf} values are obtained. If the output waveforms of evaluators do not converge after a preset iteration run, the double fault-pair selected is not the fault-pair and another fault-pair will be selected.

For a double fault-pair, there are usually other double fault-pairs which give the same faulty response. These fault pairs are equivalent fault-pairs. In the following, a power-down method using switched-opamp [4] is used to differentiate the true fault-pair from their equivalent fault-pairs.

A linear analog circuit is composed of several sub-circuits which are constituted by OPs. When the power of OPs is shut down, the inputs of OPs are open circuit, i.e., OPs in the circuit will act as a high impedance. The circuit becomes a circuit composed of only passive elements. For example, in the above benchmark filter circuit example, the CUT becomes an un-powered passive RC network. The un-powered passive RC network with double faults can be applied with the same input stimulus to obtain its output response. The input stimulus and output response are then *A/D* transformed and applied to the similar evaluator configuration but with evaluators of different equivalent fault-pairs as in Fig. 13. The true fault-pair will cause the output of the comparator to be zero. In this way, the true fault pair is identified.

Table 1.   The diagnosed single faults and results.

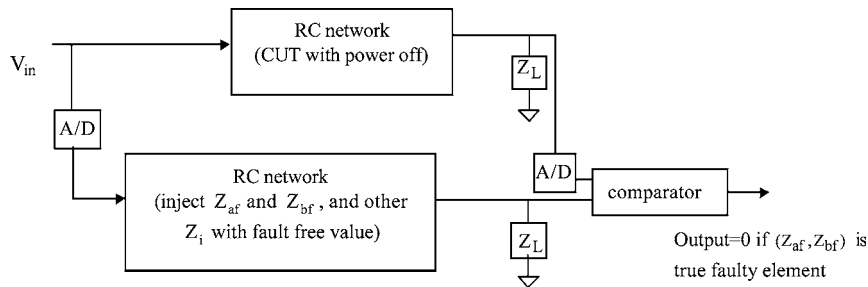| Faults	Diagnosis result
R_1 open($R_1 = 100M$)	$R_1 = 100M$
R_1 short($R_1 = 10$)	$R_1 = 10$
R_2 open($R_2 = 100M$)	$R_2 = 100M$
R_2 short($R_2 = 10$)	$R_2 = 10$
C open	$C \approx 0$
C short	$C \approx \infty$
$R_1 = 7.5M(+50\%)$	$R_1 = 7.5M$
$R_2 = 7.5M(-25\%)$	$R_2 = 7.5M$
$C = 7.5p(-25\%)$	$C = 7.5p$
OP fault: $F_{os} = 0.15V$	$F_{os} = 0.15V$
$R_1 = 7.5M(+50\%)$	$(R_1 = 7.5M, R_2 = 7.5M)$ or
$R_2 = 7.5M(-25\%)$	$(R_2 = 5M, C = 15p)$ or
	$(R_1 = 10M, C = 7.5p)$
•	•
•	•

Fig. 13.   Configuration for differentiating the true fault pair from its equivalent faults.

5. Examples

5.1. A Low Pass Filter

A low pass filter of Fig. 9 is used to demonstrate the proposed diagnosis method. For this circuit, $C = 10\,\mathrm{pF}$, $R_1 = 5\,\mathrm{M\Omega}$, $R_2 = 10\,\mathrm{M\Omega}$, and input stimulus is 0.1 Sinc(40 kHz) since the cut-off frequency of the filter is 10 kHz. The circuit is transformed to the discrete signal flow graph and the diagnosis evaluators for each component are constructed by the method described in the previous section. The faults dealt with are those listed in Table 1 and the corresponding diagnosed results after computation are also compiled.

Fig. 14 shows the simulated waveforms at the output of evaluators C, R_1 and R_2 respectively for the single fault (R_2). The waveforms in Fig. 14 (a) and (b) do not exhibit constant curves but (c) gives a constant value of 7.5M, indicating that R2 is the faulty element with a faulty value of 7.5M. Fig. 15 shows the simulated waveforms at the output of diagnosing evaluators (R_1, R_2) respectively for the double fault (R_1, R_2). Initially, the waveforms vary with time but eventually become constant values of 7.5M respectively, indicating
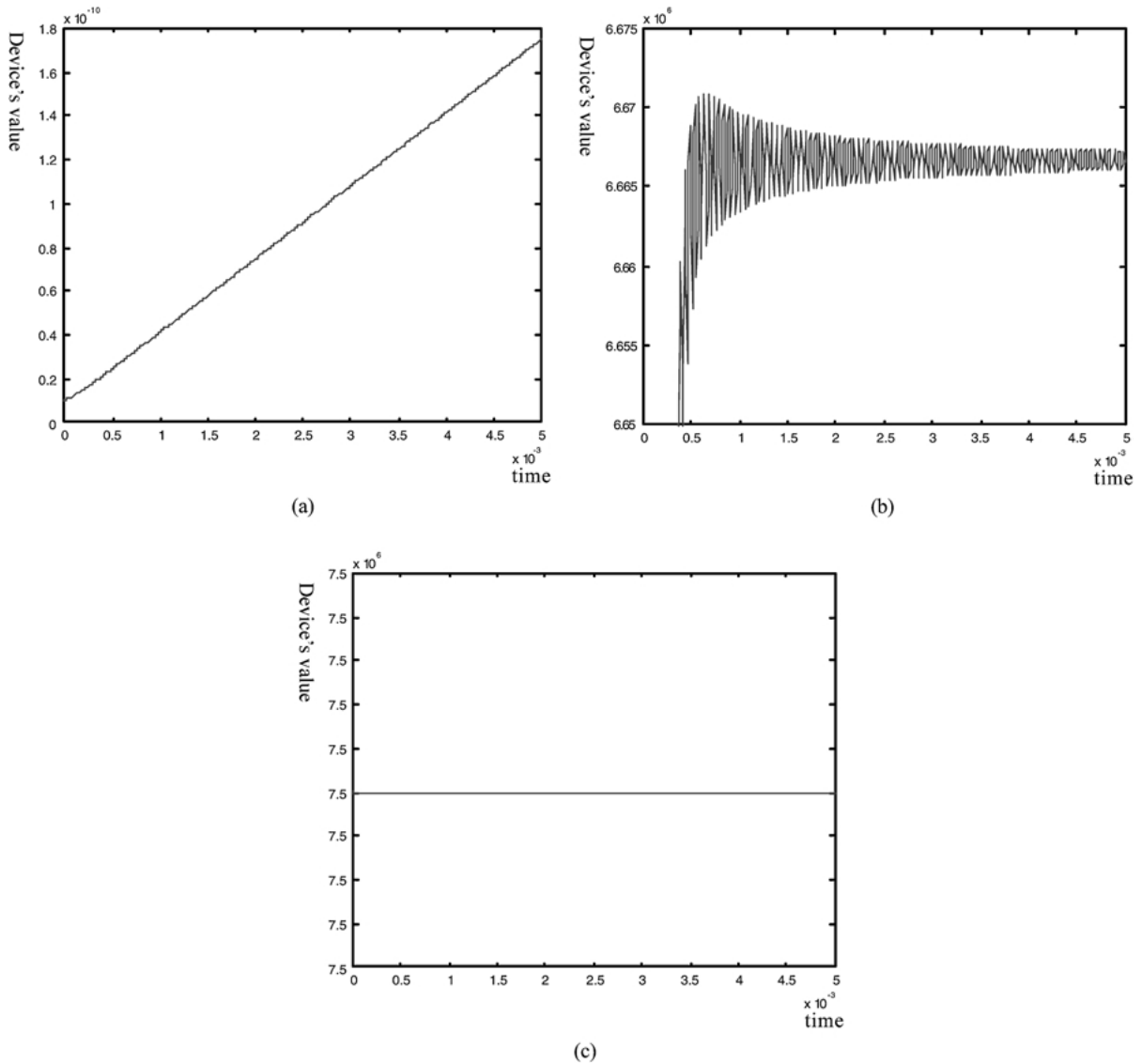

Fig. 14.   Simulated waveforms of single fault R_2 at the output of (a) evaluator C, (b) evaluator R_1, (c) evaluator R_2.
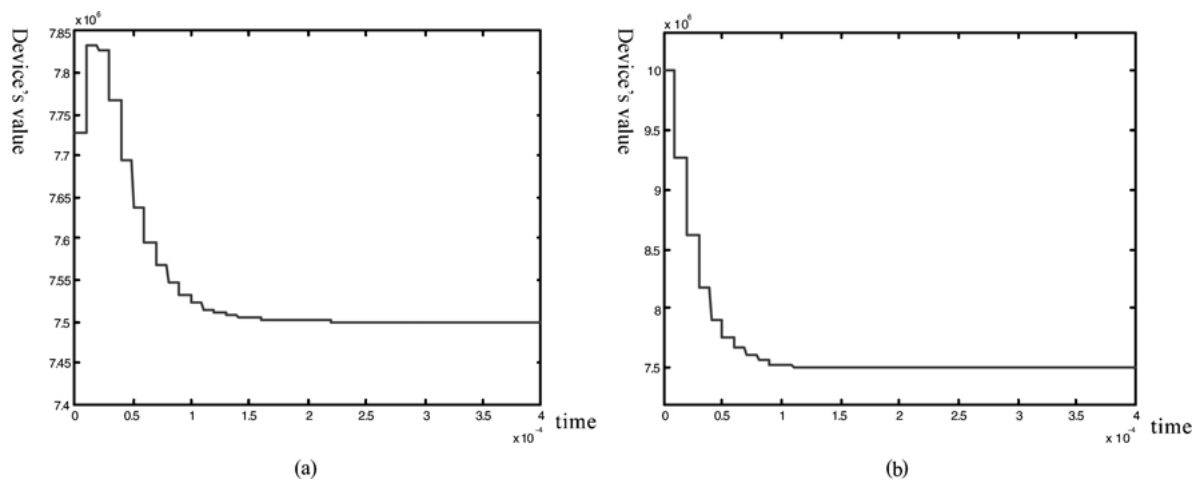
Fig. 15. Simulated waveforms of double fault ($R1, R_2$) at output of evaluator (R_1, R_2) (a) R_1 and (b) R_2.

that the double faults with faulty values of 7.5M respectively are diagnosed.

In the above example, the computation time spent for the iteration process to obtain convergent waveforms was only 0.15 msec when the sample rate of A/D was 100 kHz.

Also, the power-down method of the previous section to differentiate the equivalent double fault-pairs was applied to identify the true fault-pair. Fig. 16 shows the waveforms at two evaluators of an equivalent double fault-pair with those at the evaluators of the true fault-pair. The equivalent fault-pair outputs have non-zero curves but the true fault-pair shows a zero output. Clearly, the true fault-pair is identified.

In all above discussions, all components are assumed to be good, i.e., they have well-defined values except the faulty compone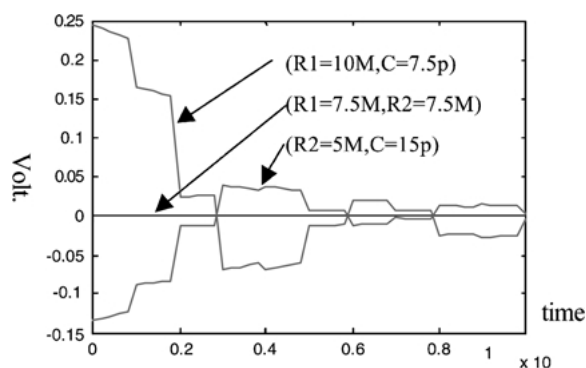nts. In practice, all components may have small tolerances on their component values. In that case, the outputs of evaluators will not converge into a constant but vary within a small range. In computation, a small tolerance range can be firstly preset as the range of convergence. Once the computation result falls into this preset tolerance range, the curves can be considered to have reached constant. For example, if there are a 5% variation on R_1, i.e. 5.25M and C, i.e. 10.5 pf when the 50% soft fault on R_2, i.e. 7.5M, is diagnosed, the simulated waveforms at outputs of C, R_1 and R_2 evaluators are those shown in Fig. 17. The waveform in Fig. 17(c) varies in a small range as compared to that of Fig. 14(c). The average value of R_2 is 7.17M, where there is only a 4.4% error as compared to true faulty value of $R_2 = 7.5$M.

5.2. *The Benchmark State Variable Filter Circuit Example [10]*

The benchmark state variable filter circuit of Fig. 7 is used as another example to demonstrate the proposed diagnosis method.

For this circuit, $C_1 = 20$ nF, $C_2 = 20$ nF, $R_1 - R_5 = 10$ kΩ, $R_6 = 3$ kΩ, $R_7 = 7$ kΩ, and the input stimulus was 0.1Sinc (10 kHz) for the central frequency of band-pass output of this filter is 795 Hz. The circuit is transformed to the discrete signal flow graph as shown in Fig. 8. All evaluators for each component are constructed by the method described as above. The single faults to be diagnosed are components with 10% variation in their values as shown in Table 2 with the diagnosed result through computation. Table 3 shows the double faults and the diagnosed results.

Fig. 16. Waveforms at two evaluators of two different equivalent fault pairs as compared with that of the true double fault-pair (R_1, R_2).

Table 2.   The diagnosed single faults and results.

Fault	Diagnosis result
$C_1 = 22n(+10\%)$	$C_1 = 22n$ or $R_3 = 11k$
$C_2 = 22n(+10\%)$	$C_2 = 22n$ or $R_4 = 11k$
$R_1 = 11k(+10\%)$	$R_1 = 11k$
$R_2 = 11k(+10\%)$	$R_2 = 11k$
$R_3 = 11k(+10\%)$	$C_1 = 22n$ or $R_3 = 11k$
$R_4 = 11k(+10\%)$	$C_2 = 22n$ or $R_4 = 11k$
$R_5 = 11k(+10\%)$	$R_5 = 11k$
$R_6 = 3.3k(+10\%)$	$R_6 = 3.3k$ or $R_7 = 6.364k$
$R_7 = 7.7k(+10\%)$	$R_7 = 7.7k$ or $R_6 = 2.727k$

In tables, the diagnosed equivalent faults and the equivalent fault pairs are also listed with the diagnosed values of each faulty component respectively. It can be seen that every fault is diagnosed and the diagnosed faulty values are the same as the injected faulty values. The iteration processes of all the faults converged within 2.5 msec when the sample rate of *A/D* was 100 kHz. For almost each single fault and double fault, there are equivalent faults and many equivalent fault-pairs respectively. If the power-down differentiation method is applied to identify the true faults, the obtained diagnosed faults are shown in Table 4. All the true single faults and most of the double fault-pairs are identified.
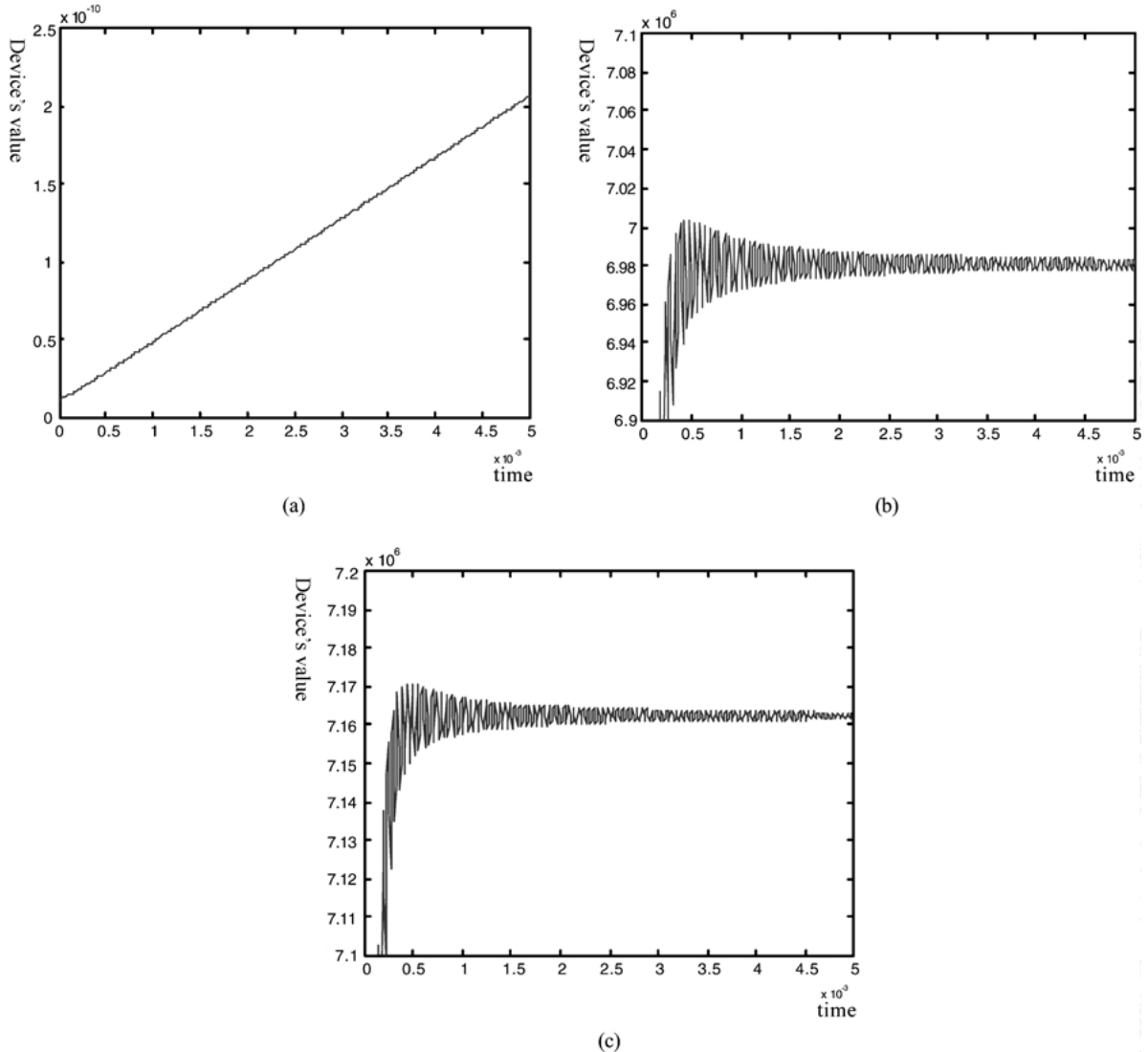

Fig. 17.   Simulated waveforms of single fault $R_2(50\%)$ with $R_1(5\%)$ and $C(5\%)$ at the output of (a) evaluator C, (b) evaluator R_1, (c) evaluator R_2.

Table 3.   The diagnosed double faults and equivalent fault pairs.

Fault	Diagnosis result (Equivalent fault pairs)
$C_1 = 22n, C_2 = 22n$	$(C_1 = 22n, C_2 = 22n)(C_1 = 22n, R_4 = 11k)(C_2 = 22n, R_3 = 11k)(R_3 = 11k, R_4 = 11k)$
$C_1 = 22n, R_1 = 11k$	$(C_1 = 22n, R_1 = 11k)(R_1 = 11k, R_3 = 11k)$
$C_1 = 22n, R_2 = 11k$	$(C_1 = 22n, R_2 = 11k)(C_1 = 20n, R_6 = 2.872k)(C_1 = 20n, R_7 = 7.313k)$
	$(C_2 = 18.18n, R_5 = 11k)(C_2 = 20n, R_6 = 2.872k)(C_2 = 20n, R_7 = 7.313k)$
	$(R_1 = 10k, R_6 = 2.872k)(R_1 = 10k, R_7 = 7.313k)(R_2 = 11k, R_3 = 11k)$
	$(R_2 = 10k, R_6 = 2.872k)(R_2 = 10k, R_7 = 7.313k)(R_3 = 10k, R_6 = 2.872k)$
	$(R_3 = 10k, R_7 = 7.313k)(R_4 = 9.091k, R_4 = 11k)(R_4 = 10k, R_6 = 2.872k)$
	$(R_4 = 10k, R_7 = 7.313k)(R_5 = 10k, R_6 = 2.872k)(R_5 = 10k, R_7 = 7.313k)$
	$(R_6 = 2.872k, R_7 = 7k)$
$C_1 = 22n, R_3 = 11k$	$(C_1 = 24.2n, C_2 = 20n)(C_1 = 24.2n, R_1 = 10k)(C_1 = 20n, R_3 = 12.1k)$
	$(C_1 = 24.2n, R_4 = 10k)(C_1 = 24.2n, R_5 = 10k)(C_1 = 24.2n, R_6 = 3k)$
	$(C_1 = 24.2n, R_7 = 7k)(C_2 = 20n, R_3 = 12.1k)(R_1 = 10k, R_3 = 12.1k)$
	$(R_2 = 10k, R_3 = 12.1k)(R_2 = 8.264k, R_6 = 2.73k)(R_2 = 8.264k, R_6 = 7.7k)$
	$(R_3 = 12.1k, R_4 = 10k)(R_3 = 12.1k, R_5 = 10k)(R_3 = 12.1k, R_6 = 3k)$
	$(R_3 = 12.1k, R_7 = 7k)$
$C_1 = 22n, R_4 = 11k$	$(C_1 = 22n, C_2 = 22n)(C_1 = 22n, R_4 = 11k)(C_2 = 22n, R_3 = 11k)(R_3 = 11k, R_4 = 11k)$
$C_1 = 22n, R_5 = 11k$	$(C_1 = 22n, R_5 = 11k)(R_3 = 11k, R_5 = 11k)$
$C_1 = 22n, R_6 = 3.3k$	$(C_1 = 18.274n, R_2 = 8.306k)(C_1 = 22n, R_6 = 3.3k)(C_1 = 22n, R_7 = 6.364k)$
	$(R_2 = 8.306k, R_6 = 9.137k)(R_2 = 9.1k, R_6 = 3.146k)(R_2 = 9.1k, R_7 = 6.676k)$
	$(R_3 = 11k, R_6 = 3.3k)(R_3 = 11k, R_7 = 6.364k)$
$C_1 = 22n, R_7 = 7.7k$	$(C_1 = 27.37n, R_2 = 12.44k)(C_1 = 22n, R_6 = 2.73k)(C_1 = 22n, R_7 = 7.7k)$
	$(R_2 = 12.44k, R_6 = 13.686k)(R_2 = 9.1k, R_6 = 2.607k)(R_2 = 9.1k, R_7 = 8.06k)$
	$(R_3 = 11k, R_6 = 2.73k)(R_3 = 11k, R_7 = 7.7k)$
$C_2 = 22n, R_1 = 11k$	$(C_1 = 18.335n, R_2 = 8.333k)(C_1 = 22n, R_6 = 3.294k)(C_1 = 22n, R_7 = 6.375k)$
	$(C_2 = 22n, R_1 = 11k)(R_1 = 11k, R_4 = 11k)(R_2 = 8.333k, R_3 = 9.167k)$
	$(R_2 = 9.091k, R_6 = 3.14k)(R_2 = 9.091k, R_7 = 6.69k)(R_3 = 11k, R_6 = 3.294k)$
$C_2 = 22n, R_2 = 11k$	$(C_1 = 18.335n, R_2 = 8.333k)(C_1 = 22n, R_6 = 3.294k)(C_1 = 22n, R_7 = 6.375k)$
	$(C_2 = 22n, R_1 = 11k)(R_1 = 11k, R_4 = 11k)(R_2 = 8.333k, R_3 = 9.167k)$
	$(R_2 = 9.091k, R_6 = 3.14k)(R_2 = 9.091k, R_7 = 6.69k)(R_3 = 11k, R_6 = 3.294k)$
	$(R_3 = 11k, R_7 = 6.375k)$
$\bullet$	$\bullet$
$\bullet$	$\bullet$
$\bullet$	$\bullet$
$\bullet$	$\bullet$
$\bullet$	$\bullet$
$\bullet$	$\bullet$

For some fault-pair, either they could not be identified or unable to be diagnosed at all such as fault-pair (C_1, R_3), (C_2, R_4), and (R_6, R_7). There is only multiplication relation between C_1 and R_3 in circuit transfer function. In other word, C_1 and R_3 are linear-dependent diagnosing variables. The same as C_2, R_4 and R_6, R_7, they are linear-dependent diagnosing variables.

Table 4.   Identified results of equivalent faults.

Fault	Diagnosis result	Fault	Diagnosis result
$C_1 = 22n(+10\%)$	$C_1 = 22n$	$R_4 = 11k(+10\%)$	$R_4 = 11k$
$C_2 = 22n(+10\%)$	$C_2 = 22n$	$R_5 = 11k(+10\%)$	$R_5 = 11k$
$R_1 = 11k(+10\%)$	$R_1 = 11k$	$R_6 = 3.3k(+10\%)$	$R_6 = 3.3k$
$R_2 = 11k(+10\%)$	$R_2 = 11k$	$R_7 = 7.7k(+10\%)$	$R_7 = 7.7k$
$R_3 = 11k(+10\%)$	$R_3 = 11k$		
$C_1 = 22n, C_2 = 22n$	$(C_1 = 22n, C_2 = 22n)$	$R_1 = 11k, R_5 = 11k$	$(R_1 = 11k, R_5 = 11k)$
$C_1 = 22n, R_1 = 11k$	$(C_1 = 22n, R_1 = 11k)$	$R_1 = 11k, R_6 = 3.3k$	$(R_1 = 11k, R_6 = 3.3k)$
$C_1 = 22n, R_2 = 11k$	$(C_1 = 22n, R_2 = 11k)$	$R_1 = 11k, R_7 = 7.7k$	$(R_1 = 11k, R_7 = 7.7k)$
$C_1 = 22n, R_3 = 11k$	Failure	$R_2 = 11k, R_3 = 11k$	$(R_2 = 11k, R_3 = 11k)$
$C_1 = 22n, R_4 = 11k$	$(C_1 = 22n, R_4 = 11k)$ $(C_2 = 22n, R_3 = 11k)$	$R_2 = 11k, R_4 = 11k$	$(R_2 = 11k, R_4 = 11k)$
$C_1 = 22n, R_5 = 11k$	$(C_1 = 22n, R_5 = 11k)$	$R_2 = 11k, R_5 = 11k$	$(R_2 = 11k, R_5 = 11k)$
$C_1 = 22n, R_6 = 3.3k$	$(C_1 = 22n, R_6 = 3.3k)$	$R_2 = 11k, R_6 = 3.3k$	$(R_2 = 11k, R_6 = 3.3k)$
$C_1 = 22n, R_7 = 7.7k$	$(C_1 = 22n, R_7 = 7.7k)$	$R_2 = 11k, R_7 = 7.7k$	$(R_2 = 11k, R_7 = 7.7k)$
$C_2 = 22n, R_1 = 11k$	$(C_2 = 22n, R_1 = 11k)$	$R_3 = 11k, R_4 = 11k$	$(R_3 = 11k, R_4 = 11k)$
$C_2 = 22n, R_2 = 11k$	$(C_2 = 22n, R_2 = 11k)$	$R_3 = 11k, R_5 = 11k$	$(R_3 = 11k, R_5 = 11k)$
$C_2 = 22n, R_3 = 11k$	$(C_1 = 22n, R_4 = 11k)$ $(C_2 = 22n, R_3 = 11k)$	$R_3 = 11k, R_6 = 3.3k$	$(R_3 = 11k, R_6 = 3.3k)$
$C_2 = 22n, R_4 = 11k$	Failure	$R_3 = 11k, R_7 = 7.7k$	$(R_3 = 11k, R_7 = 7.7k)$
$C_2 = 22n, R_5 = 11k$	$(C_2 = 22n, R_5 = 11k)$	$R_4 = 11k, R_5 = 11k$	$(R_4 = 11k, R_5 = 11k)$
$C_2 = 22n, R_6 = 3.3k$	$(C_2 = 22n, R_6 = 3.3k)$	$R_4 = 11k, R_6 = 3.3k$	$(R_4 = 11k, R_6 = 3.3k)$
$C_2 = 22n, R_7 = 7.7k$	$(C_2 = 22n, R_7 = 7.7k)$	$R_4 = 11k, R_7 = 7.7k$	$(R_4 = 11k, R_7 = 7.7k)$
$R_1 = 11k, R_2 = 11k$	$(R_1 = 11k, R_2 = 11k)$	$R_5 = 11k, R_6 = 3.3k$	$(R_5 = 11k, R_6 = 3.3k)$
$R_1 = 11k, R_3 = 11k$	$(R_1 = 11k, R_3 = 11k)$	$R_5 = 11k, R_7 = 7.7k$	$(R_5 = 11k, R_7 = 7.7k)$
$R_1 = 11k, R_4 = 11k$	$(R_1 = 11k, R_4 = 11k)$	$R_6 = 3.3k, R_7 = 7.7k$	Failure

6. Conclusion

In this paper, we have proposed an efficient method for diagnosing single and double faults for the linear analog circuit. The method first transforms the CUT into the equivalent discrete time signal flow graph and then constructs "diagnosing evaluators" which models the effect of the faulty components to form a diagnosis configuration to diagnose the circuit. It then computes for the faulty components by treating the blocks in the diagnosis configuration as digital blocks and performs the computation in the digital domain. This saves the computation time significantly as compared with the computation time if done in the analog domain. To differentiate equivalent faults, it offers a simple technique to un-power OP's and treats the CUT as a passive circuit to identify the true faulty components. The method can diagnose the faults in the passive components as well as hard faults in OP's. The method has been applied to diagnose the faults of a benchmark filter circuit and very good results have been obtained. In addition, the transformation method for transforming the linear analog circuits into discretized time domain signal flow graph is very simple and is able to be applied to other discrete time applications when the similar transform is needed.

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