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A GaAs/AlAs Wet Selective Etch Process for the Gate Recess of GaAs Power Metal-Semiconductor Field-Effect Transistors

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A highly selective wet chemical etch process for gate recess of the GaAs power metal–semiconductor field effect transistors (MESFETs) was developed. The power MESFETs used in this study were epitaxially grown devices with a 20 Å AlAs etch-stop layer for gate recess. The selective etch process using citric acid/potassium citrate/hydrogen peroxide solution was studied. A selectivity better than 3800:1 was achieved for GaAs/AlAs layers. This selective etch was applied both to high-power, high-voltage power MESFETs and low-voltage large-periphery power MESFETs. For high-power applications, the 14.7 mm device had a breakdown voltage of 22 V. When tested at 1.88 GHz with a drain bias of 10 V, it provided a maximum output power of 38.8 dBm and a maximum power-added efficiency of 52.5%. For low-voltage applications, the 19.8 mm device was tested under IS-95 code-division multiple access (CDMA) modulation at 1.88 GHz with a drain bias of 3.5 V. Under CDMA modulation, the device showed an output power of 28.03 dBm with an adjacent channel power rejection of −29.6 dBc at 1.25 MHz offset frequency. Both devices also showed excellent uniformity in pinch-off voltages.
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Gate recess plays an important role in manufacturing of field-effect transistors (FETs)[1-6] such as metal-semiconductor field-effect transistors (MESFETs)[1-2] and high-electron-mobility transistors (HEMTs).[3-6] The gate recess process is one of the major factors to affect the uniformity of devices. It is well known that power MESFETs are very sensitive to surface states and defect traps in the channel region. The gate recess step in the power MESFET process must be uniform and free from creating surface states and defect traps. Nonselective wet chemical etch has been studied for the gate recess process of the pseudomorphic HEMTs.[7] However, the nonselective etch has a problem with uniformity control. The uniform gate-recess process is essential to manufacture the GaAs MESFETs and HEMTs as well as monolithic microwave integrated circuits (MMICs). The use of the selective etch in the gate recess process is a good approach to improve uniformity of transistors.

There have been many efforts reported for the selective etch of III-V compound semiconductors.[8-12] The selectivity for GaAs/$Al_{0.3}Ga_{0.7}As$ was found to be 95 when the volume ratio of the citric acid/hydrogen peroxide etch solution was 10:1.[8] Selectivity study involving citric acid/hydrogen peroxide was also conducted for the GaAs-based and InP-based material systems.[9] The selectivity for GaAs/$Al_{0.3}Ga_{0.7}As$ was 116. Citric acid/ammonium hydroxide/hydrogen peroxide solution was used for selective etch of GaAs/$Al_{0.22}Ga_{0.78}As$ to obtain a selectivity of 200.[10] Succinic acid/hydrogen peroxide was reported for the selective etch of $Al_xGa_{1-x}As$.[11] However, neither uniformity data nor FET characteristics were reported.[8-11] Recently, Kitano *et al.* obtained uniformity data of threshold voltage for a 100 μm wide conventional GaAs/AlGaAs MESFET using a wet selective etch process and citric acid/hydrogen peroxide solution.[12] The detailed device characteristics, however, were not revealed. Moreover, small devices are not applicable to modern power applications.

For power MESFETs used in modern low-voltage wireless applications, the devices usually have very large periphery and low impedance.[2] It is desired that the devices have uniform pinch-off voltage for easy circuit matching and manufacturing. Uniformity control is extremely important and difficult for the advanced power FETs which have large periphery to deliver enough power. In addition, for high-power GaAs MESFETs, it is desired that the devices have high breakdown voltage so that the devices can be used at high drain voltage to maintain high output power and high power efficiency. Therefore, the gate recess in the power MESFETs must maintain a smooth profile in the recessed area to avoid high electrical field buildup and achieve high breakdown voltage.

In this work, a high-selectivity wet chemical etch process using citric acid/potassium citrate/hydrogen peroxide solution and AlAs etch-stop layer for gate recess was developed for power MESFETs with large periphery. A double-gate recess process was used to improve the breakdown voltage. Not only the uniformity data but also device characteristics including dc and radio frequency (rf) characteristics were exhibited. The devices developed in this work demonstrated high breakdown voltages and very uniform pinch-off voltages.

Device Structure

As shown in Fig. 1, the material structure of the MESFET was grown by the molecular beam epitaxy (MBE) on a 3 in. (100)-orient-

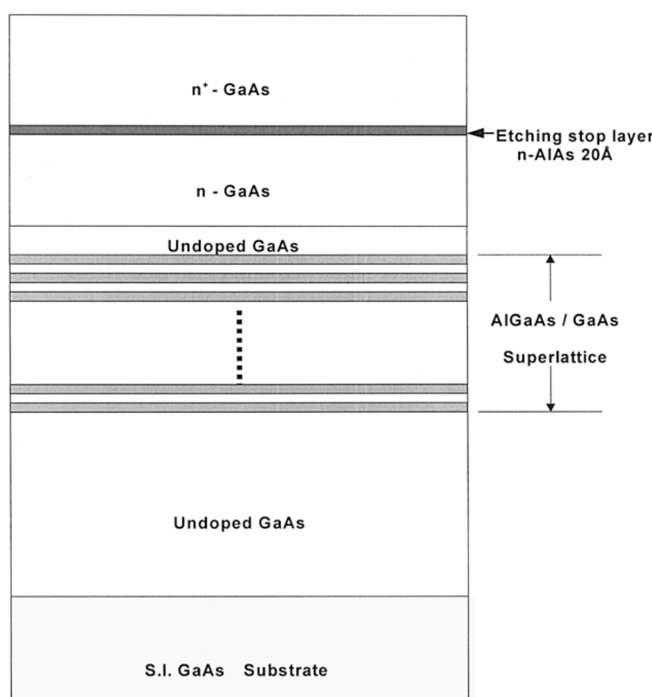

Figure 1. Schematic epitaxial structure of the GaAs power MESFET.

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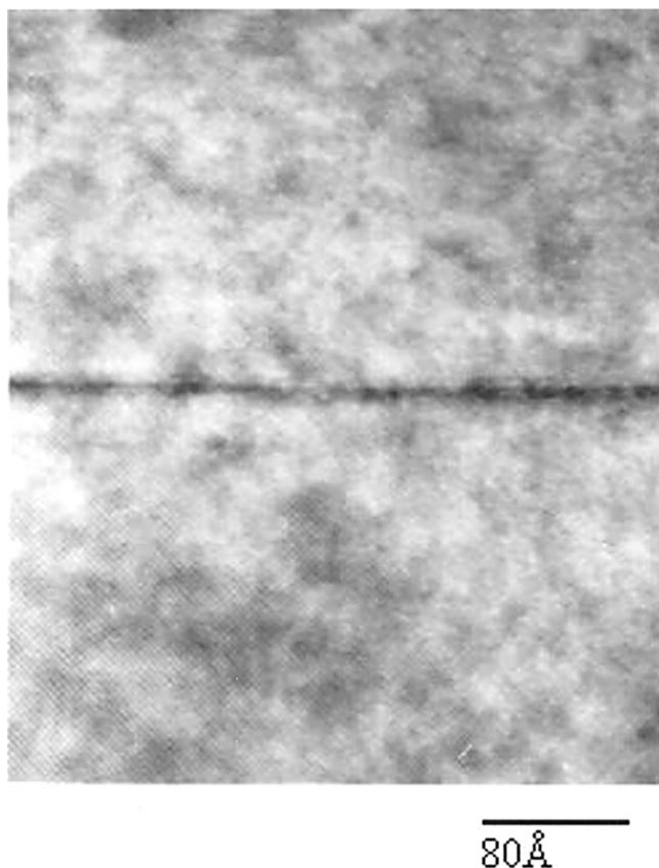

Figure 2. TEM photograph of AlAs etch-stop layer between GaAs layers.

ed semi-insulating GaAs substrate. An undoped GaAs buffer layer, an undoped AlGaAs/GaAs superlattice buffer, and then an undoped GaAs buffer were sequentially grown on the substrate. The AlGaAs/GaAs superlattice buffer suppressed carrier injection between the GaAs channel and the undoped GaAs substrate. The active channel of the structure was an n-doped GaAs layer with $2 \times 10^{17}/cm^3$ doping concentration. A 20 Å AlAs etch-stop layer was grown on top of the channel layer to obtain a uniform gate recess control. A heavily silicon-doped GaAs layer was grown on top of the AlAs layer to provide good ohmic contact and reduce source resistance.

GaAs/AlAs Selective Etch

Selective etch of the GaAs/AlAs materials was studied using different combinations of the citric-based etching solutions. Figure 2 shows the transmission electron microscope (TEM) photograph of the epitaxial structure of the samples used for selectivity study. The samples had a 1 μm GaAs buffer layer followed by a 12 Å AlAs etch-stop layer and 1500 Å GaAs on the top. Different compositions of the citric acid/hydrogen peroxide ($C_6H_8O_7{\cdot}H_2O{:}H_2O_2$) solution and citric acid/potassium citrate/hydrogen peroxide (1 M $C_6H_8O_7{\cdot}H_2O$:1 M $K_3C_6H_5O_7{\cdot}H_2O{:}H_2O_2$) solution were used for the GaAs/AlAs selective etch study. The samples for etch test were first cleaned by immersing in acetone and isopropyl alcohol, respectively, for 5 min. It was observed that the etch rate for each sample was nonaffected by stirring of the etch solutions but changed with temperature. In addition, the etch depth was linearly proportional to the etch time and the etch rate was strongly dependent on the relative proportions of the etch solutions. Therefore, the etch mechanisms for both citric acid/hydrogen peroxide and citric acid/potassium citrate/hydrogen peroxide solutions were reaction-rate limited.

For citric acid/hydrogen peroxide solution, the composition of $C_6H_8O_7{\cdot}H_2O{:}H_2O_2 = 7{:}1$ had the maximum selectivity in our study. The selectivity at this composition was 600. For citric acid/potassium citrate/hydrogen peroxide solution, higher selectivity was obtained. Figure 3 shows the etch depth *vs.* etch time for the composition of 1 M $C_6H_8O_7{\cdot}H_2O$:1 M $K_3C_6H_5O_7{\cdot}H_2O{:}H_2O_2 = 5{:}5{:}2$. The etch depth was measured by the scanning electron microscopy (SEM). Each sample was etched in the solution for an individual given time. The different data points correspond to the different samples, respectively. As can be seen from this figure, the solution etched through the 1500 Å GaAs top layer immediately with an etch rate higher than 40 Å/s, and it took more than 20 min to etch through the 12 Å AlAs layer. The selectivity of GaAs/AlAs using 1 M $C_6H_8O_7{\cdot}H_2O$:1 M $K_3C_6H_5O_7{\cdot}H_2O{:}H_2O_2 = 5{:}5{:}2$ solution was higher than 3800 in this study.

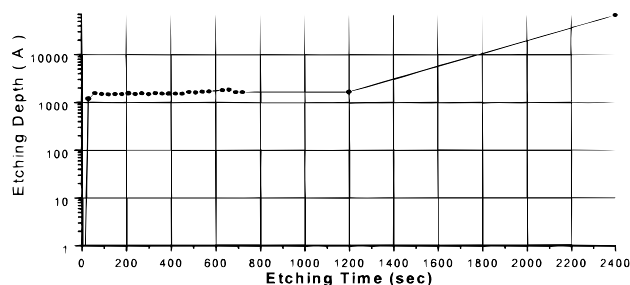

Figure 3. Etch depth *vs.* time for the 1 M $C_6H_8O_7{\cdot}H_2O$:1 M $K_3C_6H_5O_7{\cdot}H_2O{:}H_2O_2 = 5{:}5{:}2$ solution.

The chemical etching of GaAs and AlAs in citric acid/hydrogen peroxide was an oxidation-reduction reaction on the surface of the material to form oxide. The oxide was removed by dissolution. Hydrogen peroxide acted as the oxidizer, and citric acid acted as the dissolving agent. The etching rate of GaAs in citric acid/hydrogen peroxide was fast. When the top GaAs layer was etched through, the AlAs layer was exposed. The etch rate decreased rapidly due to the formation of Al_xO_y. When citric acid/potassium citrate/hydrogen peroxide solution was used, the hydrolysis of tripotassium citrate produced hydroxyls. This assisted the formation of Al_xO_y on the AlAs surface and also hinders the dissolution of the Al_xO_y. The etching rate further decreased and the selectivity of GaAs/AlAs increased dramatically. Figure 4 shows the SEM photograph of the etched profile by 1 M $C_6H_8O_7{\cdot}H_2O$:1 M $K_3C_6H_5O_7{\cdot}H_2O{:}H_2O_2 = 5{:}5{:}2$ solution. The gate direction is along the <110> direction. The etched profile shows a very smooth slope, which prevented high electrical field buildup along the edges and improved the breakdown voltage of the devices. The 1 M $C_6H_8O_7{\cdot}H_2O$:1 M $K_3C_6H_5O_7{\cdot}H_2O{:}H_2O_2 = 5{:}5{:}2$ solution was used in the gate recess process in this study.

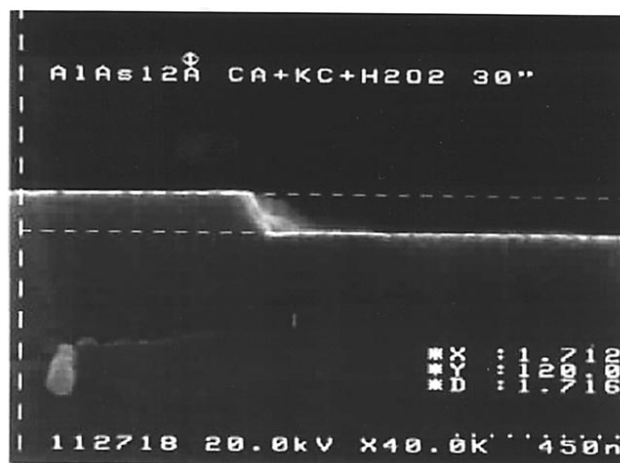

Figure 4. SEM photograph of the etched profile by 1 M $C_6H_8O_7{\cdot}H_2O$:1 M $K_3C_6H_5O_7{\cdot}H_2O{:}H_2O_2 = 5{:}5{:}2$ solution.

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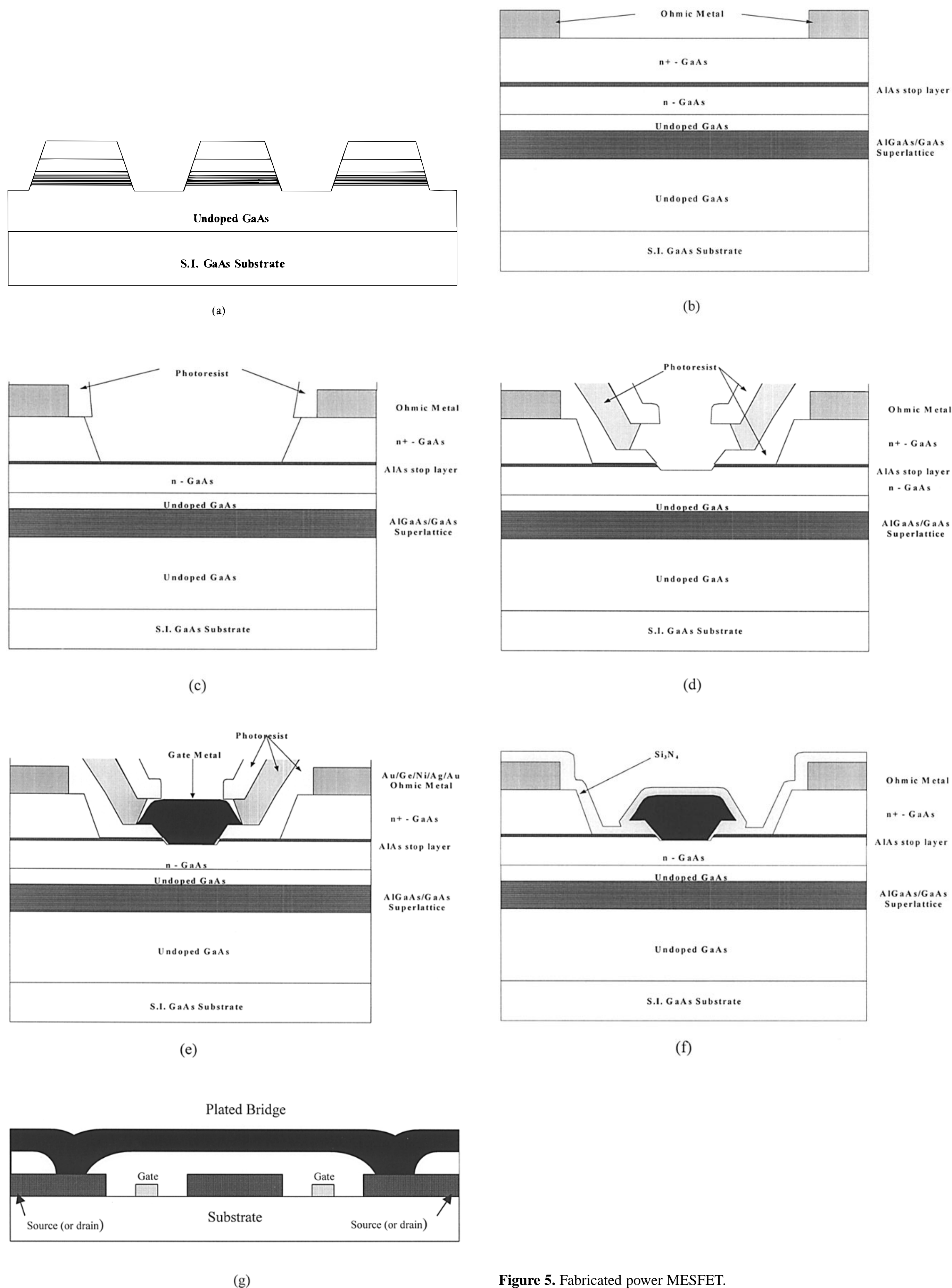

Figure 5. Fabricated power MESFET.

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Device Fabrication

The isolation process of the device was done by mesa etch using the $HF/H_2O_2/H_2O$ solution. The wafers were etched to the undoped GaAs buffer layer to provide good isolation between devices. The ohmic contacts were formed by evaporating Au/Ge/Ni/Au metals on the heavily doped top layer using an E-beam evaporator. The ohmic metal was annealed at 280°C by rapid thermal annealing (RTA).

The selective etch gate recess was performed by two steps. The gate area was first recessed to the AlAs etch-stop layer and then a second shallow recess was performed to etch the gate area to the desired depth to attain the target current. The first recess was etched in the citric acid/potassium citrate/hydrogen peroxide (1 M $C_6H_8O_7 \cdot H_2O$:1 M $K_3C_6H_5O_7 \cdot H_2O$:H_2O_2 = 5:5:2) solution and the second recess was etched in the citric acid/hydrogen peroxide solution. The double gate recess process can remove the surface charges and alleviate the electric field between the gate and the drain.[1,6,13,14] This can lead to the improvement of the gate-to-drain breakdown characteristics. The drain saturation current (I_{dss}) of the devices in the process control monitor (PCM) region was used to monitor the second recess depth.

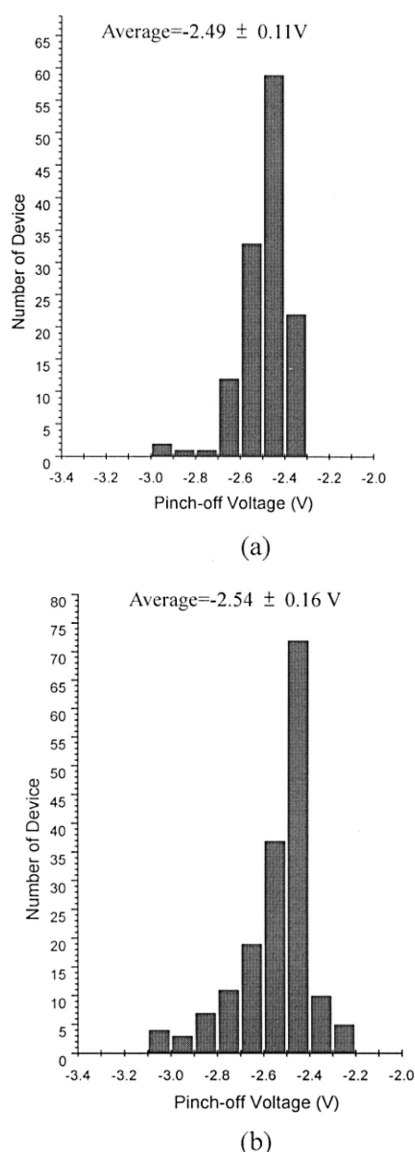

Figure 6. Histograms of the pinch-off voltage for the GaAs power MESFETs using the selective etch process with citric acid/potassium citrate/hydrogen peroxide solution for the gate recess: (a) 14.7 and (b) 19.8 mm.

The gates were formed immediately after the second shallow recess process. The gate metal used was 5000 Å Ti/Pt/Au and was deposited by an electron-beam evaporator. The device passivation was done by 1000 Å plasma-enhanced chemical vapor deposition (PECVD) silicon nitride. Gold-plated air-bridges were used to connect the source fingers. The back side of the wafer was lapped to 4 mils thick and plated with gold for better heat dissipation. The picture of the fabricated power MESFET is shown in Fig. 5.

Device Uniformity

The uniformity of the GaAs power MESFETs with large periphery (14.7 and 19.8 mm) on the 3 in. wafer was investigated. Figure 6 shows the histograms of the pinch-off voltage for the GaAs power MESFETs using the selective etch process with citric acid/potassium citrate/hydrogen peroxide solution for the gate recess. The 14.7 mm devices had a mean pinch-off voltage of -2.49 V with a standard deviation of 0.11 V. For the 19.8 mm devices, the average pinch-off voltage was -2.54 V with a standard deviation of 0.16 V. The large-periphery devices using the selective etch process with citric acid/potassium citrate/hydrogen peroxide solution for the gate recess exhibited good pinch-off voltage uniformity. On the other hand, the 14.7 mm MESFETs using only citric acid/hydrogen peroxide solution for the gate recess had a mean pinch-off voltage of -2.63 V with a standard deviation of 0.26 V. The better uniformity of pinch-off voltage was obtained by citric acid/potassium citrate/ hydrogen peroxide solution compared to citric acid/hydrogen peroxide solution.

Device Performance

Both the dc and rf performance of the devices fabricated using the selective etch process were characterized. Figure 7 shows the typical current–voltage and breakdown characteristics of the 150 μm wide GaAs power MESFETs. In Fig. 7a, the saturation drain current was 34 mA, corresponding to current density of 226 mA/mm. The pinch-off voltage was about -2.5 V when the measurement step of gate voltage was set to 0.5 V. The difference in the pinch-off voltage values between Fig. 7a and Fig. 6 is due to the resolution difference of different measurement instruments. Therefore, the pinch-off voltage values of Fig. 7a and Fig. 6 are in good agreement. In Fig. 7b, the drain-to-gate current as a function of the drain-to-gate voltage is depicted. The gate-to-drain breakdown voltage, defined at a drain current of 1 mA/mm, was 28 V. When the device size was increased to 14.7 mm, the breakdown voltage was changed to 22 V. This value is even better than the breakdown voltage (18 V) of the 150 μm MESFET using only citric acid/hydrogen peroxide solution.

The device was evaluated both at high drain bias (10 V) for high-power applications and at low drain bias (3.3 or 3.5 V) for low-voltage handset applications.

Figure 8 shows the typical power performance of the 14.7 mm wide GaAs power MESFET at high drain bias. The output power (P_{out}), power-added efficiency (PAE), and power gain are illustrated. When operating at the drain bias of 10 V and a quiescent drain current of 500 mA and at 1.88 GHz, the MESFET provided a maximum output power of 38.8 dBm with a power-added efficiency of 49.5% and a gain of 8.42 dB. The linear gain was 12.2 dB and the output power at 1 dB compression point (P_{1dB}) was 37.7 dBm with a PAE of 50.7%. The maximum PAE was 52.5%. The performance shows that the combination of the wet chemical etch process and the etch-stop layer results in an etched profile that can sustain high breakdown voltage for high-power MESFET manufacture.

A large-periphery device was measured at low bias voltage for wireless handset applications. The power performance of the 19.8 mm device at 3.3 V drain bias and 650 mA quiescent drain current is shown in Fig. 9. P_{out}, PAE, and power gain *vs.* input power are illustrated. When biased at 3.3 V and 1.9 GHz, the device had a maximum power of 31.49 dBm and a maximum PAE of 51.4%. The output power at maximum efficiency was 31 dBm. The P_{1dB} was 29.39 dBm and the associated gain was 10.12 dB.

The 19.8 mm device was also tested under IS-95 code-division multiple access (CDMA) modulation at 1.88 GHz and under a drain

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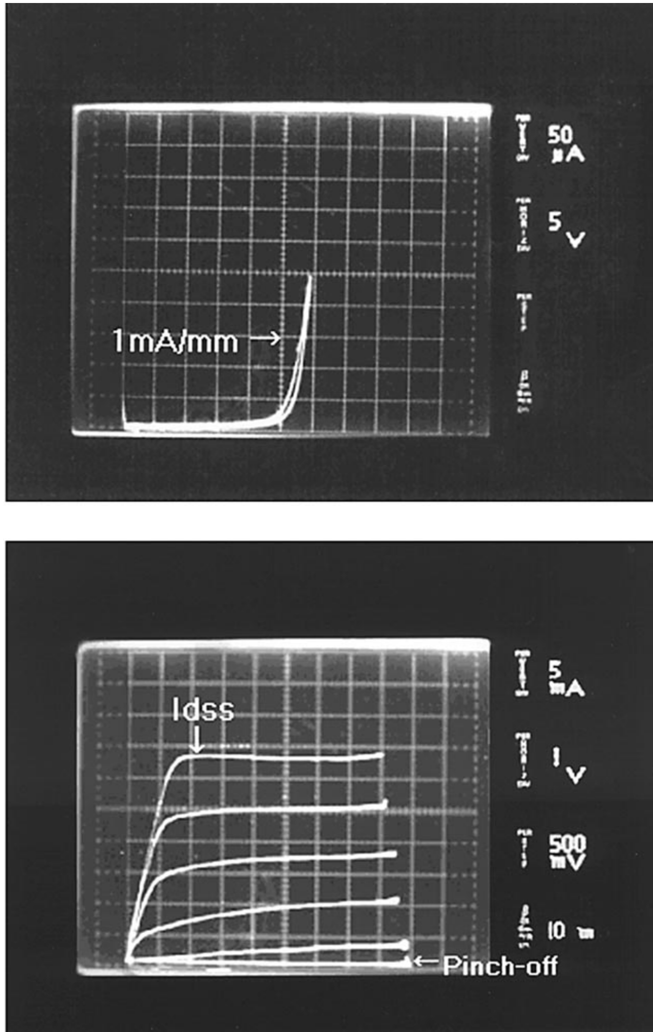

Figure 7. Typical dc characteristics of the 150 μm wide GaAs power MESFETs: (a, top) current-voltage characteristics and (b, bottom) breakdown characteristics.

bias of 3.5 V and a quiescent current of 30 mA. Figure 10 is the CDMA regrowth spectrum. Under such testing conditions, the device showed an output power of 28.03 dBm with an adjacent channel power rejection (ACPR) of −29.6 dBc at 1.25 MHz offset frequency and −42.9 dBc at 2.25 MHz offset frequency. The efficiency at 28.03 dBm output power was 34%. The test data show that these devices using a selective etch process can be used for 3.5 V CDMA handset applications.

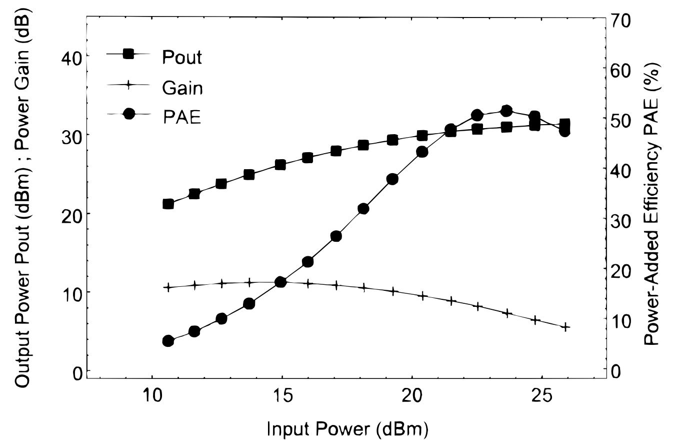

Figure 9. The power performance of the 19.8 mm device at a frequency of 1.9 GHz and under a drain-source bias voltage of 3.3 V and a quiescent drain current of 650 mA.

Conclusion

Power MESFETs using a thin AlAs etch-stop layer and $C_6H_8O_7 \cdot H_2O:K_3C_6H_5O_7 \cdot H_2O:H_2O_2$ based solution for selective gate recess were developed. The selectivity of AlAs/GaAs in this study was higher than 3800. The selective etch process developed in this study can be used both for high-power devices which require high breakdown voltage and for low-voltage power devices which require good pinch-off voltage uniformity and good power efficiency as well as linearity. The power devices developed using this process have good power performance, including high output power density, high power efficiency, and good power linearity. The devices developed also have good pinch-off uniformity across 3 in. wafers. No surface-state effect was observed in the devices processed. The selective etch process developed simplifies the steps for gate recess and provides good device uniformity. The power MES-

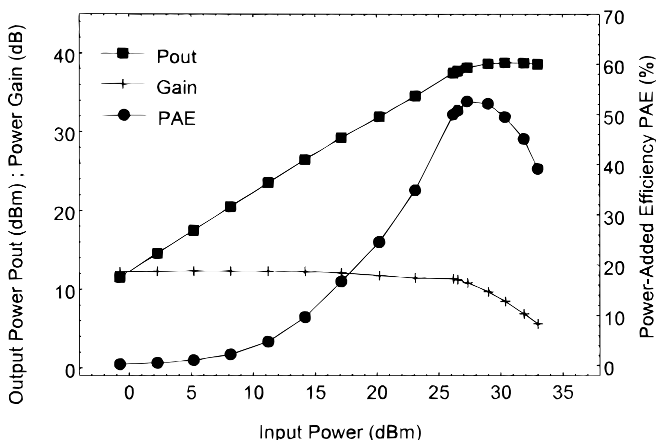

Figure 8. Typical power performance of the 14.7 mm wide GaAs power MESFET at a frequency of 1.88 GHz and under a drain-source bias of 10 V and a quiescent drain current of 500 mA.

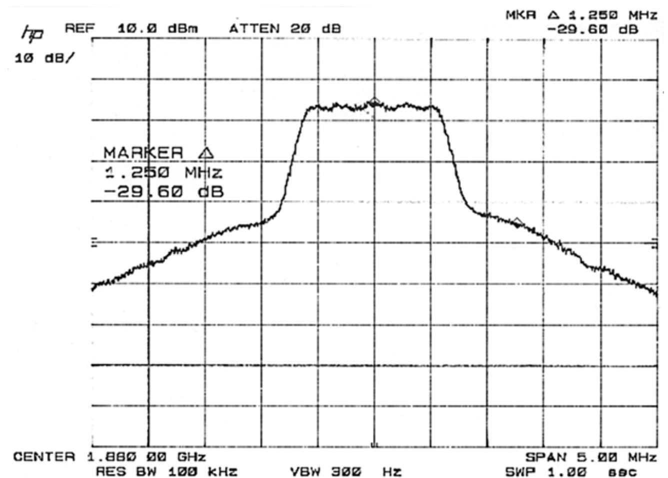

Figure 10. The CDMA spectrum of the 19.8 mm power MESFET under a drain bias voltage of 3.5 V and a quiescent drain current of 30 mA. The center frequency is 1.88 GHz.

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FETs using this gate recess technique are applicable to digital wireless communications including CDMA applications.

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