Analytical design formulation for minority-carrier well-type guard rings in CMOS circuits

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Indexing terms: CMOS circuits, Guard rings, Dual collector structures

Abstract: Minority carriers injected from an active emitter into the substrate and partially collected by the bottom well junction in an epitaxial CMOS structure are studied. Two-dimensional numerical simulation has revealed that the minority-carrier collection current along the bottom well junction is contributed primarily by two mechanisms: the first due to minority carriers injected into a layer between the upper collecting plate and the bottom reflecting plate; and the second due to those penetrating the high/low junction and then spreading out in the large, highly-doped bulk as in the nonepitaxial case. Based on this observation, a new analytic model for the minority-carrier escape current has been developed as a measure of well-type guard ring efficiency. This model, including a closed-form expression as function of epitaxial layer thickness, well junction depth and guard ring width, has been confirmed by experimental data as well as by two-dimensional numerical simulation. As predicted by the model, the measured escape current has been found to be dominated by the second mechanism for the case of well junction depth close to epitaxial layer thickness while the first mechanism has been identified to dominate the escape current measured from the structure having sufficient epitaxial layer thicknesses.

1 Introduction

Minority-carrier well-type guard rings in CMOS circuits have been widely used as a special layout guideline for separating potential minority-carrier injectors in the substrate from the internal circuitry, making an attempt to avoid latchup and charge upset of the internal circuitry. The efficiency of such a guard ring can be greatly enhanced by using epitaxial CMOS [1]. Troutman [1] attributed this to the reflection property of the high/low junction. However, such interpretation is not sufficient to understand the significant mechanisms dominating the guard ring efficiency and should be greatly improved. Moreover, the effectiveness of the well-type guard ring can be determined quantitatively as long as the corresponding minority-carrier collection current distributed along the bottom well junction is known [2]. Recently, a study of well-type guard ring efficiency by solving the 2D carrier diffusion equation has been reported [3]. However, no design formulation for minority-carrier well-type guard ring efficiency, taking into account the effect of both epitaxial-layer thickness and guard ring width, has been published. In this work, we report such a design model and its verification by 2D numerical simulation as well as by experimental data.

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2 Model development

Fig. 1 schematically shows the cross-section of an n-well guard ring separating the n^+ emitter from the internal circuitry.

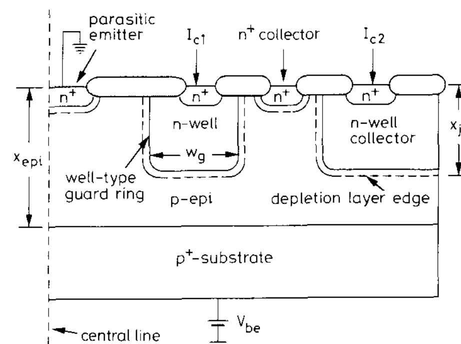

Fig. 1 *Schematic cross-section of n-well guard ring structure on p-epi/p^+-substrate*

The internal circuitry can be typically represented by an n^+ collector and an outer n-well collector as shown in Fig. 1. Two-dimensional numerical simulator Summos II [4], which solves simultaneously the Poisson equation and the current continuity equations for both electrons and holes, has been used for analysing this structure in the worst case, i.e. the guard ring attaching a nearby n-well of the internal circuitry. The emitter junction depth is 0.35 μm, the well junction depth is 3 μm, the

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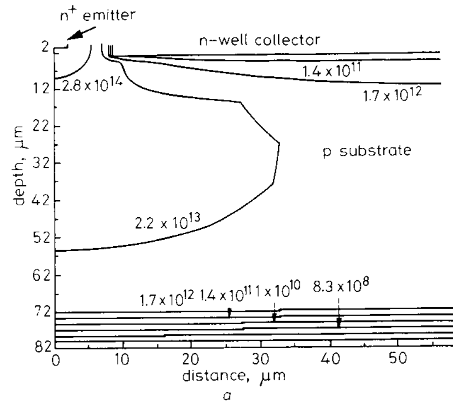
emitter width is 2 μm, and the emiter to inner collector spacing is 8 μm. The epitaxial layer thickness (x_{epi}) ranges from 3 to 40 μm. The doping concentrations in n^+ emitter, n-well, p-type epitaxial layer, and p^+ substrate are 10^{20}, 10^{17}, 10^{15}, and 10^{18} cm^{-3}, respectively. The physical mechanisms such as Auger recombination, Shockley–Read–Hall recombination and the bandgap narrowing effect have been taken into account.

The simulated 2D minority-carrier (i.e. electron) density contours for both epitaxial and nonepitaxial cases are shown in Fig. 2. From Fig. 2*a* it is clearly observed that minority carriers injected from the emitter not only flow laterally to the well sidewall but also flow vertically down and then spread out in the large bulk. Note that such spreading feature contributes to minority carriers collected by the bottom well junction. For the epitaxial case of $x_{epi} = 11$ μm, Fig. 2*b* shows clearly that in addition to the lateral component flowing to the well sidewall, the injected minority carriers which are reflected by the high/low junction, flow into a layer between the upper well junction and the bottom high/low junction. At the same time, the minority carriers, which penetrate the high/low junction and then spread out in the large, highly-doped bulk, can contribute to those collected by the bottom well junction.



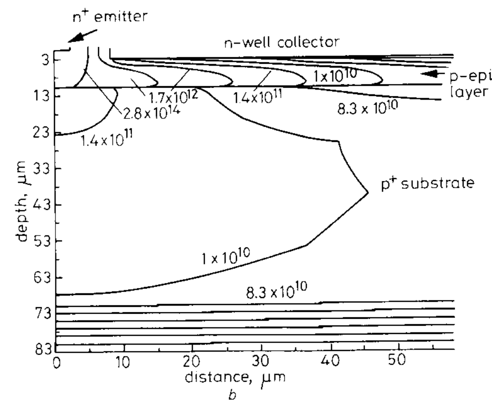


Fig. 2 *Simulated 2D electron density distributions*
a nonepitaxial case
b $x_{epi} = 11$ μm

One of the major features described, i.e. the first current component due to minority carriers injected into a layer between the upper collecting plate and the bottom reflecting plate, is represented by the 2D boundary value problem as given in Fig. 3. The upper collecting plate at $x = x_{jd}$ is indeed the edge of the depletion region across the bottom reverse-biased well–substrate junction and thus the excess electron concentration $n(x, y) = 0$ at $x = x_{jd}$. Further, we idealise the capability of the high/low junction to reflect minority carriers by making $dn/dx = 0$ at $x = x_{epi}$. Irrespective of such a simplified boundary condition, the resulting model has been positively judged. The corresponding 2D minority-carrier diffusion equation in the neutral region of $x_{jd} \leqslant x \leqslant x_{epi}$ and $y_2 \leqslant y$ in Fig. 3 is given by $\nabla^2 n(x, y) - n(x, y)/L_n^2 = 0$ where $n(x, y)$ is the injected excess minority-carrier density and L_n is the minority-carrier diffusion length. Using the method of separation of variables, the corresponding solution with boundary conditions satisfied can be written as

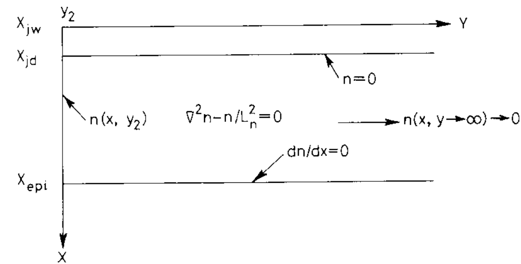


Fig. 3 *Proposed boundary value problem for analytically finding first component of escape current*
y_2 is location of guard ring edge facing n^+ emitter
x_{jw} is well junction depth

$$n(x, y) = \sum_{m=1}^{\infty} A_m \cos\left[\frac{(2m-1)\pi(x_{epi} - x)}{2(x_{epi} - x_{jd})}\right] \times \exp\left[-\sqrt{\left\{\frac{1}{L_n^2} + \left[\frac{(2m-1)\pi}{2(x_{epi} - x_{jd})}\right]^2\right\}}(y - y_2)\right] \quad (1)$$

where

$$A_m = \frac{2}{(x_{epi} - x_{jd})} \int_{x_{jd}}^{x_{epi}} n(x, y_2) \times \cos\left[\frac{(2m-1)\pi(x_{epi} - x)}{2(x_{epi} - x_{jd})}\right] dx$$

Assuming $n(x, y_2)$ to be a constant (n^*) for $x_{jd} \leqslant x \leqslant x_{epi}$, then $A_m = (2n^*/((2m-1)\pi)) \sin((2m-1)\pi/2)$. For relatively large y, i.e. $(y - y_2) \geqslant (1/L_n^2 + (\pi/2(x_{epi} - x_{jd}))^2)^{1/2}$, and for $L_n \gg x_{epi}$ which is usually encountered, the injected minority-carrier density $n(x, y)$ in eqn. 1 rapidly approaches its asymptotic form given by the first term

$$n(x, y) \rightarrow \frac{2n^*}{\pi} \cos\left[\frac{\pi(x_{epi} - x)}{2(x_{epi} - x_{jd})}\right] \exp\left[-\frac{\pi(y - y_2)}{2(x_{epi} - x_{jd})}\right] \quad (2)$$

where the coefficient n^* in cm^{-3} is used as a fitting parameter in this work. The position-dependent minority-carrier escape current $I_1(y)$ [2] can be obtained by integrating the minority-carrier current density $J_1(y)$ ($\equiv qD_n\, dn/dx$) at $x = x_{jd}$ from $y > y_2$ to infinite, resulting

in the following expression:

$$I_1(y) = I_{eff1} \exp\left(-\frac{y - y_2}{L_{eff1}}\right) \quad \text{for } y > y_2 \tag{3}$$

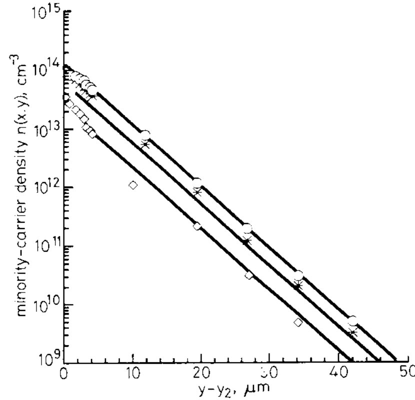


Fig. 4 *2D electron distributions below well junction calculated using both Summos 2 and model (x_{epi} = 11 μm)*

◇ 5.8 μm above high/low junction } 2D full analysis
✱ 4 μm above high/low junction
○ high/low junction
——— eqn. 2 with $n^* = 1.45 \times 10^{14}$ cm^{-3}

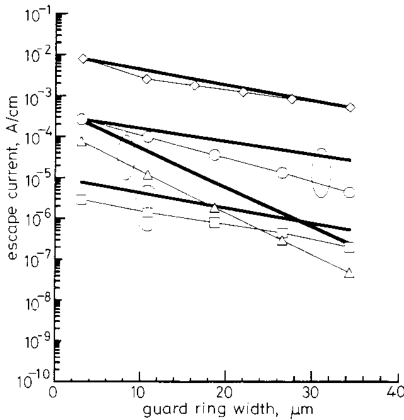


Fig. 5 *Escape currents calculated using both summos 2 and model for x_{epi} = 5, 11 and 18 μm as well as for nonepitaxial case*

◇ nonepitaxial V_{be} = 0.7 V } 2D full analysis
□ x_{epi} = 5 μm V_{be} = 0.7 V
○ x_{epi} = 18 μm V_{be} = 0.6 V
△ x_{epi} = 11 μm V_{be} = 0.6 V
——— model

where $I_{eff1} = 2qD_n n^* W_{eff}/\pi$ and $L_{eff1} = 2(x_{epi} - x_{jd})/\pi$. The parameter W_{eff} in eqn. 3 represents the effective peripheral length and thus the escape current $I_1(y)$ has the unit of A.

For the nonepitaxial case we adopt the empirical expression [3] $I_{escape}(y) = I_{eff2} \exp(-(y - y_2)/33\ \mu\text{m})$. The validity has been verified by a variety of experimental data in terms of the induced potential drop in the well due to the action of an emitter in the substrate, as well as in terms of the steady-state collector current of an active parasitic lateral bipolar transistor for triggering the latchup [5]. Fortunately, we have found that eqn. 3 can be reasonably applied in the nonepitaxial case as long as $L_{eff1} = 33$ μm since the corresponding calculated values have offered sufficient accuracy when compared with the 2D full simulation results. As a result, $I_{eff2} \approx I_{eff1}$, which will be judged later.

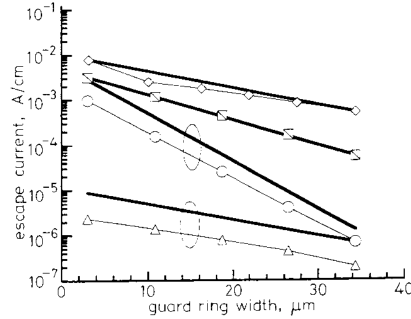


Fig. 6 *Comparisons of escape currents calculated using both Summos 2 and 2D simplified analysis [3]*

◇ nonepitaxial } 2D full analysis
⧅ x_{epi} = 18 μm
○ x_{epi} = 11 μm
△ x_{epi} = 5 μm
——— Reference 3

For the epitaxial case, therefore, the escape current component due to minority carriers penetrating the high/low junction and then spreading out in the large, heavily-doped bulk as in the nonepitaxial case, can be, for the first-order approximation, modelled by $I_2(y) = \eta_1 I_{eff1} \exp(-(y - y_2)/33\ \mu\text{m})$, where $\eta_1 = N_{AL} \exp(\Delta E_g/kT)/N_{AH}$ [3]. N_{AL} and N_{AH} are the doping concentrations of low-doped epitaxial layer and highly doped substrate, respectively; and ΔE_g is the effective bandgap shrinkage in the heavily doped substrate. The parameter η_1 represents the capability of minority-carriers penetrating high/low junction [3]. The total position-dependent escape current contributed by two components can be written as $I_{escape}(y) = I_1(y) + I_2(y)$. Note that $I_1(y) > I_2(y)$ for small guard ring width, while a critical guard ring width $W_g(\equiv y - y_2)$ appears from which $I_2(y) > I_1(y)$. Such critical W_g can be obtained by making $I_1(y) = I_2(y)$, yielding W_g (critical) $= \ln(\eta_1)/(1/33\ \mu\text{m} - 1/L_{eff1})$.

3 Model identification 1

The simulated 2D minority-carrier density distributions in the epitaxial layer below the well junction for x_{epi} = 11 μm are shown in Fig. 4, where the corresponding results using eqn. 2 with $n^* = 1.45 \times 10^{14}$ cm^{-3} are also shown for comparison. From Fig. 4 it can be observed that the results based on eqn. 2 for $y - y_2 > 2$ μm are in good agreement with the 2D numerical simulation. The deviation is evident for small values of y. This discrepancy can be improved by considering the remaining terms. The corresponding escape currents calculated by eqn. 3 are shown in Fig. 5 where the 2D numerical simulation results are depicted for comparison. From Fig. 5 it can be observed that an excellent agreement between the two has been obtained. This is also the case for x_{epi} = 18 μm, as shown in Fig. 5. Moreover, Fig. 5 shows that

the 2D full simulation results have confirmed reasonably not only the calculated escape current using $I_{escape}(y) = I_{eff1} \exp(-(y - y_2)/33\ \mu m)$ for the nonepitaxial case, but also $I_{escape}(y) = I_2(y)(I_2(y) \gg I_1(y))$ using $I_2(y) = \eta_1 I_{eff1} \exp(-(y - y_2)/33\ \mu m)$, where $\eta_1 \approx 10^{-3}$ for $x_{epi} = 5\ \mu m$.

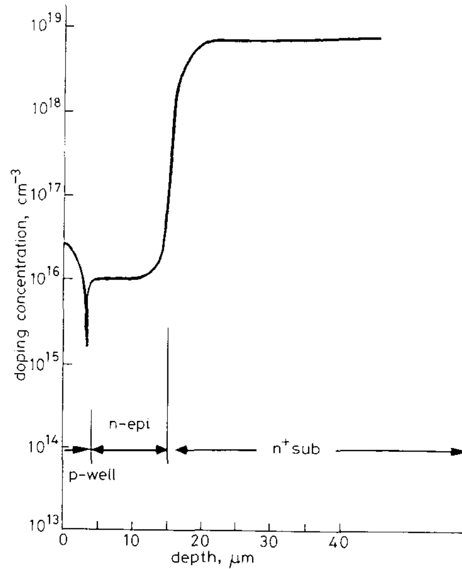


Fig. 7 *Measured doping profile for one p-well epitaxial CMOS case*

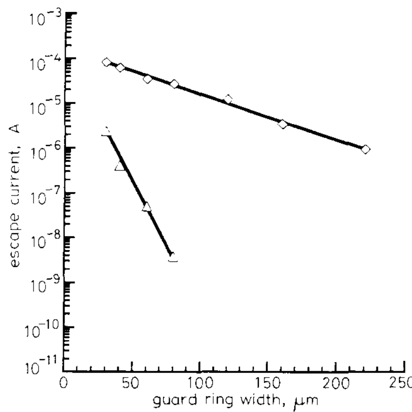


Fig. 8 *Escape current as function of guard ring width measured from nonepitaxial wafer as well as from epitaxial wafer corresponding to Fig. 7 with calculated escape currents based on model shown for comparison*

Value of 7.63 μm obtained from $L_{eff1} = 2(x_{epi} - x_{jd})/\pi$ where $x_{epi} = 16\ \mu m$ and $x_{jd} = 4\ \mu m$

◇ nonepitaxial $I_{escape}(W_g) = 1.6 \times 10^{-4} \exp(-W_g/33\ \mu m)$ A

△ $x_{epi} = 16\ \mu m$ $I_{escape}(W_g) = 1.2 \times 10^{-4} \exp(-W_g/7.63\ \mu m)$ A

— · —— model

By solving only a 2D carrier diffusion equation the work cited in Reference 3 has yielded the results shown in Fig. 6 for comparison with both Summos II and the model. Without any parameter adjustment, close agreement has been obtained, as depicted in Fig. 6. This is to be expected since such simplified analysis simultaneously holds the features of the minority carriers injected into a neutral layer between the upper collecting plate and the bottom reflecting plate, and the minority carriers penetrating the high/low junction and then spreading out in the large bulk. This strongly supports the model in this respect.

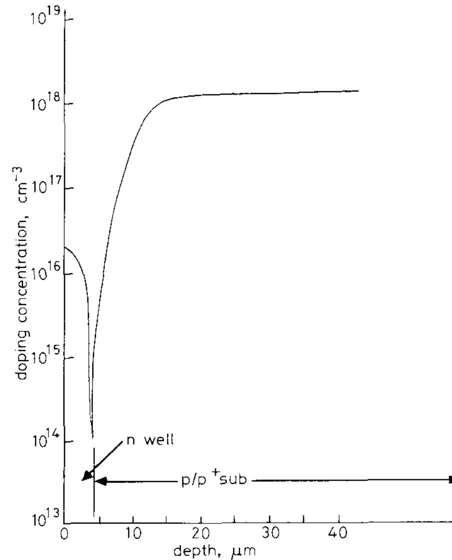


Fig. 9 *Measured doping profile for one n-well epitaxial CMOS case*

4 Model identification 2

The specially designed dual collector structures have been fabricated by using both n-well and p-well CMOS processes with both well-type guard ring width and epitaxial layer thickness as parameters. The fabricated structures identical to Fig. 1 are similar to that reported by Troutman [1]. In our work, however, all of these structures have the identical layout dimensions except the inner well-type guard ring width (W_g) taken as a design parameter. This procedure allows the appropriate determination of the minority-carrier escape current via the outer collector current I_{c2}, as labelled in Fig. 1.

Fig. 7 shows the measured doping profile for the p-well epi CMOS case, where a nearly abrupt high/low junction is clearly observed. From Fig. 7, a layer with sufficient thickness exists between the upper collecting plate and the bottom reflecting plate. The same structures have also been fabricated on the single nonepitaxial wafer. Fig. 8 shows the measured escape currents I_{c2} against the guard-ring width W_g for the epitaxial and nonepitaxial cases.

In Fig. 8, the escape current I_{c2} measured from the epitaxial case decreases rapidly as W_g increases while for the nonepitaxial case the decrease in I_{c2} is much slower. Also note that the corresponding calculated values as shown in Fig. 5 deliver the same behaviour as the experimental results. Moreover, the rapid decrease in I_{c2} as W_g increases can be explained by the dominant limiting mechanism of the minority carriers injected into a layer between the upper collecting plate and the bottom reflecting plate. Fig. 8 also shows that the measured I_{c2} against W_g data for the expitaxial and nonepitaxial cases can be fitted well using eqn. 3 and $I_{eff2} \exp(-W_g/33\ \mu m)$,

respectively. In this case, the value of I_{eff1} is reasonably close to I_{eff2}.

Fig. 9 shows the measured doping profile for the n-well epitaxial CMOS case, where a graded doping profile from p^+ substrate dominates over the original low-doped epitaxial layer under the well. From Fig. 9 the well junction depth is nearly identical to the epitaxial layer thickness. This is caused by the out-diffusion from the heavily-doped substrate. The corresponding measured data of the escape current against guard ring width are shown in Fig. 10 where the nonepitaxial case is also shown for comparison. From Fig. 10 the measured escape current I_{c2} decreases very slowly as W_g increases. The corresponding calculated results, as illustrated in Figs. 5 and 6 for both $x_{epi} = 5\ \mu m$ and the nonepitaxial case, predict the same behaviour as the experimental data. The slow decrease in I_{c2} as W_g increases can be attributed to the dominant limiting mechanism of the minority carriers spreading out in the large bulk. Fig. 10 also shows that the experimental data can be fitted well by the model.

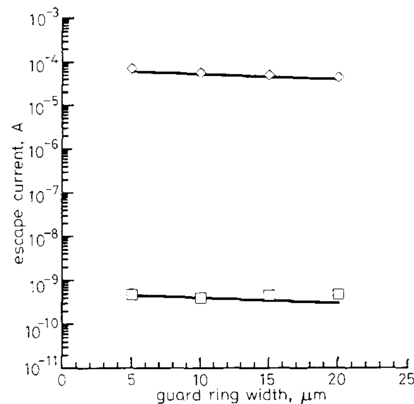


Fig. 10 *Escape current as function of guard ring width measured from nonepitaxial wafer as well as from epitaxial wafer corresponding to Fig. 9 with calculated escape currents based on model shown for comparison*

◇ nonepitaxial case $I_{escape}(W_g) = 6.847 \times 10^{-5} \exp(-W_g/33\ \mu m)$ A

□ epitaxial case $I_{escape}(W_g) = 5.479 \times 10^{-10} \exp(-W_g/33\ \mu m)$ A

——— model

5 Conclusion

A new analytical model for estimating the escape current has been developed for the design of minority-carrier well-type guard rings in CMOS circuits. The two mechanisms responsible for escape current have been found numerically and have been located experimentally. The calculated results based on the model have been confirmed by 2D numerical simulation and experimental data measured from a variety of specially designed dual collector structures.

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