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Improvement on performance and reliability of TaN/HfO_2 LTPS-TFTs with fluorine implantation

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Abstract

In this paper, we demonstrate the low-temperature polycrystalline silicon thin-film transistors (LTPS-TFTs) with TaN metal-gate and HfO_2 gate dielectric to achieve high performance characteristics. A high performance LTPS-TFT with low threshold voltage 0.9 V, excellent subthreshold swing 0.15 V/decade and high I_{on}/I_{min} current ratio 1.9×10^6 are derived without any hydrogen treatment. In addition, we also introduce the fluorine implantation prior to the Si thin-film crystallization to passivate the defects in grain-boundaries of the channel film and HfO_2/polysilicon interface. Significant improvements on subthreshold swing and I_{min} are observed. In addition, the transconductance degradation and threshold voltage instability due to hot carrier stress is also investigated, respectively. Finally, we derive a high reliability and performance LTPS-TFT with low threshold voltage ~1.38 V, ultra-low subthreshold swing 0.132 V/decade and high I_{on}/I_{min} current ratio 1.21×10^7, which is suitable for the application of system-on panel (SOP).
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Keywords: LTPS-TFTs; Metal-gate; High-κ; Fluorine implantation

1. Introduction

High performance low-temperature polycrystalline-silicon thin-film transistors (LTPS-TFTs) have been attracted much attention in many applications in recent years, especially for the integrated circuit of the active matrix liquid phase-crystal displays (AMLCD) [1,2] and the most important elements for SRAM's [3]. This is because the field effect mobility μ_{EF} in polycrystalline-silicon is significantly higher (by two orders of magnitude) than that in amorphous silicon [4]. However, there are many defects at the grain-boundary of polycrystalline silicon thin-film, resulting in the degradation of LTPS-TFTs' performance [5]. In order to fill the traps with enough charges to make the channel more conductive, a large operation voltage was needed for the conventional LTPS-TFTs without any defects passivation [6–8]. These defects would result in very poor subthreshold swing and large threshold voltage.

The increase of gate capacitance is one effective way to improve the performance of LTPS-TFTs. A large gate capacitance can attract more carriers with a smaller voltage to make the LTPS-TFTs turn on. However, a higher gate leakage current would be introduced when the thickness of gate oxide becomes thinner to make large gate capacitance. In order to overcome this drawback, many high-κ dielectrics have been used to reduce the gate leakage current and to increase the transconductance [9–14]. Among these dielectric materials, HfO_2 is the most promising candidate of future high-κ gate dielectric material due to its high permittivity (~20) and thermal stability with poly-Si [12–14].

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In spite of using the high-κ gate dielectrics, the defects of channel film still exist that affect the leakage current [5]. Therefore, defects passivation is necessary to improve leakage current and I_{on}/I_{min} current ratio. Hydrogen plasma is the most popular species employed to passivate defects and reduce the leakage current [15–17]. However, the introduction of hydrogen passivation method would degrade the reliability due to the weak Si–H bond [18,19]. In this paper, we replace the weak Si–H bond with the strong Si–F bond by using the fluorine implantation method [20–22] instead of hydrogen passivation. Finally, the metal-gate/high-κ LTPS-TFTs with fluorine implantation is demonstrated for the first time.

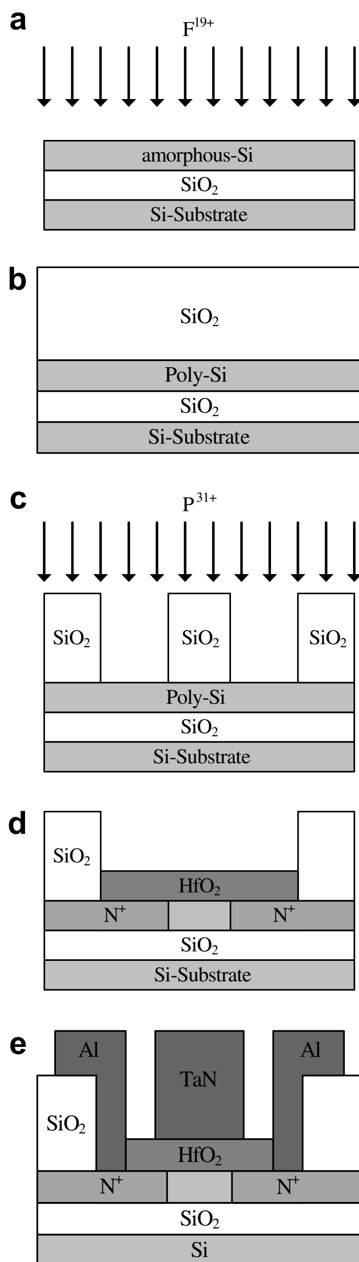

Fig. 1. Process flow of high-κ HfO_2 gate dielectric and TaN gate LTSP-TFT structure with fluorine implantation.

2. Experimental procedure

The fabrication of devices started by depositing a 50 nm undoped amorphous Si (α-Si) layer at 550 °C in a low-pressure chemical vapor deposition (LPCVD) system on Si wafers capped with a 500 nm thick thermal oxide layer. Then, the fluorine atoms were implanted with 11 keV implant energy and dose $5 \times 10^{14}\,cm^{-2}$ as shown in Fig. 1a. After the fluorine implantation, the α-Si layer was re-crystallized by solid-phase-crystallization (SPC) process by furnace at 600 °C for 24 h in a N_2 ambient. Then 500 nm thick plasma-enhanced chemical vapor deposition (PECVD) oxide was deposited at 300 °C for device isolation as shown in Fig. 1b. The device active region was formed by patterning and etching the isolation oxide. The source and drain regions in the active device region was implanted with phosphorus (20 keV at $5 \times 10^{15}\,cm^{-2}$) and activated at 600 °C for 24 h annealing in a N_2 ambient as shown as Fig. 1c. After the active region was patterning, a 75 nm HfO_2 was deposited by electron-beam evaporation system as shown in Fig. 1d. An O_2 treatment in furnace was applied to improve the gate oxide quality at 400 °C for 30 min. Then, the gate electrode was patterning by reactive ion etching after TaN deposition. After the patterning of contact holes, the TFT devices were completed by probe pads formation etching after aluminum deposition by thermal evaporation system as shown in Fig. 1e. The measurement of device has gate length and width of 10 and 100 μm, respectively. The threshold voltage is defined as the gate voltage at which the drain-current reaches 100 nA × W/L and $V_{DS} = 0.1$ V. Field effect mobility μ_{FE} is extracted from the maximum transconductance (G_m).

3. Results and discussion

The transfer characteristics I_{DS}–V_{GS} of the TaN/HfO_2 gate stack structure LTPS-TFTs with and without fluorine implantation were shown in Fig. 2. It indicates a significant

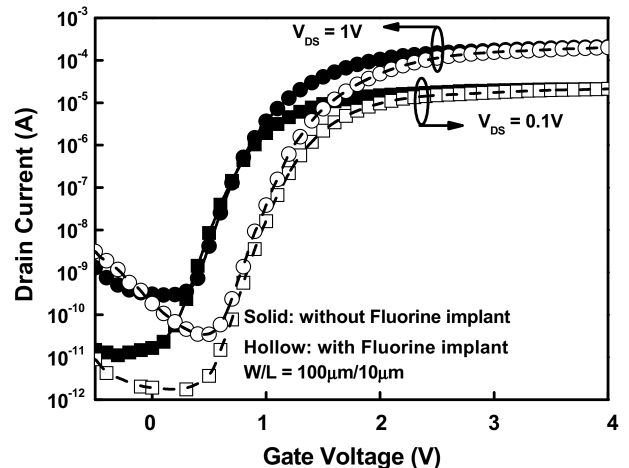

Fig. 2. The transfer characteristics $I_{DS} - V_{GS}$ of the TaN/HfO_2 gate stack structure LTPS-TFTs with and without fluorine implantation.

I_{min}-current reduction from 11.1 to 1.71 pA, subthreshold swing improvement from 0.150 to 0.132 V/decade, and a positive 0.48 V threshold voltage shift after the fluorine ion implantation. The I_{min} current and subthreshold swing are related to grain defects and interface density of states [5]. By neglecting the depletion capacitance in the channel layer, the effective interface-trap-state density (D_{it}) near the HfO_2/poly-Si interface can be evaluated from the subthreshold swing (S.S.) as equation [23]

$$D_{it} = \left[\left(\frac{\text{S.S.}}{\ln 10}\right)\left(\frac{q}{KT}\right) - 1\right]\left(\frac{C_{ox}}{q}\right). \quad (1)$$

The effective interface-trap-state density (D_{it}) was improved from $1.7 \times 10^{12}\,\text{cm}^{-2}$ to $1.37 \times 10^{12}\,\text{cm}^{-2}$. It indicates a 19.41% reduction of D_{it} due to the fluorine passivation. In addition, a positive 0.48 V threshold voltage indicates that fluorine would introduce negative fixed oxide charges in HfO_2, and the result of the introduction of negative fixed charge by fluorine is consistence with the work by Maegawa et al. [24]. Fig. 3 shows the transconductance G_m of the TaN/HfO_2 gate stack structure LTPS-TFTs with and without fluorine implantation. A slightly improvement of transconductance G_m is observed. It is due to the passivation of the effective interface-trap-state density (D_{it}) after the fluorine ion implantation. In addition, the ion implantation would also result in some amorphization of the channel film, and the channel film may have the chance to form larger grains after re-crystallizing annealing. However, the grain size effect due to the fluorine ion implantation would not be significant under a thin channel film and low implantation energy. Yang et al. [25] have demonstrated that the grain size effect would not be obvious if the channel film was thin enough and fluorine ion implantation energy was low, even with 60-nm channel thin-film, which is thicker than our case, and higher ion implantation energy (15 keV) [25]. This unobvious grain size effect is also consistence with the result of Tu et al. [6].

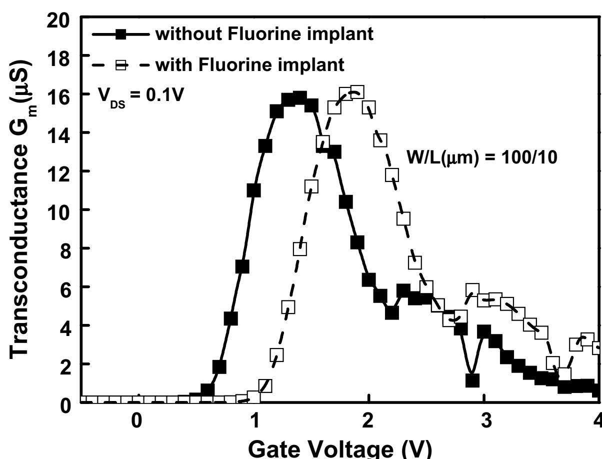

Fig. 3. The transconductance G_m of the TaN/HfO_2 gate stack structure LTPS-TFTs with and without fluorine implantation.

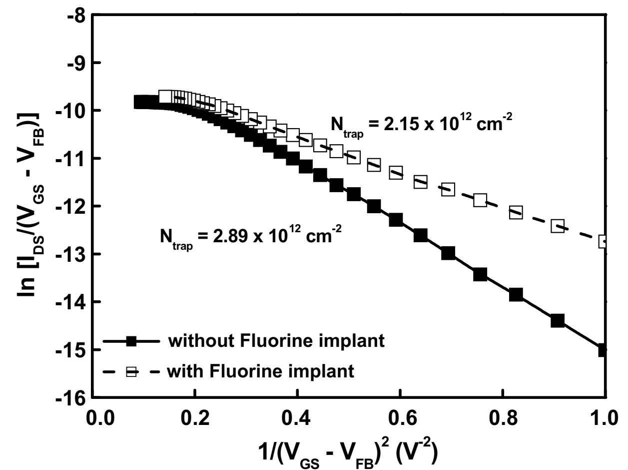

Fig. 4. The plots of ln $[I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ curves at $V_{DS} = 1$ V and high V_{GS}.

The grain-boundary trap-state densities (N_{trap}) with and without fluorine implantation were also estimated by Levinson and Proano method [26,27]. Fig. 4 exhibits the plots of $\ln[I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ curves at $V_{DS} = 1$ V and high V_{GS}, where the flat-band voltage (V_{FB}) is defined as the gate voltage that yields the minimum drain-current from the transfer characteristic. The grain-boundary trap-state densities (N_{trap}) can be determined from the square root of the slope

$$N_{trap} = \frac{C_{ox}}{q}\sqrt{|\text{Slope}|}. \quad (2)$$

From Fig. 4, it is apparent that the grain-boundary trap-state densities decrease from $2.89 \times 10^{12}\,\text{cm}^{-2}$ to $2.15 \times 10^{12}\,\text{cm}^{-2}$ after fluorine passivation. It indicates an improvement about 25.6% on the grain-boundary trap-state densities. The important parameters of LTPS-TFTs are listed in Table 1. A significant performance improvement was observed by the fluorine ion implantation to achieve low threshold voltage ~1.38 V, excellent subthreshold swing ~0.132 V/decade, and high I_{on}/I_{min} current ratio $\sim 1.21 \times 10^7$. These improvement results can be attributed to the traps passivation of D_{it} and N_{it} for 19.41% and 25.6% improvement, respectively.

The reliability of LTPS-TFTs is also another important issue. Because the operation voltage of LTPS-TFTs with TaN/HfO_2 gate stack structure was within 3 V, we employee the hot carrier stress with $V_{GS} - V_{TH} = V_{DS} = 5$ V for 1000 s instead of $V_{GS} = V_{DS} = 5$ V because that different hot carrier stability is observed under different V_{GS} and constant V_{DS} [28]. The threshold voltage stability ($\Delta V_{TH} = V_{THf} - V_{THi}$) was improved from 1.6 V to 1.22 V of the threshold voltage shift after 1000 s hot carrier stress as shown in Fig. 5. Positive voltage shifts of threshold voltage indicate that the electrons were trapped by the gate dielectric HfO_2 under hot carrier stress. The fluorine implanted device shows a smaller threshold voltage shift indicates that fewer electrons were trapped in HfO_2

Table 1
Device parameters of TaN/HfO_2 gate stack TFTs with and without Fluorine implantation

	V_{TH} (V)	Swing (V/decade)	G_m (μS)	I_{min} (pA)	I_{on} (μA)	I_{on}/I_{min} (10^6)	D_{it} (10^{12} cm^{-2})	N_{trap} (10^{12} cm^{-2})
Control	0.9	0.15	15.9	11.1	21.1	1.9	1.7	2.89
F-implant	1.38	0.132	16.1	1.74	21.1	12.1	1.37	2.15

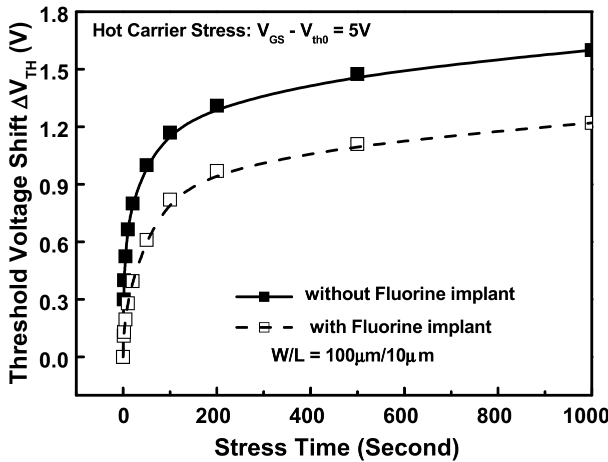

Fig. 5. The threshold voltage shift ΔV_T of TaN/HfO_2 LTPS-TFTs with and without fluorine implantation after 1000-s hot carrier stress.

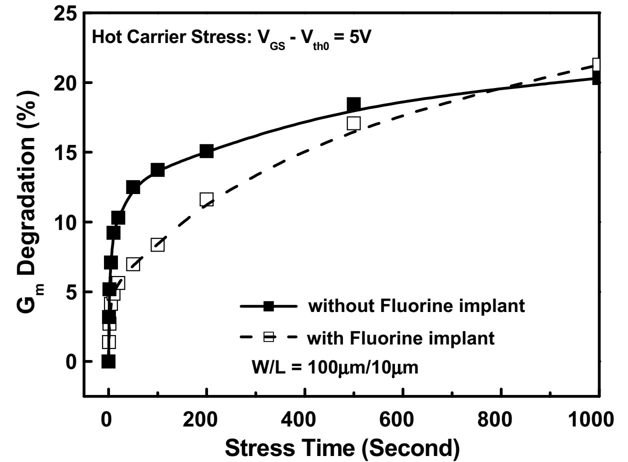

Fig. 7. The transconductance G_m degradation of TaN/HfO_2 LTPS-TFTs with and without fluorine implantation during 1000 s hot carrier stress.

after fluorine passivation. Fig. 6 shows the gate leakage current of LTPS-TFT with and without fluorine ion implantation. A smaller reduction rate of gate leakage current of the fluorine-implanted device under hot carrier stress was observed, which shows a smaller electron trapping rate than the device without fluorine ion implantation.

Fig. 7 shows the transconductance G_m degradation of the LTPS-TFT with and without fluorine ion implantation. For the device without fluorine ion implantation, a suddenly high degradation rate of transconductance G_m was happened within 50 s of hot carrier stress, and then a saturation behavior was observed. For the fluorine-

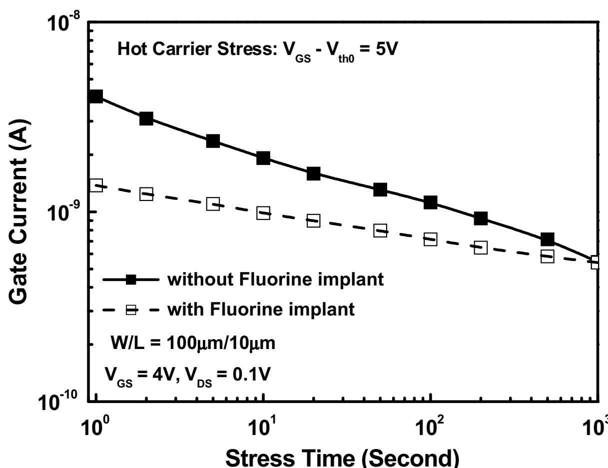

Fig. 6. The gate leakage current of TaN/HfO_2 LTPS-TFTs with and without fluorine implantation during the hot carrier stress.

implanted device, the suddenly high degradation rate region of transconductance G_m was within 20 s. In addition, the degradation of transconductance G_m after 1000 s of hot carrier stress was more serious for the LTPS-TFT with fluorine ion implantation. In the short stress time regime, the degradation of G_m for the fluorine-implanted device is smaller than that of the device without fluorine implantation. Because the grain-boundaries and the high-κ/poly-Si interface of the fluorine-implanted device were passivated by the strong Si–F bonds, the device was less degraded as the stress was initially performed. As stress time increases, the fluorine-implanted device shows a larger degradation rate in G_m than the one without fluorine implantation. We attributed the severe degradation of the fluorine-implanted device to the more strict stress current, and this can be further explained from Fig. 8, which shows the time dependence of the driving current under hot carrier stress.

It is worth noting that the fluorine-implanted device shows a larger driving current through all the stress time. The degradation improvement of driving current is attributed to the defects passivation by fluorine. Chern et al. have proposed that the fluorine can passivate uniformly the band tail-states, which are produced due to strain bond, and midgap deep-states, which are produced due to dangling bond, within the poly-Si channel film [29]. Fluorine can break the strain bond of channel film, like Si–Si and Si–O–Si bond, to relax the local strain and also passivate the dangling bonds in grain-boundaries and HfO_2/polysilicon interface [20–22]. Therefore, hot carrier immunity is enhanced due to the strong Si–F bond.

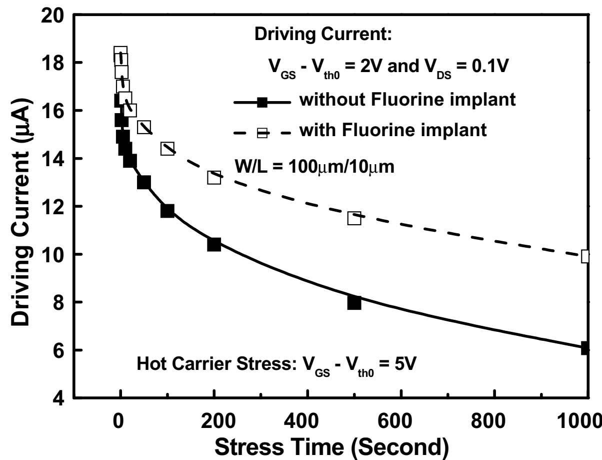

Fig. 8. The driving current of TaN/HfO_2 LTPS-TFTs with and without fluorine implantation during 1000 s hot carrier stress.

Finally, a high performance LTPS-TFT with low threshold voltage ~1.38 V, ultra-low subthreshold swing 0.132 V/decade, high I_{on}/I_{min} current ratio 1.21×10^7, and strong hot carrier immunity is derived. Consequently, the metal-gate/high-κ LTPS-TFTs with fluorine implantation is demonstrated for the first time.

4. Conclusions

The high performance LTPS-TFTs using TaN/HfO_2 gate stack structure and fluorine implantation prior the Si thin-film crystallization to passivate the defects in grain-boundaries and interface of thin-film is proposed for the first time. Improvements on higher I_{on}/I_{min} current ratio and excellent subthreshold swing are derived due to the fluorine implantation. These devices exhibit excellent electrical characteristics even without hydrogen passivation or excimer laser crystallization process steps. These results suggest that the fluorine implantation is one of the simple methods to improve the characteristics of low-temperature polycrystalline-silicon TFTs.

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References

[1] Hanari J. Development of a 10.4 in. UXGA display using low-temperature poly-Si technology. J Soc Inf Disp 2002;10:53.
[2] Oana Y. Current and future technology of low-temperature poly-Si TFT-LCDs. J Soc Inf Disp 2001;9:169.
[3] Tsutsumi K, Inoue Y, Murakami S, Sakamoto O, Ashida M, Kohno Y. A high-performance SRAM memory cell with LDD-TFT loads. In: Dig Symp VLSI Tech; 1991. p. 23–24.
[4] Hawkins WG. Polycrystalline-silicon device technology for large-area electronics. IEEE Trans Electron Dev 1986;33(4):477–81.
[5] Olasupo KR, Hatalis MK. Leakage current mechanism in sub-micron polysilicon thin-film transistors. IEEE Trans Electron Dev 1996;43(8):1218–23.
[6] Tu C-H, Chang T-C, Liu P-T, Chen C-H, Yang C-Y, Wu Y-C, et al. Electrical enhancement of solid-phase-crystallized poly-Si thin-film transistors with fluorine ion implantation. J Electrocehm Soc 2006;153(9):815–8.
[7] Tu C-H, Chang T-C, Liu P-T, Zan H-W, Tai Y-H, Yang C-Y, et al. Enhanced performance of poly-Si thin-film transistors using fluorine ions implantation. Electrocehm Solid State Lett 2005;8(9):246–8.
[8] Wang S-D, Lo W-H, Lei T-F. CF_4 plasma treatment for fabricating high-performance and reliable solid-phase-crystallized poly-Si TFTs. J Electrocehm Soc 2005;152(9):703–6.
[9] Wilk GD, Wallace RM, Anthony JM. High-k gate dielectrics: current status and materials properties considerations. J Appl Phys 2001;89:5243–6.
[10] Hung BF, Chiang KC, Huang CC, Chin Albert, McAlister SP. High-performance polysilicon TFTs incorporating $LaAlO_3$ as the gate dielectric. IEEE Electron Dev Lett 2005;26(6):384–6.
[11] Jin Zhonghe, Kwok Hoi S, Wong Man. High-performance polycrystalline SiGe thin-film transistors using Al_2O_3 gate insulators. IEEE Electron Dev Lett 1998;19(12):502–4.
[12] Lin C-P, Tsui B-Y, Yang M-J, Huang R-H, Chien CH. High-performance polysilicon TFTs using HfO_2 gate dielectric. IEEE Electron Dev Lett 2006;27(5):360–3.
[13] Hobbs C, Tseng H, Reid K, Taylor B, Dip L, Hebert L et al., 80 nm poly-Si gate CMOS with HfO2 gate dielectric. In: IEDM Tech. Dig. 2001; 651–54.
[14] Kim Y, Lim C, Young CD, Matthews K, Barnett J, Foran B, et al. Conventional poly-Si gate MOS – transistors with a novel, ultra-thin Hf-oxide layer. In: Dig. Symp. VLSI Tech. 2003;167–68.
[15] Kamins T, Marcoux PJ. Hydrogenation of transistors fabricated in Dolvcrystalline silicon films. IEEE Electron Dev Lett 1980:159–61.
[16] Mimura A, Konishi N, Ono K, Ohwada J-I, Hosokawa Y, Ono YA, et al. High performance low-temperature poly-Si n-channel TFT's for LCD. IEEE Trans Electron Dev 1989;36:351–9.
[17] Wu I-W, Huang T-Y, Jackson WB, Lewis AG, Chiang AC. Passivation kinetics of two types of defects in polysilicon TFI by plasma hydrogenation. IEEE Electron Dev Lett 1991;12:181–3.
[18] Banerjee S, Sundaresan R, Shichijo H, Malhi S. Hot-camer degradation of n-channel polysilicon MOSFET's. IEEE Trans EIectron Dev 1988;35:152–7.
[19] Hack M, Lewis AG, Wu I-W. Physical models for degradation effects in polysilicon thin-film transistors. IEEE Trans Electron Dev 1993;40:890–7.
[20] Ma TP. Effects of fluorine on MOS properties. Mat Res Soc Symp Proc 1992;262:139–741.
[21] Kouvatsos DN, Stevie FA, Jaccodine RJ. Interface statebdensity reduction and effect of oxidation temperature on fluorine incorporation and profiling for fluorinated metal oxide semiconductor capacitors. J Electrochem Soc 1993;140(4):1160–4.
[22] Kouvatsos D, Huang JG, Jaccodine RJ. Fluorine-enhanced oxidation of silicon: effects of fluorine on oxide stress and growth kinetics. J Electrochem Soc 1991;138(6):1752–5.
[23] Dimitriadis CA, Coxon PA, Dozsa L, Papadimitriou L, Economou N. Performance of thin-film transistors on polysilicon films grown by low-pressure chemical vapor deposition at various pressures. IEEE Trans Electron Dev 1992;39(3):598–606.
[24] Maegawa S, Ipposhi T, Maeda S, Nishimura H, Ichiki T, Ashida M, et al. Performance and reliability improvements in poly-Si TFT's by fluorine implantation into gate poly-Si. IEEE Trans Electron Dev 1995;42(6):1106–12.
[25] Yang C-K, Lei T-F, Lee C-L. Characteristics of top-gate polysilicon thin-film transistors fabricated on fluorine-implanted and crystal-

lized amorphous silicon films. J Electrochem Soc 1996;143(10): 3302–7.
[26] Levinson J, Shepherd FR, Scanlon PJ, Westwood WD, Este G, Rider M. Conductivity behavior in polycrystalline semiconductor thin-film transistors. J Appl Phys 1982;53(2):1193–202.
[27] Proano RE, Misage RS, Ast DG. Development and electrical properties of undoped polycrystalline-silicon thin-film transistor. IEEE Trans Electron Dev 1989;36(9):1915–22.
[28] Fortunato G, Pecora A, Tallarida G, Mariucci L, Reita C, Migliorato P. Hot carrier effects in n-channel polycrystalline-silicon thin-film transistors: a correlation between off-current and transconductance variation. IEEE Trans Electron Dev 1994;41(3):146–340.
[29] Chern HN, Lee CL, Lei TF. The effects of fluorine passivation on polysilicon thin-film transistor. IEEE Trans Electron Dev 1994;41(5): 698–702.