

High-performance top and bottom double-gate low-temperature poly-silicon thin film transistors fabricated by excimer laser crystallization

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Available online 3 December 2007

The review of this paper was arranged by Guglielmo Fortunato

Abstract

In this work, high-performance low-temperature poly-silicon (LTPS) thin film transistors (TFTs) with double-gate (DG) structure and lateral grain growth have been demonstrated by excimer laser crystallization (ELC). Therefore, the DG TFTs with lateral silicon grains in the channel regions exhibited better current–voltage characteristics as compared with the conventional solid-phase crystallized (SPC) poly-Si double-gate TFTs or conventional ELC top-gate (TG) TFTs. The proposed ELC DG TFTs ($W/L = 1.5/1.5 \mu\text{m}$) had the field-effect-mobility exceeding $400 \text{ cm}^2/\text{V s}$, on/off current ratio higher than 10^8 , superior short-channel characteristics and higher current drivability.

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Keywords: Excimer laser crystallization; Double-gate; Thin film transistor (TFT)

1. Introduction

Low-temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) fabricated by excimer laser crystallization (ELC) have been extensively studied for active matrix liquid crystal displays (AMLCDs), active matrix organic light emitting displays (AMOLEDs), and potential for three-dimension integrated circuits applications owing to their superior mobility performance [1–3]. In recent years, many efforts has been devoted to producing LTPS TFTs with silicon-on-insulator-like (SOI-like) performance by improving the channel material quality and advanced device structures of poly-Si TFTs for system-on-panel

applications [4–7]. Double-gate (DG) structure is expected to be the alternative device structure for the ultimate high-performance ideal metal oxide semiconductor field-effect transistors (MOSFETs). These devices possess the potential advantages of excellent control of short-channel effects (SCE), drain-induced-barrier-lowering (DIBL), larger on/off current ratio, and higher channel conductivity [8–17]. If this advanced structure is applied to polycrystalline-Si, the performance of TFTs will be also improved. From the perspective of improving channel quality, excimer laser crystallization (ELC) seems to be the most promising method at this moment for its great potential in mass production and high quality silicon grains without damage to glass substrates. Although large grains can be attained in the super lateral growth (SLG) regime by ELC, many fine grains still spread between these large grains due to the narrow process window for producing large grain poly-Si

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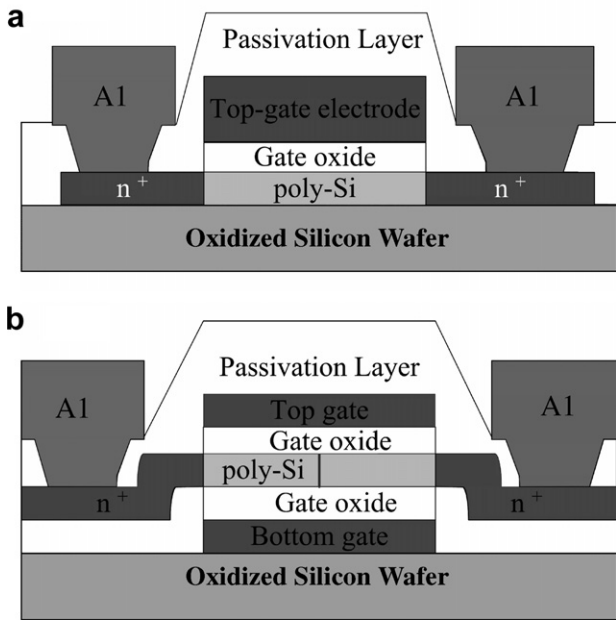


Fig. 1. The schematic cross-sectional view of the different poly-Si TFT devices. (a) Conventional n-channel top-gate TFT and (b) n-channel DG TFT.

[18,19]. Consequently, non-uniform and randomly distributed poly-Si grains will result in large variation of TFT performance when the laser energy density is controlled in the SLG regime, especially for small-dimension TFTs [20,21]. Thus, many laser crystallization methods have been proposed to produce large grains with uniformly grain size distribution, including SLS [22,23], grain filters method [24], capping the reflective or anti-reflective layer [25], phase-modulated ELC [26], dual beam ELA [27], double-pulsed laser annealing [28,29], selectively floating a-Si active layer [30], continuous-wave laser lateral crystallization [31,32], selectively enlarging laser crystallization [33,34], and so on. However, some of them need complex fabrication process or not readily be attached to the existing excimer laser annealing systems.

In this letter, high-performance double-gate LTPS TFTs with a simple excimer laser crystallization method have been demonstrated. Because of the double-gate operation mode and lateral silicon grains formed in the channel region, the devices have a high driving current, steeper sub-threshold slope, superior short-channel effect immunity, and suppression of the floating-body effect. Moreover, not only the fabrication process steps are highly compatible

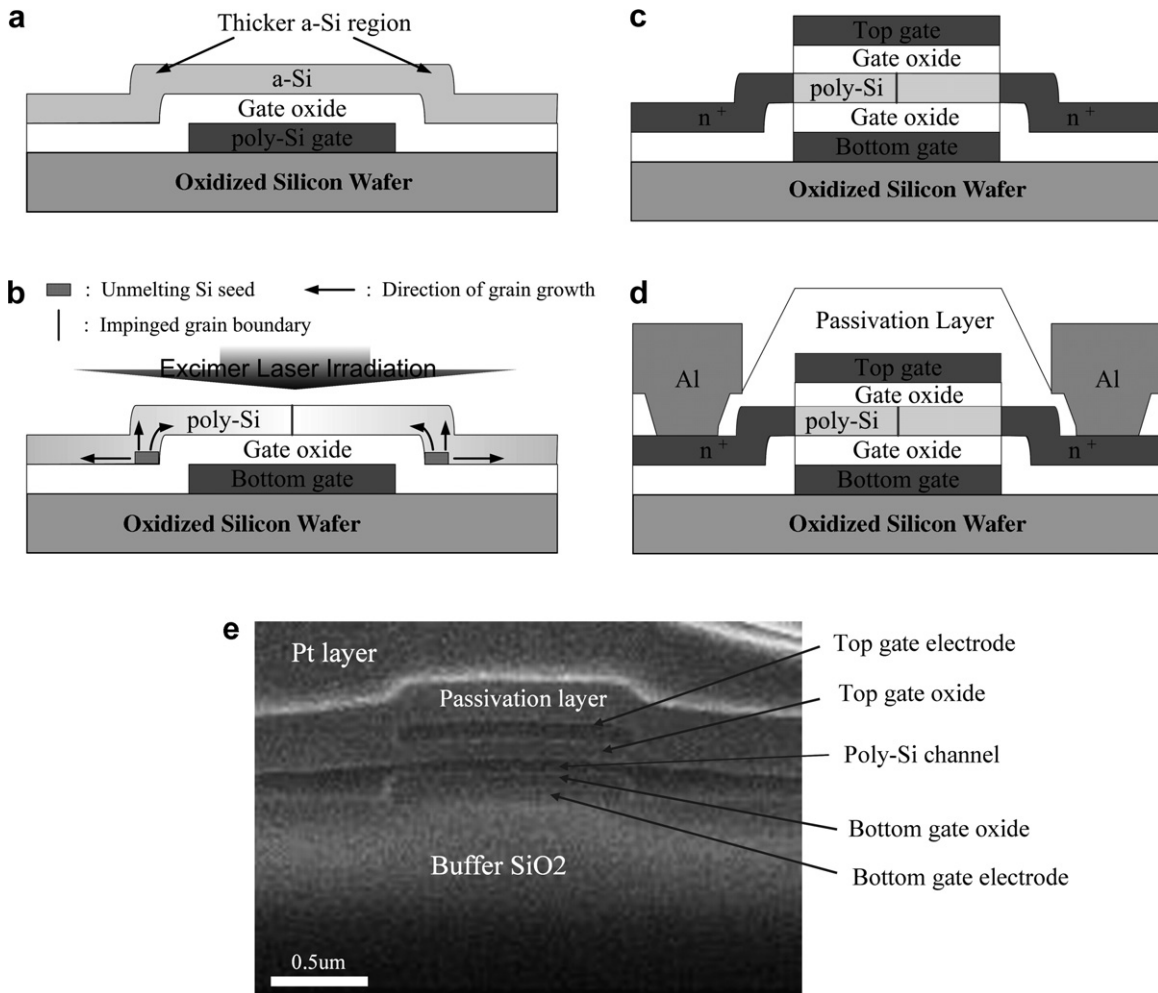


Fig. 2. (a)–(d) The key fabrication processes and (e) the cross-sectional SEM graph of proposed excimer-laser-crystallized double-gate LTPS TFTs.

with the conventional commercial a-Si TFTs but also the uniformity of device performance can be further improved.

2. Device fabrication

For the sake of simple analysis and comparison, a schematic cross-sectional view of the *n*-channel double-gate poly-Si TFT is shown in Fig. 1b along with the conventional ELC top-gate TFT, as shown in Fig. 1a. The maximum process temperature of *n*-channel LTPS TFTs fabrication is 600 °C for the dopant activation by furnace annealing. Fig. 2 displays the key fabrication steps for the proposed double-gate short-channel LTPS TFTs structure crystallized with excimer laser annealing. At first, a 1000 Å-thick phosphorus-doped poly silicon layer was deposited by low-pressure chemical vapour deposition (LPCVD) at 550 °C on silicon wafer with oxide thickness of 1 μm. After defining the bottom-gate region, a 1000 Å-thick tetraethyl orthosilicate (TEOS) bottom-gate oxide layer was deposited by plasma-enhanced chemical vapour deposition (PECVD) at 550 C following a 1000 Å-thick a-Si layer deposited by pyrolysis of pure silane (SiH₄) using LPCVD at 550 °C. After standard RCA clean process, the samples were then subjected to 248 nm KrF (Lambda Physik Excimer Laser LPX 210i) excimer laser crystallization (ELC). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10⁻³ Torr and substrate was maintained at room temperature. The laser beam was homogenized into a semi-gaussian shape in the short axis and a flat-top shape in the long axis. The number of laser shots per area was 20 (i.e. 95% overlapping) and laser energy density was varied.

A scanning electron microscopy (SEM) (S4700, Hitachi) is used to get the surface micrograph of poly-Si thin films after Secco-etch. After laser crystallization, the poly-Si active layers were etched to define the active channel region, and a 1000 Å-thick TEOS top-gate oxide was subsequently deposited. Poly-Si layer was deposited by LPCVD for formation of the top-gate electrode at 550 °C. Then, the poly-Si thin films were etched by RIE to form top-gate electrodes and a phosphorous ion implantation with dose of 5 × 10¹⁵ cm⁻² was carried out to form source and drain regions. Next, a TEOS passivation oxide layer was deposited by PECVD and the implanted dopants were activated by thermal annealing at 600 °C for 12 h. Contact holes opening and metallization were carried out to complete the fabrication of DG TFTs. Then, a 30-min sintering process was performed in N₂ ambient at 400 °C to reduce the contact series resistance of the source and drain electrodes. Finally, LTPS TFTs were passivated by 2-h NH₃ plasma treatment to further improve the device performance. Fig. 2e was the cross-sectional SEM graph of the completed excimer-laser-crystallized double-gate LTPS TFTs. For comparison, the conventional SPC DG TFTs and conventional ELC TG ones with using the super lateral growth (SLG) laser annealing condition were also fabricated in the same run.

After TFTs formation, an automatic measurement system that combines IBM PC/AT, semiconductor parameter analyzer (4156C, Agilent Technologies) and a probe station were used to measure the *I*–*V* characteristics. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_{ds} = (W/L) \times 10^{-8}$ A at $V_{ds} = 0.1$ V. The field-effect mobility and subthreshold

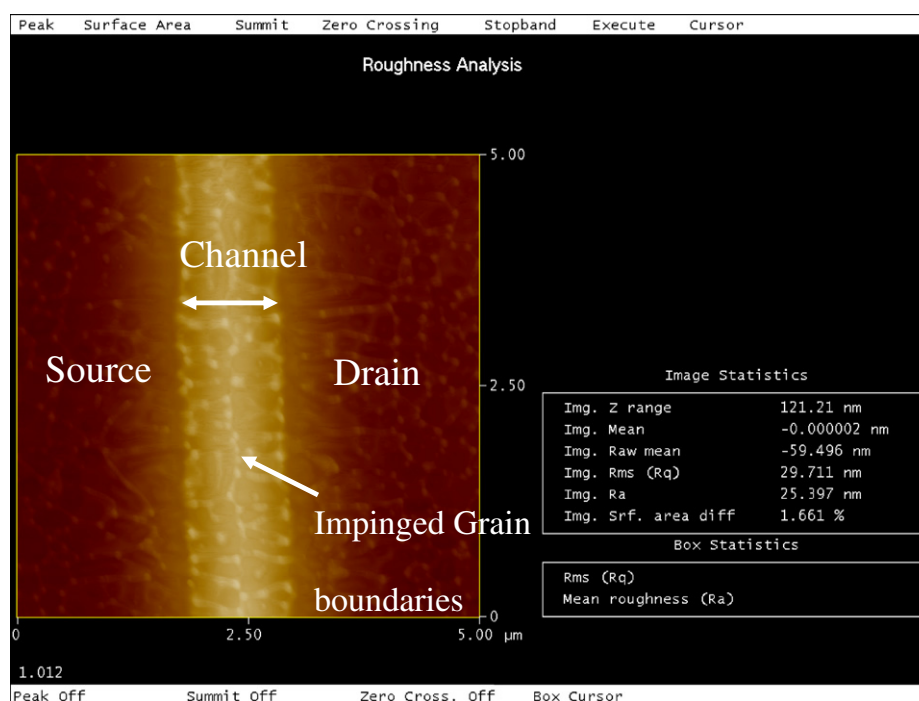


Fig. 3. AFM images of poly-Si thin film with bottom-gate structure after laser irradiation.

swing were extracted at $V_{ds} = 0.1$ V, and the I_{on}/I_{off} current ratio was defined at $V_{ds} = 3$ V. An analytical transmission electron microscopy (TEM) (JEM-2000FX, JEOL Ltd.) was employed to analyze the microstructure of poly-Si films and the device structure of TFTs. Cross-sectional TEM samples were prepared by focused-ion-beam (FIB) technique (Nova 200, FEI Company).

3. Results and discussion

Fig. 2b shows the schematic illustration of lateral grain growth mechanism using plateau structure of a-Si thin film with excimer laser crystallization. When the excimer laser irradiation is applied on the a-Si thin film, the applied laser energy density is controlled to completely melt the thin region of a-Si film in the channel region. Since the laser energy density is almost uniform in a local region, if the thickness of thick region of a-Si film near the edges of bottom-gate is thick enough, the thick region of a-Si film is partially melted, and a lot of un-melting solid seeds remain near the edges of bottom-gate electrode. As a result, a lateral temperature gradient can be produced between the local thin and thick regions of a-Si film, and grains will grow laterally towards the complete melting region from the un-melting solid seeds. Therefore, the lateral grain growth can be artificially controlled in the channel region of DG TFTs and only one grain boundary perpendicular to the direction of current flow is formed in the middle of the channel region. Atomic force microscopy (AFM) analysis is used to investigate the surface morphology of silicon thin film after laser crystallization. Fig. 3 exhibits that the ridge and hillock occur at the grain boundaries located at the center of channel where two grains collide due to the freezing of capillary waves excited in the melting silicon during laser crystallization [35]. The protruded grain boundaries will cause severe gate leakage and thicker gate dielectric must be integrated into poly-Si TFTs for better reliability.

In order to investigate the relationship between laser energy density and length of lateral grain growth, the channel length was adjusted to laser energy density of 450 mJ/cm² and laser shot number of 1 shot. Fig. 4a–c show the SEM graphs of poly-Si thin films irradiated by excimer laser in which the device channel length was 1.2, 1.5, 2 μm , respectively. As the device channel length was less than 1.5 μm , there were always two columns of longitudinal grains colliding in the middle of channel region. Fig. 5 shows the typical transfer and output characteristics of proposed ELC DG LTPS TFT (Fig. 1b) and conventional SPC DG TFT and conventional ELC TG TFT (Fig. 1a) for $W = L = 1.5$ μm . The nominal mobility of the DG TFT was calculated from transconductance (g_m), which we defined as a TG TFT of the same gate length and gate width with a 100 nm gate-SiO₂ layer. Owing to both of the uniformly large transverse grains grown in the device channel region and double-gate operation mode, this proposed ELC DG TFT exhibits better electrical char-

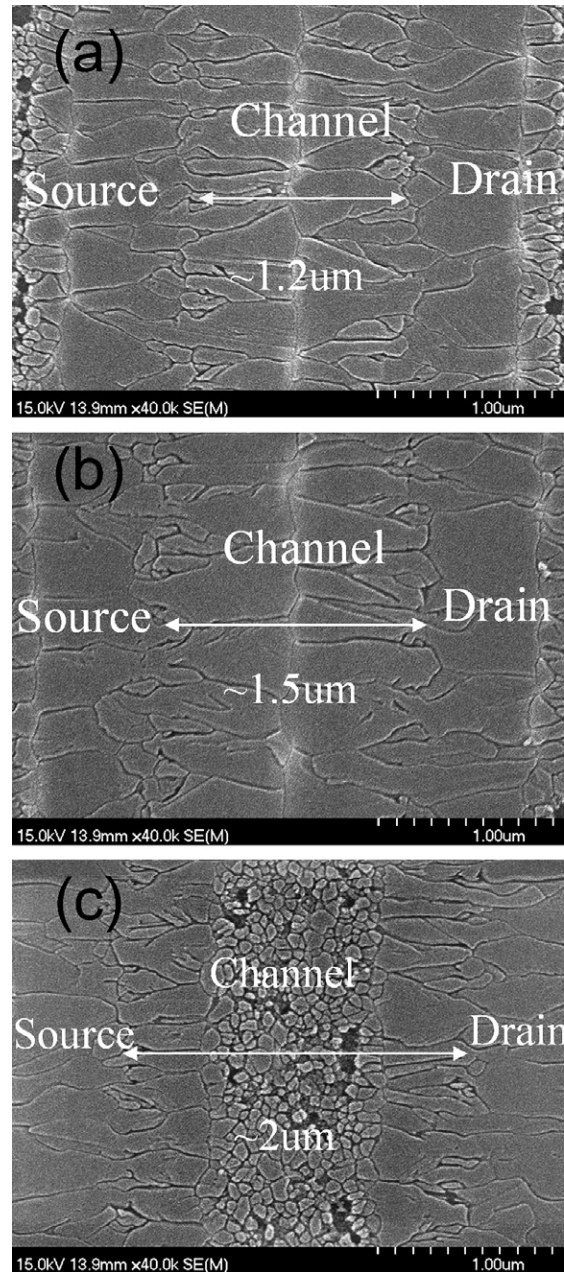


Fig. 4. Scanning electron microscope micrographs of excimer laser crystallized poly-Si film with bottom-gate structure after Secco etch, in which the device channel length was 1.2, 1.5, 2 μm , respectively.

acteristics, and Table 1 lists several important electrical characteristics of the three different TFTs. Via the top and bottom-gates connected together, the higher electron density in the channel region at on state and the channel is more efficiently modulated by both gate electrodes [36]. Obvious improvement in devices characteristics is obtained for ELC DG TFTs instead of ELC TG TFTs; field-effect-mobility increases from 129 to 396 cm²/V s. But the proposed ELC DG TFT has a high off-current under a large negative gate bias at the $V_{ds} = 3$ V from the I_d - V_g transfer characteristics. The large leakage current indicates that ELC DG TFTs suffer a higher lateral peak electric field

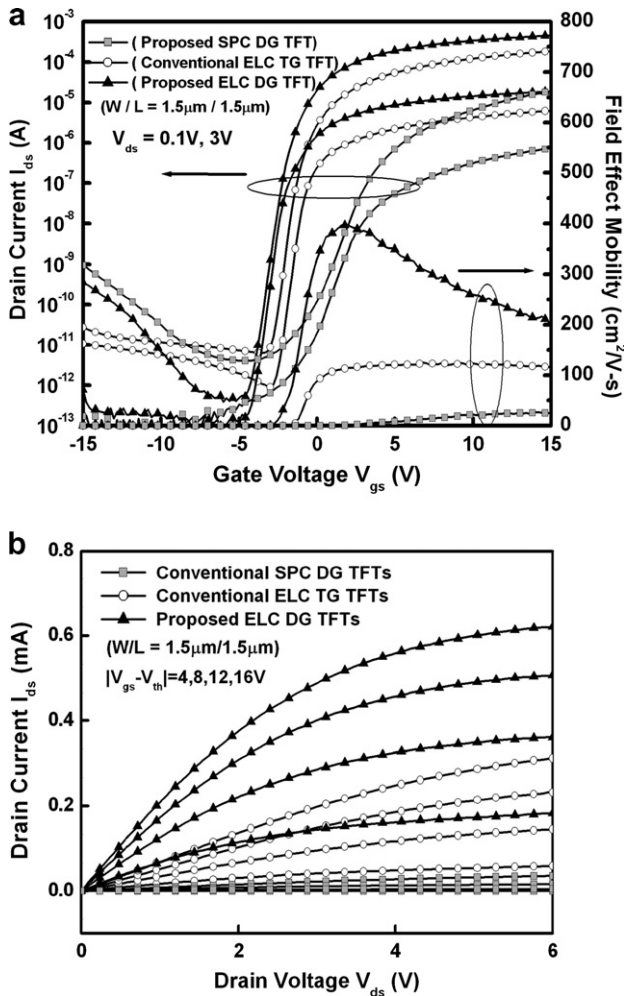


Fig. 5. I - V curves of proposed ELC DG TFT, conventional SPC DG TFT, and conventional ELC TG TFT. (a) Transfer characteristics. (b) Output characteristics.

than the ELC TG TFT [37]. If lightly-doped-drain (LDD) and gate-overlapped lightly-doped-drain (GOLDD) structures were applied to the ELC DG TFTs, the severe anomalous off-current could be relieved by reducing the lateral peak electric field in the drain region. In order to avoid the threshold voltage difference, the applied gate driving voltages in Fig. 5b are kept at constant values of $|V_g - V_{th}| = 4, 8, 12$ and 16 V, respectively. It is demonstrated that the ELC DG poly-Si TFTs exhibit higher driving capability due to both of the location-controlled silicon grains in the channel and double-gate operation mode. Take the $|V_g - V_{th}| = 16$ V as an example, the current drivability of ELC DG poly-Si TFTs is about two times as

large as that of an ELC TG poly-Si TFT and seventeen times as large as that of a SPC DG poly-Si TFT under the same bias condition. At higher gate voltages, however, the current ratio between these three devices decreases. The plausible reason is the self-heating effect due to the large driving current on the poor thermal conducting SiO_2 substrate. It also clearly shows that ELC DG poly-Si TFTs provide better current saturation characteristics than the other two TFTs. The superior short-channel characteristics and driving capability imply that the proposed ELC DG-TFT structure is more suitable for high-resolution AMLCDs, and AMOLEDs application.

The grain boundary trap state densities (N_t) of the conventional TG and proposed DG poly-Si TFTs were estimated according to the modified Levinsons analysis [38,39]. The N_t was extracted from the slopes of $\ln(I_D/V_{GS})$ versus $1/(V_{GS})$. Fig. 6 displays that ELC DG poly-Si TFT exhibits a smaller N_t of $3.29 \times 10^{11} \text{ cm}^{-2}$ than that of conventional ELC TG TFT. This result implies that DG TFTs with lateral silicon grains possess better crystallinity and fewer microstructure defects which are also confirmed by cross-sectional TEM image of excimer laser crystallized poly-Si thin films with plateau structure shown in the Fig. 7. The inset of Fig. 7 shows the electron diffraction pattern of the one of lateral silicon grains in the channel regions above the bottom-gate electrode. The diffraction pattern reveals that the lateral silicon grain exhibits $\langle 123 \rangle$ orientation with respect to the normal direction of

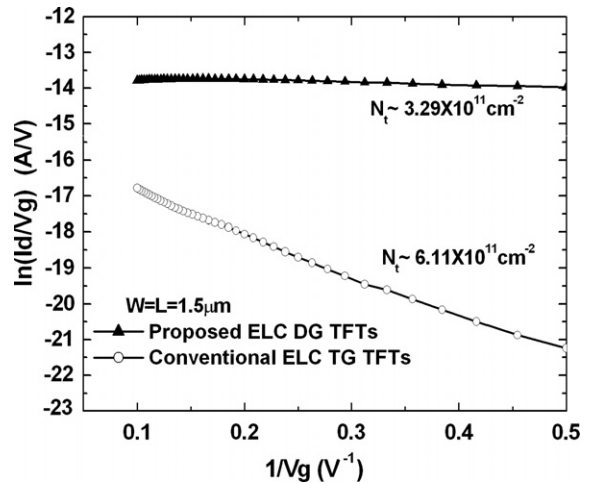


Fig. 6. Plot of $\ln(I_D/V_{GS})$ versus $1/(V_{GS})$ curves at $V_{DS} = 0.1$ V and high V_{GS} for DG and TG poly-Si TFTs.

Table 1

Measured electrical characteristics of ELC DG TFTs with lateral grain growth, SPC DG TFTs, and conventional ELC TG TFTs

TFT structures ($W = L = 1.5 \mu\text{m}$)	Threshold voltage (V)	Field-effect-mobility ($\text{cm}^2/\text{V s}$)	Subthreshold swing (V/dec)	On/off current ratio
Conventional SPC double-gate TFT	2.92	29.2	0.598	4.82×10^6
Conventional ELC top-gate TFT	-1.17	129	0.345	4.32×10^7
Proposed ELC double-gate TFT	-2.48	396	0.335	9.21×10^8

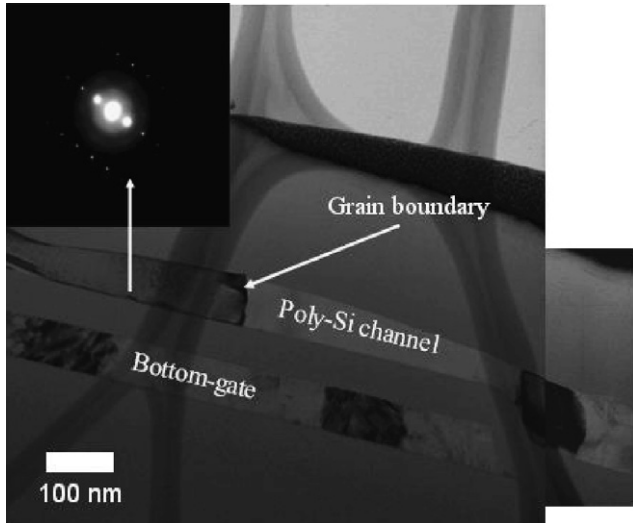


Fig. 7. FIB-prepared cross-sectional TEM image of excimer laser crystallized poly-Si film with plateau structure.

the paper and the crystallinity within this lateral silicon grain is excellent attributed to the clear dot pattern.

The dependence of field-effect mobility on temperature for ELC DG TFTs with lateral silicon grains, ELC TG TFTs with random silicon grains and SPC DG TFTs was investigated to study the electron-transport-scattering mechanism of poly-Si thin films, as shown in the Fig. 8. For ELC TG TFTs with random silicon grains, the electron field-effect-mobility increases as the temperature increases. Such positive temperature dependency of field-effect-mobility is attributed to the reduced grain boundary scattering where the probability of carrier transport over the grain boundary potential barrier height by thermionic emission increases [40]. On the other hand, negative dependency of field-effect-mobility for ELC DG TFTs with lateral silicon grains indicates lattice-phonon scattering is the dominate scattering mechanism because only one grain boundary perpendicular to the direction of current flow in the channel region. The field-effect-mobility of SPC DG

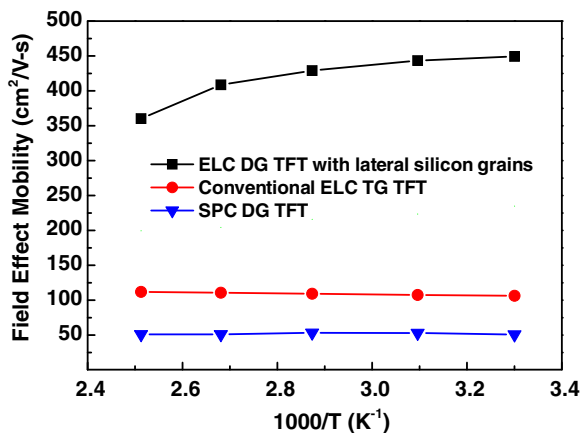


Fig. 8. The dependence of field-effect mobility on temperature for ELC DG TFTs with lateral silicon grains, ELC TG TFTs with random silicon grains and SPC DG TFTs.

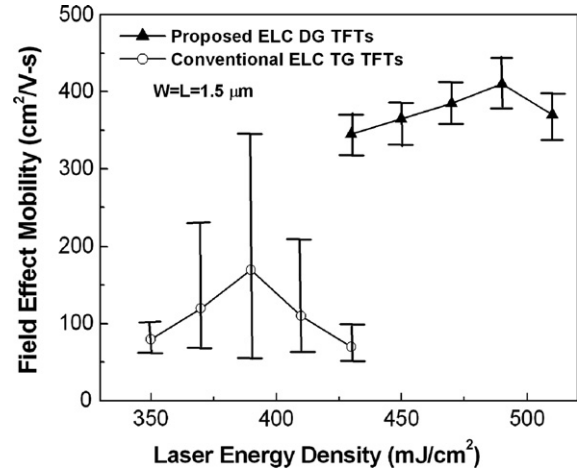


Fig. 9. Dependence of field-effect-mobility on applied laser energy density for ELC DG TFTs with lateral silicon grains and conventional ELC TG ones.

TFTs increase as first and then starts to decrease as the temperature increases, indicating grain-boundary scattering and lattice-phonon scattering compete with each other and dominate under different temperature.

Fig. 9 displays the dependence of field-effect mobility on laser energy densities for DG TFTs and conventional TG ones whose channel length is 1.5 μm . Twenty TFTs were measured for each laser irradiation condition to investigate the device-to-device uniformity. Compared to the conventional ELC TG-TFTs, it was found that ELC DG-TFTs with lateral silicon grains exhibited smaller electrical deviation since the number of spontaneous small grains and grain boundaries were reduced and the uniformity of TFTs performance could be improved with artificially laterally-grown grains.

4. Conclusions

A novel high-performance DG LTPS TFTs have been fabricated by excimer laser crystallization. Poly-Si TFTs exhibit high field-effect-mobility of 400 $\text{cm}^2/\text{V s}$ and excellent short-channel characteristics because of the large transverse grains artificially grown in the channel region and double-gate structure for better gate controllability. In addition, the experimental results reveal a steeper sub-threshold value, higher driving current, and excellent device uniformity in proposed TFTs. The ELC DG TFTs are therefore ideally suitable for future system-on-panel and three-dimensional integrated circuit applications.

Acknowledgements

The authors thank the National Science Council of Taiwan for financial support of this research under Contract No. NSC 95-2221-E-009-252, and the Nano Facility Center (NFC) of National Chiao Tung University and National Nano Device Laboratories (NDL) for providing process equipment.

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