High-Performance and High-Reliability 80-nm Gate-Length DTMOS with Indium Super Steep Retrograde Channel

Sun-Jay Chang, Chun-Yen Chang, *Fellow, IEEE*, Coming Chen, Tien-Sheng Chao, *Member, IEEE*, Yao-Jen Lee, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*— In this paper, we demonstrate for the first time a high-performance and high-reliability 80-nm gate-length dynamic threshold voltage MOSFET (DTMOS) using indium super steep retrograde channel implantation. Due to the steep indium super steep retrograde (In-SSR) dopant profile in the channel depletion region, the novel In-SSR DTMOS features a low V_{th} in the off-state suitable for low-voltage operation and a large body effect to fully exploit the DTMOS advantage simultaneously, which is not possible with conventional DTMOS. As a result, excellent 80-nm gate length transistor characteristics with drive current as high as 348 μA/μm (off-state current 40 nA/μm), a record-high $Gm = 1022$ mS/mm, and a subthreshold slope of 74 mV/dec, are achieved at 0.7 V operation. Moreover, the reduced body effects that have seriously undermined conventional DTMOS operation in narrow-width devices are alleviated in the In-SSR DTMOS, due to reduced indium dopant segregation. Finally, it was found for the first time that hot-carrier reliability is also improved in DTMOS-mode operation, especially for In-SSR DTMOS.**

***Index Terms*—DTMOS, indium, super-steep-retrograde (SSR) channel.**

I. INTRODUCTION

As MOSFETs scale to subquarter-micrometer regime and beyond, an effective way to improve subthreshold turn-off and to alleviate short-channel effects (SCEs) is to increase the substrate doping. A uniform increase in substrate doping, however, suffers from undesirable channel mobility reduction, junction capacitance increase, and high threshold voltage. To circumvent these shortcomings, MOSFETs with a retrograde channel profile have been proposed [1]. In a retrograde channel, the peak substrate doping is positioned beneath the surface, leaving a lightly doped surface channel region [2]. Super-steep-retrograde (SSR) channel, which features a sharp transition from the lightly doped surface to the heavily doped substrate, has been proposed for transistors with channel length smaller than 0.1 μm [3]–[5]. The SSR scheme allows the transistor to exhibit a high driving current characteristic of the lightly doped surface channel with a low surface impurity scattering, while also simultaneously preserving a good V_{th}-roll-off behavior due to a reduced channel depletion width which improves punchthrough control. Indium dopant with its low diffusion coefficient at elevated temperature is known to be an ideal candidate to form SSR profile for subquarter-micron nMOSFETs.

On the other hand, the power supply voltage, V_{DD}, is scaling down at a faster pace than threshold voltage scaling. This has resulted in current drive reduction and therefore speed degradation. To improve the current drive capability of MOSFETs at low supply voltage (e.g., $V_{DD} < 0.7$ V), Assaderaghi *et al.* [6] proposed the use of **D**ynamic **T**hreshold Voltage **MOS**FET (DTMOS) for ultralow voltage applications. By shorting the gate to the body, the V_{th} in DTMOS mode is reduced in the on-state to boost the current drive; while the device exhibits the normal V_{th} in the off-state to maintain a low stand-by power. The DTMOS scheme thus appears to be very promising for future low-power and high-speed circuit applications, since it improves the circuit speed without compromising the stand-by power. Previously reported DTMOS's, however, suffer from a small body-effect-factor (γ) [7]. This is because the normal V_{th} suitable for low V_{DD} operation is usually too small to be compatible with a high substrate doping concentration, resulting in a low γ. A low γ prevents the DTMOS from enjoying a large V_{th} reduction in the on-state, thus minimizes its gain in on-state current-drive during DTMOS-mode operation [7]–[10]. Recently, we have proposed a new DTMOS using an SSR channel profile by indium implantation to overcome the above shortcomings [11]. In this paper, a comprehensive comparison of the In-SSR DTMOS and conventional BF_2-DTMOS, with 80-nm channel length has been reported.

II. EXPERIMENTAL

Devices with channel length down to 80 nm were fabricated on 8-in silicon wafers with resistivity of 15 to 25 Ω-cm. Wafers were processed using a conventional CMOS twin-well process flow. Shallow trench isolation (STI) was used for device isolation. To form SSR channel, a 150 keV indium channel implant with a dose of 1×10^{13} cm^{-2} was conducted. Conventional

Manuscript received March 21, 2000; revised July 26, 2000. This work was supported in part by the National Science Council of the Republic of China under Contract NSC 89-2215-E-317-004.

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Publisher Item Identifier S 0018-9383(00)10404-6.

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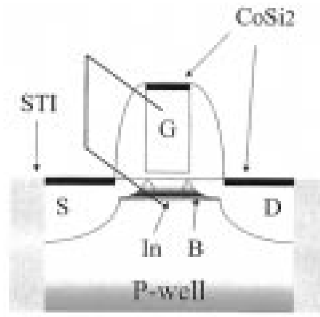

Fig. 1. Schematic of indium super steep retrograde (In-SSR) DTMOS.

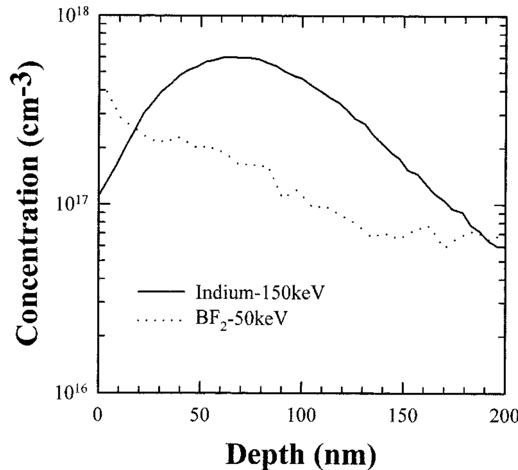

Fig. 2. SIMS profiles of In and B in the channel region.

devices with BF_2-implant (at 50 keV, 6×10^{12} cm^{-2}) were also processed in the same lot to serve as the control. A 2.6-nm gate oxide was grown using rapid thermal oxidation (RTO) at 850 °C, followed by the deposition of a 200-nm polysilicon gate. After gate patterning, a 20-nm offset-space (i.e., a narrow spacer) was used to reduce the gate-to-drain capacitance and suppress the short channel effects. Ultrashallow S/D extensions were then formed by a 4 keV As implant, followed by a boron pocket implant (i.e., 20 keV, 1×10^{13} cm^{-2}, tilt angle 20°). Afterwards, a 0.1 μm sidewall spacer was formed. Then, a deep source/drain junction was formed by As ion implantation at 40 keV. Finally, wafers were annealed by rapid thermal processing (RTP) at 1000 °C for 20 s, followed by $CoSi_2$ salicidation. Wafers were then processed through a standard backend flow to completion. The device structure of 80-nm gate-length In-SSR DTMOS is shown in Fig. 1.

III. Results and Discussion

A. Short-Channel In-SSR DTMOS Performance

The resultant channel profiles measured by the secondary ion mass spectroscopy (SIMS) for In-SSR and conventional BF_2-implanted samples are shown in Fig. 2. The channel profiles are measured after all processing steps. Compared to BF_2-implanted control, In-implanted sample exhibits a well-behaved Gaussian profile, in which the surface doping concentration is low while the concentration underneath the channel increases abruptly. The surface channel concentration is 1×10^{17} cm^{-3} for In-SSR sample, compared to 4×10^{17} cm^{-3} for BF_2-implanted control. V_{th} roll-off characteristics are shown in Fig. 3. The threshold voltage is deduced from $Gm_{\max}$ method at $Vd = 0.1$ V. It can be seen that short-channel effects are effectively suppressed in In-SSR DTMOS due to a smaller drain depletion layer. In addition, In-SSR devices also depict a larger V_{th} reduction under DTMOS mode, compared to BF_2 counterparts, due to a larger body effect factor (γ). It has also been explicitly explained that SSR DTMOS shows the improved γ and hence performance [8]. It is worthy to note here that the amount of V_{th} reduction in 80-nm gate length devices are 40 mV for In-SSR DTMOS, compared to 18 mV for BF_2 DTMOS, despite the fact that the V_{th} of In SSR device is smaller than that of the BF_2 control. Fig. 4 compares the saturated transconductance ($Gm.sat$) versus drain-induced-barrier-lowering (DIBL) for In-SSR and BF_2-implanted devices both under standard- and DTMOS-modes at 0.7 V operation. For the standard-mode operation, In-SSR device depicts better

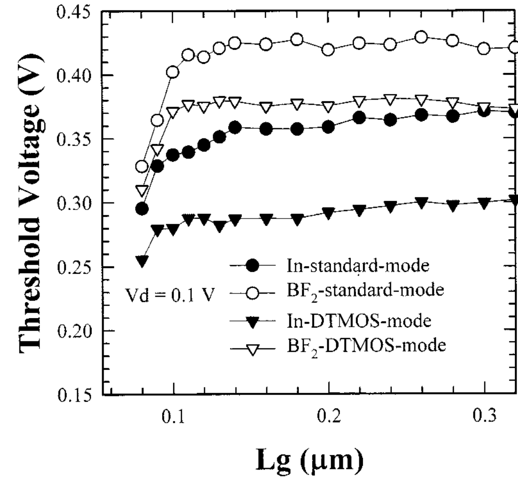

Fig. 3. Threshold voltage versus gate length (Lg) for In-SSR and BF_2-implanted devices, both under standard- and DTMOS-modes. The threshold voltage is taken at $Vd = 0.1$ V.

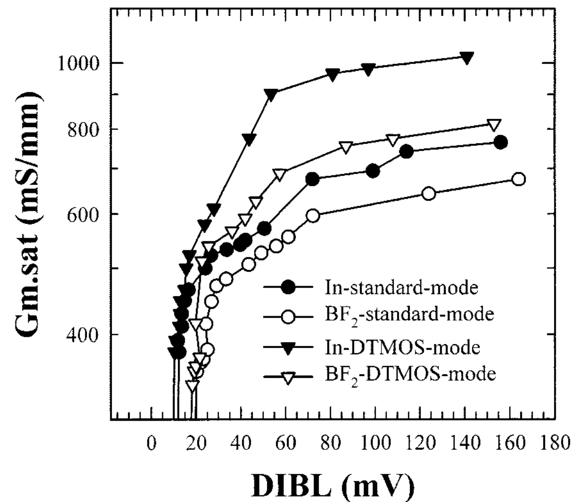

Fig. 4. The gm versus drain-induced-barrier-lowering (DIBL) for In-SSR and BF_2-implanted devices, both under standard- and DTMOS-modes. The DIBL is taken between $Vd = 0.1$ and 0.7 V.

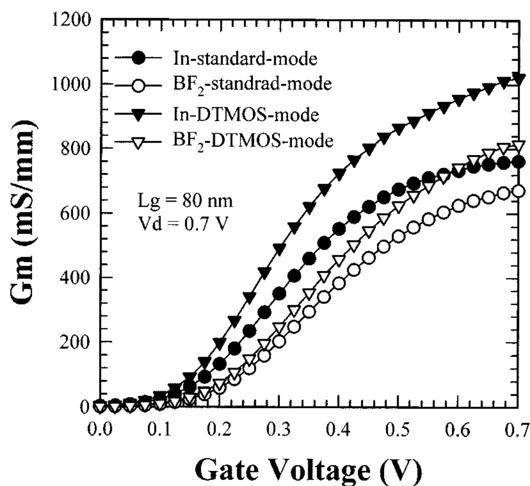

Fig. 5. The Gm–Vg characteristics for In-SSR and BF_2-implanted devices, both under standard- and DTMOS-modes. The gate length is 80 nm.

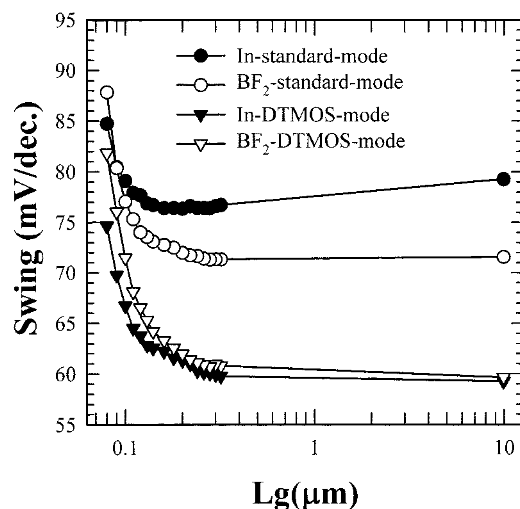

Fig. 6. Subthreshold swing as a function of Lg for In-SSR and BF_2-implanted devices, both under standard- and DTMOS-modes.

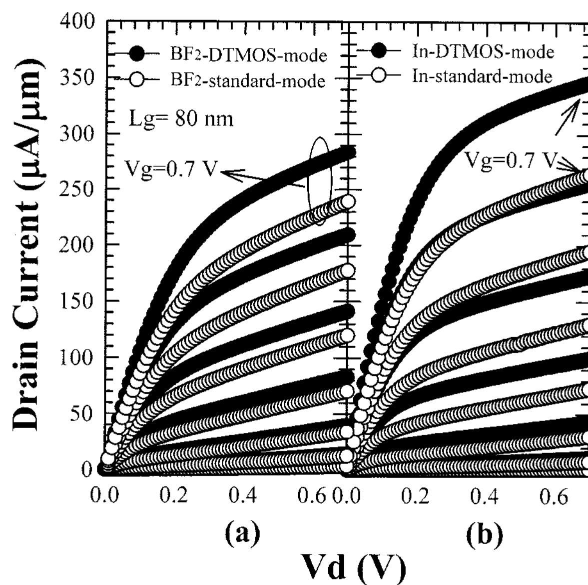

Fig. 7. Drain current of (a), BF_2-implanted, and (b) In-SSR devices, both under standard- and DTMOS-modes. The gate length is 80 nm. Vg varies from 0 to 0.7 V in 0.1 V steps.

characteristics than the BF_2-implanted counterpart, and can be attributed to its super steep channel profile. While for the DTMOS-mode operation, In-SSR DTMOS also depicts higher saturated Gm for a given DIBL, compared to BF_2-DTMOS. Furthermore, the improvement of In-SSR DTMOS is higher than that of BF_2 DTMOS. We believe this is again due to the higher substrate doping and a larger body factor in In-SSR device. This is because the larger body factor of In-SSR DTMOS will lead to a larger current drive increment, and therefore a higher Gm improvement. Furthermore, a larger body factor of In-SSR DTMOS will also result in a more effective reduction in the drain depletion layer, and therefore more effective DIBL suppression. In fact, a record high Gm of 1022 mS/mm was achieved at 0.7 V operation for the 80-nm gate-length In-DTMOS, as shown in Fig. 5. In addition, the Gm ratio ($Gm_{\mathrm{DTMOS}}/Gm_{\mathrm{Standard}}$) are 1.34 and 1.21 for In-SSR and for BF_2 devices, respectively. It is worthy to note here that the off-state current of In-SSR DTMOS is larger than that of BF_2-DTMOS (i.e., 40 nA/μm compared to 31 nA/μm) due to the smaller V_{th}. In general, low V_{th} devices also show a small body effect (gamma) and thus reduce the dynamic efficiency of DTMOS. On the contrary, In-SSR device shows the combination of low V_{th} and high body effect simultaneously (i.e., higher dynamic efficiency) which allows a full exploitation of DTMOS. The subthreshold swing factors are plotted as a function of channel length Lg in Fig. 6. It is interesting to note that In-SSR devices actually depict worse subthreshold swing than the BF_2-implanted counterparts under standard-mode operation. This is because of a shallower channel depletion layer in the indium-implanted channel, resulting in a larger depletion capacitance and therefore a larger subthreshold swing. However, the subthreshold swing of the In-SSR devices operating under DTMOS mode is significantly improved, and becomes even better than that of the BF_2-implanted controls operating under DTMOS mode, due to a larger γ. This is because as the Vg increases, the V_{th} decreases more aggressive for a larger γ DTMOS, thus the drain current increases more rapidly, resulting in a sharp Id–Vg slope (i.e., better subthreshold swing). Fig. 7 shows the output characteristics of 80 nm BF_2-SSR and In-implanted devices both under standard- and DTMOS-mode operations. The gate voltage is varied from 0 to 0.7 V in 0.1 V steps. The improvement in current drive (measured at $V_D = Vg = 0.7$ V) due to DTMOS-mode operation are 18.8% and 32% for BF_2-DTMOS and for In-SSR DTMOS, respectively.

B. Narrow-Channel Characteristics

Fig. 8 shows the body effects of nMOSFETs with In-SSR and BF_2-implant (i.e., control). The device threshold voltage V_{th} is plotted as a function of the body bias for long channel transistors with narrow- and wide-channel widths. We found that the V_{th} of In-SSR split is more sensitive to body bias (i.e., it depicts a larger γ) for both wide and narrow transistors, compared to BF_2-implanted control. This is primarily due to

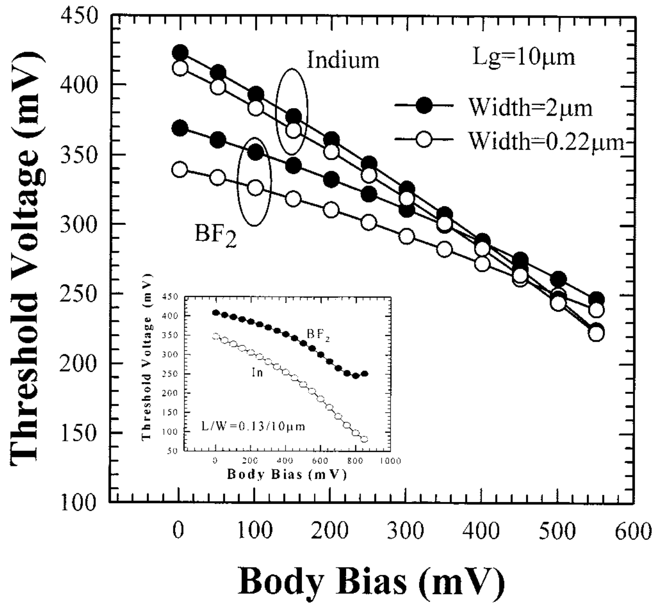

Fig. 8. Dependence of threshold voltage on the body bias for BF_2-implanted and In-SSR devices with channel width of 0.22 and 2 μm. Inset shows the result for short-channel devices with $L/W = 0.13$ μm/10 μm.

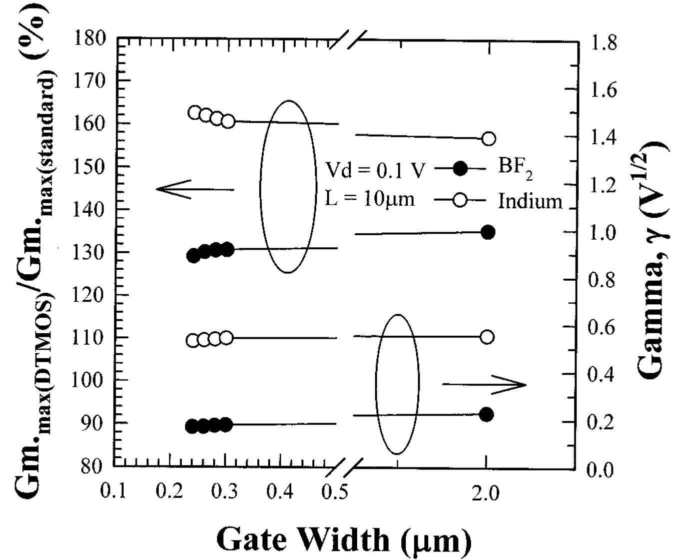

Fig. 9. Gm ratio and γ versus gate width for BF_2-implanted and In-SSR DTMOS. BF_2-DTMOS shows Gm ratio degradation in narrow-channel devices.

the steep indium dopant profile in the channel depletion layer, as has been confirmed from SIMS analyses (shown previously in Fig. 2). In addition, the V_{th} of In-SSR devices show a less dependence on channel width, compared to BF_2-implanted controls. In the insert of Fig. 8, we plot the V_{th} as a function of body bias for a short channel (i.e., 0.13 μm) device. It is found that In-SSR device indeed depicts a larger body effect, albeit its V_{th} is lower than that of BF_2-implanted control. It is worthy to note here that we have chosen an indium implant dose of 1×10^{13} cm^{-2}, because it has been previously reported that the achievable body effect factor saturates at around this dose, with a corresponding doping concentration of no more than 7–8 $\times$ 10^{17} cm^{-3} [12]. In addition, the V_{th} of In-SSR devices are larger than BF_2 devices in long channel region (i.e., 10 μm), and smaller than BF_2 devices in short channel region. This is mainly because the In-SSR devices suffer from indium de-activation. So the V_{th} (standard device) shows a long-distance roll-off behavior which have been reported previously [12]. Fig. 9 shows the plot of linear transconductance (Gm) ratio ($Gm_{\rm DTMOS}/Gm_{\rm Standard}$) and the body effect factor (γ) versus the coded channel width $W_{\rm coded}$ for both In-SSR and BF_2-implanted controls. Compared to the BF_2-implanted counterparts, In-SSR DTMOSs show a higher Gm ratio and γ. More importantly, while the ratio of BF_2-implanted devices shows a 6% reduction when *Wcoded* reduces from 2 to 0.22 μm, a 5.5% increase is found for In-SSR devices instead. The undesirable γ and V_{th} reduction in the narrow-channel devices for the BF_2-implanted controls are believed to be due to the boron diffusion and segregation into the edge in the channel width direction [13]. Since In-SSR DTMOS is less susceptible to such undesirable dopant segregation, it can therefore fully exploit the high current drive and low standby power features of DTMOS, even in narrow-channel devices.

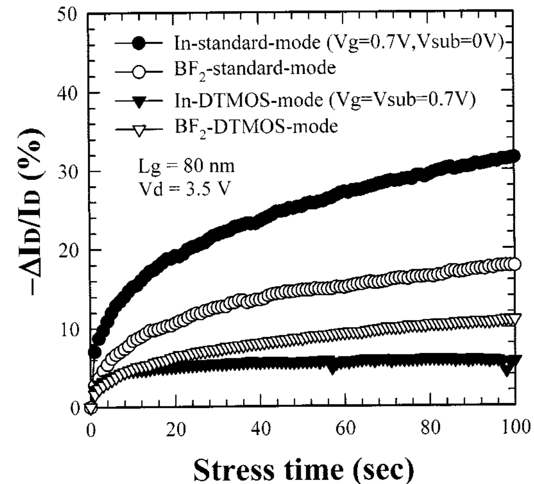

Fig. 10. Hot-carrier degradation of 80-nm gate-length standard and DTMOS devices.

C. Hot-Carrier Reliability

Hot-carrier reliability of In-SSR and BF_2-implanted 80-nm gate-length devices both under standard- and DT-modes has been investigated. Hot-carrier-induced drain current degradation is plotted in Fig. 10. In-SSR device shows a worse hot-carrier resistance, compared to BF_2-implanted control, both under standard-mode operation. This is consistent with previous literature report that most channel conducting electrons are located in the lightly doped surface channel in In-SSR device, thus more electrons are available for injection into the oxide [14]. Surprisingly, it is observed for the first time that hot carrier degradation is actually reduced in DTMOS-mode operation for both In-SSR and BF_2-implanted control. More importantly, the improvement is so dramatic in In-SSR DTMOS that it depicts an even smaller hot-carrier degradation than BF_2-implanted DTMOS control. This can be attributed to the bulk charge being shared by the high

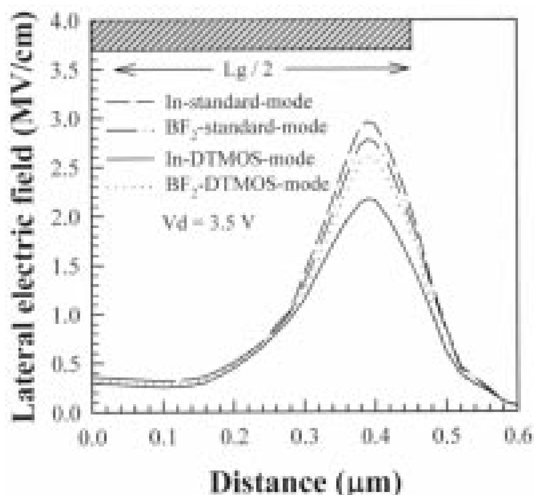

Fig. 11. Simulated lateral channel electric field distributions for both In-SSR and BF_2-implanted devices under standard- and DT-modes.

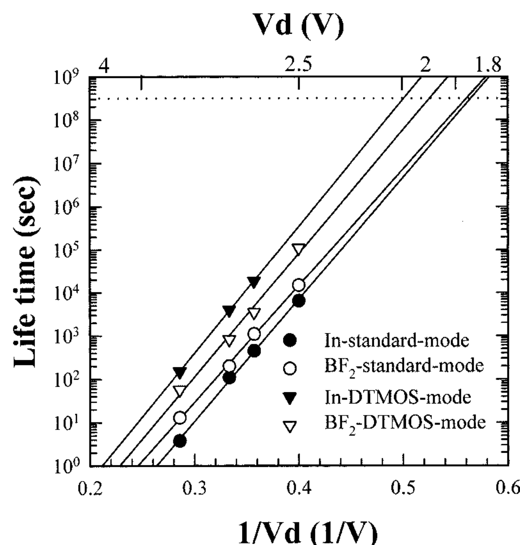

Fig. 12. Hot-carrier lifetime of 80-nm gate-length standard and DTMOS devices.

body potential under DTMOS-mode, thus the maximum drain electric field is reduced. The simulated lateral channel electric field distributions for both In-SSR and BF_2-implanted devices under standard- and DT-modes are shown in Fig. 11. The simulated lateral channel electric field is at 3 nm below the Si/SiO_2 interface. Although the lateral channel electric field of In-SSR device is larger than that of BF_2 under standard-mode operation, the electric field of In-SSR DTMOS is indeed smaller than that of BF_2-implanted DTMOS. This is because In-SSR device has a higher γ, thus the bulk charge sharing is larger than that of BF_2-implanted DTMOS with a smaller γ, resulting in a smaller channel electric field. The hot carrier lifetime versus stressing drain voltage is plotted in Fig. 12. Although In-SSR device depicts a worse hot-carrier lifetime than BF_2 control under standard-mode operation, In-SSR DTMOS exhibits a superior lifetime than BF_2-implanted DTMOS.

IV. Conclusion

A novel high-performance and high-reliability 80-nm gate-length DTMOS suitable for low-voltage ($V_{DD} < 0.7$ V) applications has been proposed by using indium super-steep-retrograde (SSR) channel implantation. The new In-SSR DTMOS has a large dynamic threshold efficiency at a low V_{th} compatible with low-voltage applications, due to its low surface concentration and steep channel dopant profile. As a result, In-SSR DTMOS depicts significant performance improvements in terms of driving current, dynamic threshold property, subthreshold swing and Gm, which are difficult to achieve with conventional BF_2-implanted DTMOS. In addition, contrary to conventional narrow-channel BF_2-implanted DTMOS that suffers from degraded dynamic threshold gain, In-SSR DTMOS maintains its high performance in narrow-channel devices, due to reduced channel dopant segregation into the isolation edge oxide. Finally, it is found for the first time that the hot-carrier resistance is improved for devices under DTMOS-mode operation, especially for In-SSR DTMOS. The new In-SSR DTMOS thus appears to be a very promising candidate for future ultralow-voltage ULSI applications.

Acknowledgment

The authors would also like to thank UMC TD/Logic Advanced Device Group for device fabrications and the anonymous reviews for their helpful comments.

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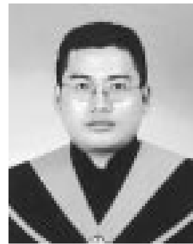
He joined the National Nano Device Laboratories (NDL), Hsinchu, as an Associate Researcher in July 1992, and became as a Researcher in 1996. He was engaged in developing the thin dielectrics preparations and cleaning processes. He is presently responsible for the deep submicron device integration at NDL.



Yao-Jen Lee was born in Kaoshiung, Taiwan, R.O.C., in 1976. He received the B.S. degree in physics from the National Chung-Hsing University, Taichung, Taiwan, in 1998, and the M.S. degree from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 2000.

His research interest is in the area of deep submicron devices.

Tiao-yuan Huang (S'78–M'80–SM'88–F'95) was born in Kaohsiung, Taiwan, R.O.C., on May 5, 1949. He received the B.S.E.E. and M.S.E.E. degrees from National Cheng Kung University, Tainan, Taiwan, in 1971 and 1973, respectively. After serving two years in the Taiwanese Navy, he joined Chung Shan Institute of Science and Technology, Lungtan, for two years, working on missile development. He received the Ph.D. degree in electrical engineering from the University of New Mexico, Albuquerque, in 1981.

He spent two years with the Semiconductor Process & Design Center, Texas Instruments. He then worked with several IC companies, including Xerox Palo Alto Research Center, Integrated Device Technology, Inc., and VLSI Technology, Inc. He has worked in various VLSI areas including memories (DRAM, SRAM, and nonvolatile memories), CMOS process/device technologies and device modeling/simulation, ASIC technologies, and thin-film transistors for LCD display. In 1995, he returned to Taiwan to become an Outstanding Scholar Chair Professor with National Chiao Tung University and Vice President in charge of R&D, National Nano Device Laboratories, National Science Council. He has published over 100 technical papers in international journals and conference proceedings. He holds over 20 issued U.S. patents.

Dr. Huang served on the technical committee of the IEEE International Electron Devices Meeting (IEDM) in 1991 and 1992. He also served on the program committee of the International Conference on Solid-State Devices and Materials (SSDM) from 1996 to 1998. He received the 1988 Semiconductor International's R&D Technology Achievement Award for his invention of the fully overlapped LDD transistors.