Study the impact of liner thickness on the 0.18 μm devices using low dielectric constant hydrogen silsesquioxane as the interlayer dielectric

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Abstract

The electrical performance of hydrogen silsesquioxane (HSQ) as the interlayer level dielectric (ILD) has been determined by using two-metal-layered test structures to study the impact of oxide liner thickness on the capacitance reduction. In comparison with SiO_2, HSQ test structures formed with SiO_2 cap and liner or with SiO_2 cap only, have 20−27% lower intraline capacitance while 6−16% reduction was observed for fluorosilicate glass (FSG) relative to SiO_2. It was found that the capacitance of SiO_2/HSQ ILDs did not vary with oxide liner thickness as expected. Similar effects were observed with via resistance measurement. Analysis of the structure shows that wide variation of SiO_2/HSQ/SiO_2 stack thickness after oxide Chemical Mechanical Polishing (CMP) step changed the expected contribution of liner thickness on the intraline and interlayer capacitance. This thickness variation also has a strong impact on landed/unlanded via resistance. Therefore, a good control of oxide CMP on the ILD stack is needed to reduce the thickness variation of the liner/HSQ/cap ILD stack which in turn will enhance process yields in the 0.18 μm devices. © 2000 Elsevier Science B.V. All rights reserved.

Keywords: Hydrogen silsesquioxane; HSQ; Low *k*; Liner thickness; Capacitance; Via resistance

1. Introduction

As the minimum geometry in integrated circuits (ICs) continues to shrink to the 0.18−0.25 μm range, the capacitance between metal lines increases dramatically and causes delay in signal propagation. Therefore, low-*k* dielectric materials are used in ultra large scale integrated (ULSI) devices to reduce the delay in line-to-line cross-talk, and hence increase the signal propagation speed [1]. Among the available low-*k* processes and materials, only spin-on hydrogen silsesquioxane (HSQ) and high-density plasma chemical vapor deposited (HDP-CVD) fluorosilicate glass (FSG) films have been successfully integrated in manufacturing processes for 0.18 μm technology [2,3]. HSQ processes (*k* value 2.9−3.5) have potential for better performance than FSG (*k* value 3.2−3.7) [4,5].

In addition to lower dielectric constant, HSQ has excellent gap filling and planarization capability [6]. When integrating HSQ in ILD applications, it is a common practice to use SiO_2 layers to form liner/HSQ/cap sandwich structures [6]. The oxide liner is used to raise ILD mechanical integrity and minimize

leakage current between adjacent metal lines. The cap oxide is to provide the protective top layer for HSQ and it, along with the oxide liner, also balances the overall stress from tensile to compressive. In addition, the oxide cap needs to be polished back by chemical mechanical polishing (CMP) to provide global planarization. Since SiO_2 (*k* value 3.9–4.1) has a higher dielectric constant than that of HSQ, the overall capacitance of the ILD depends on the combined properties of HSQ and SiO_2 layers. The interaction is more of a concern for devices with metal gaps smaller than 0.25 μm since the overall capacitance increases dramatically as the gap size decreases and the increase is dependent on the relative amount of HSQ to SiO_2 in the gap [7]. Therefore, metal/dielectric test structures with small geometries using HSQ with different thickness of SiO_2 liner were processed to explore the impact of liner thickness on overall capacitance and via chain resistance. A comparison of the capacitance among HSQ, SiO_2/HSQ, FSG, and SiO_2 ILD structures and the impact of these ILD schemes on the via resistance of landed and unlanded vias are reported in this study.

2. Experimental

Test structures with two layers of metal were processed for this study. The metal pattern layer is TiN/Ti/Al/TiN/Ti and the ILD layer is SiO_2/HSQ/SiO_2 sandwich structure. A 25–100-nm thick PECVD oxide was then deposited on top of metal patterns as the liner. Flowable Oxide FOx®-15 from Dow Corning Corporation was then spin-coated onto the wafers to produce the HSQ layer, which were next processed at 150, 200, and 350°C hot plates for 1 min each, and then cured at 400°C under an N_2 ambient for 1 h. Another 1.8 μm of PECVD oxide was deposited on top of the HSQ layer to form the liner/HSQ/cap sandwich structure and then CMP was performed on the ILD layer to enhance the global planarization. The deposited cap oxide thickness was fixed for all ILD test structures.

The second metal layer stack was then deposited and etched to form desired patterns for electrical testing. All the test structures were processed under the same conditions except for the liner deposition step. Since oxide liners were deposited at slightly different conditions, 500-nm thick of PECVD oxide films were deposited on the Si wafers and evaluated to assess the differences in wet/dry etch rate study, and dielectric constant. The wet etch rate was measured using 200:1(H_2O/HF) buffer HF solution. The dry etch rate was measured using a HDP etcher in a $CO/CH_2F_2/C_4H_8/C_2F_8/O_2/Ar$ environment. The dielectric constant was measured using a HP 4194 impedance analyzer at 1 MHz. The interline and intraline capacitance were measured between metal lines at the frequency of 100 kHz.

3. Results and discussion

The dielectric constant, wet etch rate, and dry etch rate of different oxide liners and HSQ were measured on 500 nm thick films as listed in Table 1. The data show that there exists slight difference in the dielectric constant, wet etch rate and dry etch rate for different liner films, which is due to the different deposition conditions. The wet etch rate of HSQ was observed to be 20 times larger than that of the oxide liners. However, the dry etch rate of HSQ is less than twice of that of oxide liners. Therefore, the wet etch rate and the dry etch rate of HSQ could be very different depending on the etch method and etch chemistry used during etching processes and the film composition.

Computer modeling shows that the intraline capacitance plays a more important role than interlayer capacitance on the interconnect RC delay for IC geometry smaller than 0.5 μm [8]. Therefore, the intraline capacitance for metal width/metal spacing of 0.23 μm/0.23 μm, 0.23 μm/0.46 μm, and 0.46 μm/0.23 μm were measured in this study. In Fig. 1, the X-SEM pictures of HSQ with 50 nm oxide liner are shown as the examples of test patterns with various metal widths and metal spacings. The intraline capacitance in metal comb structures for HSQ with different liner thicknesses is shown in Fig. 2. The data show that wider metal patterns have larger intraline capacitance than those of narrower metal patterns at the same metal spacing. This is due to the fact that wider metal pattern has a larger fringing effect on capacitance [9].

Table 2 shows the relative intraline capacitance in

Table 1
The dielectric constant, wet etch rate, and dry etch rate of different oxide liners and HSQ

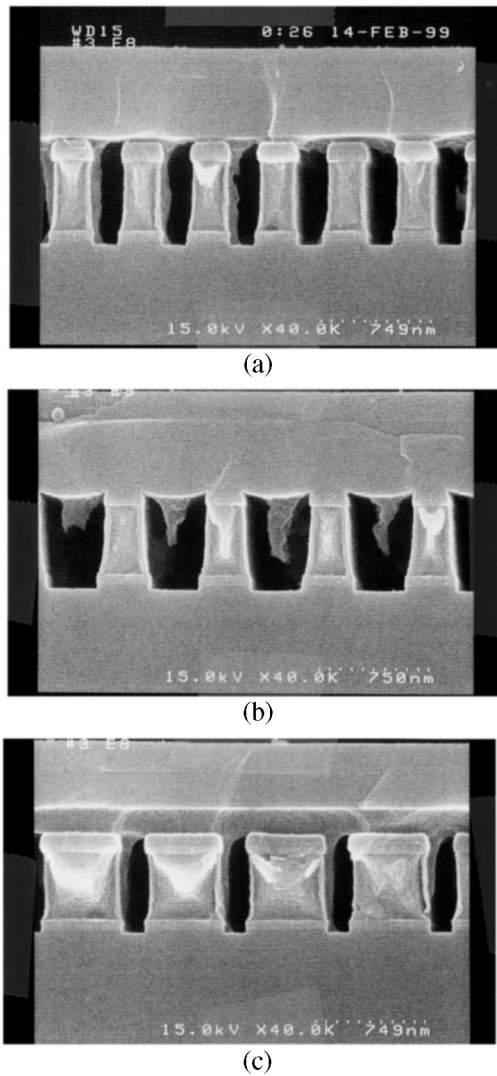| Dielectric films	Dielectric constant at 1 MHz	Wet etch rate (A°/min)	Dry etch rate (A°/min)
Use 1000 A° recipe	4.2	166	3795
Use 500 A° recipe	4.3	156	3894
Use 350 A° recipe	4.4	156	3630
Use 250 A° recipe	4.5	133	3573
HSQ (4000 A°)	2.9	> 3237	5145

(a)

(b)

(c)

Fig. 1. The cross-section SEM of pattern wafers of HSQ with 500 A°
liner at metal width/spacing of (a) 0.23 μm/0.23 μm (b) 0.23
μm/0.46 μm (c) 0.46 μm/0.23 μm.

metal comb structure for various ILD configurations.
The test structures of USG and FSG were processed at
similar targeted ILD thickness as $SiO_2/HSQ/SiO_2$
ILD stack within certain process variations. Combina-
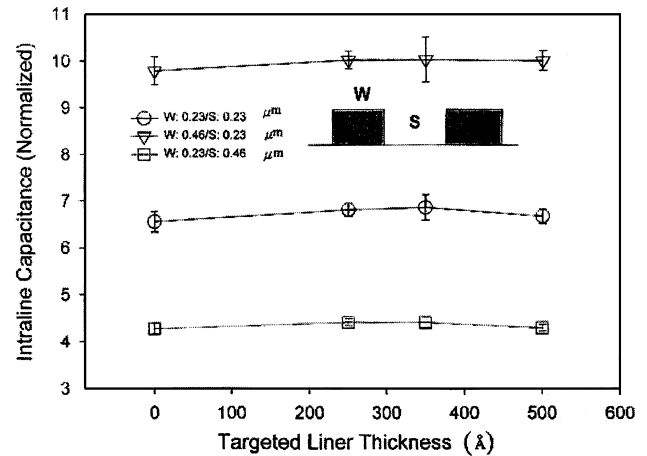tion of $SiO_2/HSQ/SiO_2$ ILD stacks can achieve

Fig. 2. The normalized intraline capacitance of HSQ with different
thickness of oxide liner.

20−25% reduction compared to SiO_2 alone while only
6−16% reduction was observed for fluorosilicate glass
(FSG) relative to SiO_2 [4]. Similar results have been
reported on 0.35 and 0.25 μm devices [10,11]. Even
further reduction can be achieved with HSQ alone, but
additional processing is required to insure adequate
electrical isolation between adjacent vias [12]. The HSQ
structure, even with oxide liner, has lowest intraline
capacitance when compared to USG and FSG.

The interlayer capacitance for various $SiO_2/HSQ/$
SiO_2 stacks is shown in Fig. 3. The data show that HSQ
with 100 nm oxide liner and with 25 nm oxide liners has
a lower interlayer capacitance than other liner cases.
Interlayer capacitance should be proportional to metal
separation (i.e. the ILD stack thickness between metal
layers), but the measured data are not consistent with
the targeted SiO_2 liner thickness. In Table 3, the data
from X-SEM measurement show that the trend of
actual metal separation differs from the expected sepa-
ration and is consistent with the capacitance results.
This variation in ILD stack thickness is caused by the
remaining cap oxide thickness after cap oxide CMP
step. Since it is difficult to use end point detection in
the oxide CMP step, time mode control was applied in
this study. However, the remaining thickness of ILD

Table 2

Intraline capacitance reduction on two-metal-layered structures for FSG and HSQ when compared with USG[a]

Different ILD materials	Capacitance reduction % (width/gap)		
	0.23 μm/0.23 μm	0.46 μm/0.23 μm	0.23 μm/0.46 μm
HDP USG	0	0	0
HDP FSG	10.1	16	6.7
HSQ (0 A° liner)	26.3	27.0	23.2
HSQ (250 A° liner)	23.3	24.2	20.7
HSQ (350 A° liner)	22.9	23.3	20.7
HSQ (500 A° liner)	25.0	25.4	22.8

[a] The oxide liner is deposited using SiH_4 and O_2 gas sources.

Table 3
Normalized ILD stack thickness between metal-1 and metal-2 for HSQ with different targeted liner thickness

Target liner thickness (A°)	0 A° liner	250 A° liner	350 A° liner	500 A° liner	1000 A° liner
ILD stack	1	1.143	0.978	0.818	1.331
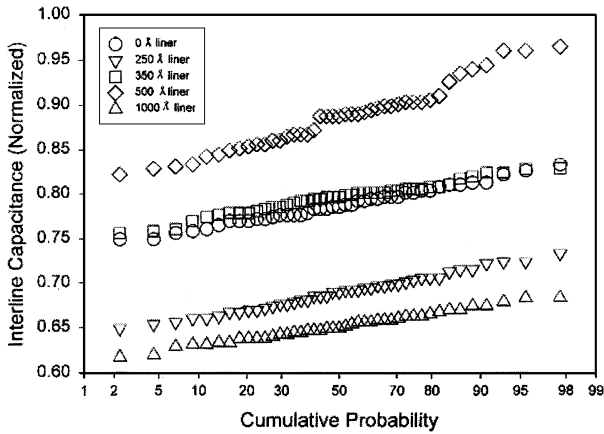
Fig. 3. The interlayer capacitance between metal 1 and metal 2 of HSQ with different liner thickness.

Fig. 5. The via resistance of 0.25 μm landed via for HSQ with ILD stack thickness.

stack under time mode control will vary due to changes in polish rate, pad conditions, and the pattern density [13,14].

Fig. 4 shows that the landed via resistance increases with decreasing via diameter, which is expected based on the via geometry. There is no significant correlation between landed via resistance and liner thickness. The correlation between landed via resistance and ILD thickness is shown in Fig. 5 It implies that the SiO_2/HSQ ILD stack thickness might impact the via resistance of landed via. With time control of the via etch, in regions of thinner ILD, the Ti + TiN may be etched away in the lower metal level. Since Ti + TiN have high resistance compared to Al, when removed,
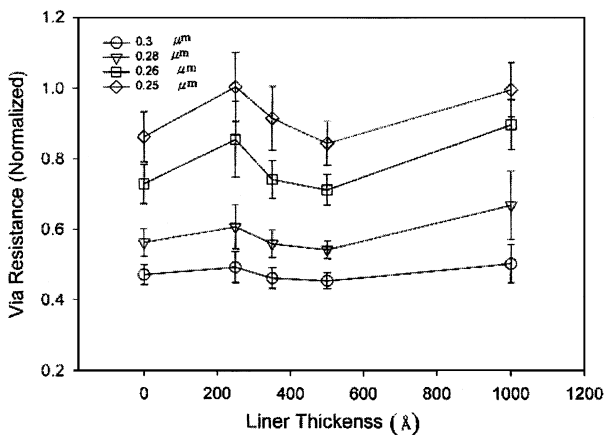
the via resistance can decrease. In addition, a lower aspect ratio is easier to fill for device with thinner ILD stack.

Fig. 6 shows the via resistance of 0.26 μm (the via size under 0.18 μm design rule) unlanded via with 0.04 μm misalignment. There is no significant correlation between liner thickness and measured unlanded via resistance except for the 50 nm liner case. It was observed that the unlanded via of HSQ with 50 nm oxide liner was over etched as shown in Fig. 7. The degree of via over etch is determined by the remaining thickness of ILD stack after the oxide CMP step, the etch rate of the via etch processes, and the via etch time [15]. For other degrees of misalignment in the 0.26 μm vias, the unlanded via resistance increases with

Fig. 4. The via resistance of various diameter landed via for HSQ with different liner thickness.

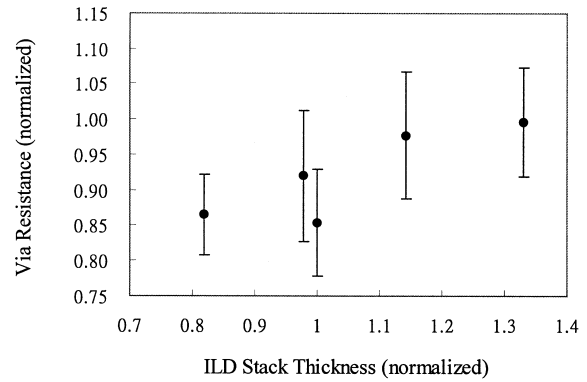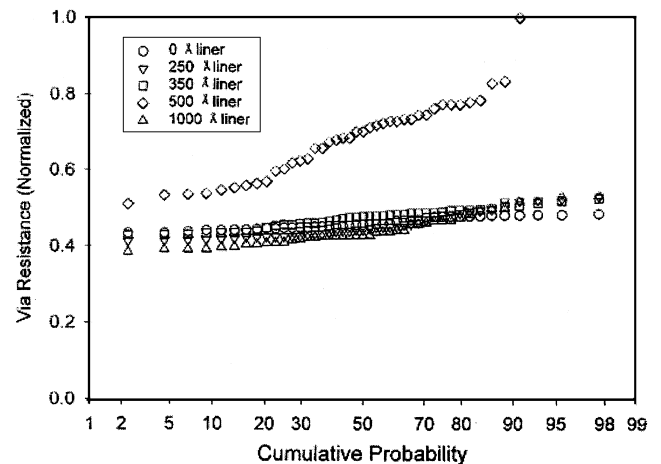Fig. 6. The via resistance of 0.26 μm unlanded via with 0.04 μm misalignment for HSQ with different liner thickness.
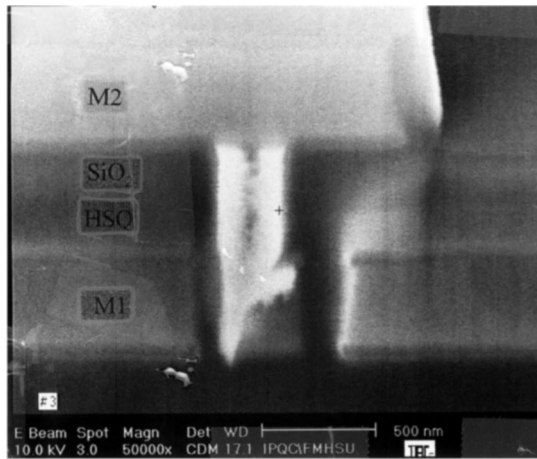
Fig. 7. The FIB picture of unlanded via with via over etch in HSQ.

decreasing the ILD stack thickness. In this study, due to the time mode control for the via etch and etch rate difference between oxide and HSQ, it is expected that via over etch for thinner ILD stack will lead to a higher aspect ratio of unlanded via, which causes void formation during W deposition. Therefore, a higher unlanded via resistance and a lower via yield were observed. In contrast, better thickness control in the oxide CMP step can prevent the over etch of unlanded via as shown in Fig. 8.

4. Conclusions

The intraline capacitance, interlayer capacitance, landed via resistance, and unlanded via resistance of $SiO_2/HSQ/SiO_2$ ILD sandwich structure with various liner thicknesses have been measured. Compared with SiO_2 alone, there is approximately 20–25% reduction in intraline capacitance for the $SiO_2/HSQ/SiO_2$ ILD stack while only 6–16% reduction was observed for fluorosilicate glass (FSG) relative to SiO_2. The data

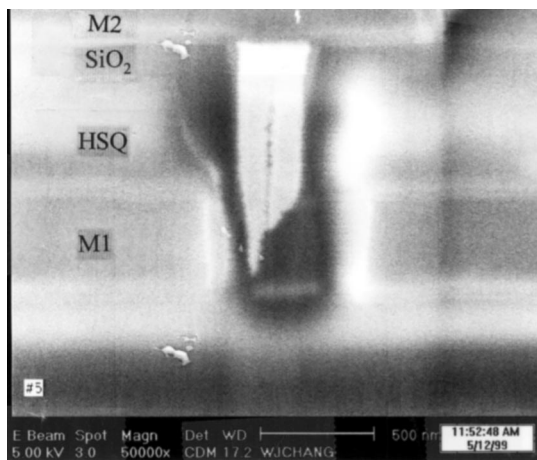show that the wide variation of $SiO_2/HSQ/SiO_2$ stack thickness, which is determined by the cap oxide CMP step, affects the expected contribution of the liner thickness on the intraline and interlayer capacitance. This thickness variation also has stronger impact on landed/unlanded via resistance than that of liner thickness. Therefore, minimizing ILD thickness variations and having tighter control in the oxide CMP step will help to maximize the performance of the HSQ in ILD applications for 0.18 μm devices.

Acknowledgements

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Fig. 8. The FIB picture of unlanded via without via over etch in HSQ.