Hot Carrier Reliability Improvement by Utilizing Phosphorus Transient Enhanced Diffusion for Input/Output Devices of Deep Submicron CMOS Technology

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***Abstract*—This letter presents a deep submicron CMOS process that takes advantage of phosphorus transient enhanced diffusion (TED) to improve the hot carrier reliability of 3.3 V input/output transistors. Arsenic/phosphorus LDD nMOSFETs with and without TED are fabricated. The TED effects on a LDD junction profile, device substrate current and transconductance degradation are evaluated. Substantial substrate current reduction and hot carrier lifetime improvement for the input/output devices are attained due to a more graded n^- LDD doping profile by taking advantage of phosphorus TED.**

***Index Terms*—Hot carriers, MOS devices, transient enhanced diffusion.**

I. INTRODUCTION

IN THE development of deep submicron CMOS technologies, the use of a super-steep retrograde channel, highly doped shallow source/drain extensions and pocket halo implants are necessitated to maintain good short channel characteristics and high current drive [1]. Rapid thermal anneal (RTA) prior to side-wall spacer formation is adopted to suppress detrimental transient enhanced diffusion (TED) effects on shallow junction formation [2], [3]. Hot carrier effects in these devices are relieved by using reduced supply voltage ($\leq$2.0 V). In some applications, CMOS technologies are required to offer input/output (I/O) interface compatible with higher operating voltages, for example, 3.3 V. To meet this requirement, dual gate-oxide process is employed, i.e., a thinner gate oxide for core devices and a thicker gate oxide for I/O devices. Since I/O devices usually share the same substrate architecture as in core devices to minimize processing cost, hot carrier effects become a major concern in the design of I/O devices.

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TABLE I
MAJOR STEPS IN TWO CMOS PROCESS FLOWS

Process A	Process B
Poly gate definition	Poly gate definition
S/D extension and halo implants for core device and I/O PMOS	S/D extension and halo implants for core device and I/O PMOS
As/P nLDD implants for I/O NMOS	***RTA***
RTA	***As/P nLDD implants for I/O NMOS***
Nitride spacer deposition	Nitride spacer deposition
Source/Drain Formation	Source/Drain Formation

To achieve better performance and hot carrier reliability, a hybrid arsenic/phosphorus (As/P) LDD junction is used in high voltage I/O transistors [4]. The phosphorus in hybrid implant can help grading the n^- LDD doping profile, thus reducing the peak electric field in the channel. To further increase the hot carrier resistance of I/O devices, we propose to take advantage of TED of phosphorus [5], [6] to yield a more graded n^- LDD doping profile. In this work, As/P LDD n^- MOSFET's with and without TED phosphorus are fabricated. Hot carrier effects in these devices are compared. The influence of phosphorus TED on the n^- junction profile, substrate current and device performance degradation is investigated.

II. EXPERIMENT

Two process sequences for a deep submicron dual gate-oxide CMOS technology are shown in Table I. In process A, RTA is applied after S/D extension and halo implants for core devices and the As/P LDD implant for I/O devices. In process B, the sequence of the As/P implant and RTA is reversed. All other conditions are the same. In process B, I/O devices can take advantage of phosphorus TED during subsequent nitride spacer deposition while core devices still have the same fabrication procedure as in process A. The deposition temperature and time of nitride spacer are 750 °C and 2 h, respectively. Three kinds of I/O devices are fabricated. Device A is made with the process flow A, device B is with the process flow B, and device C is the same

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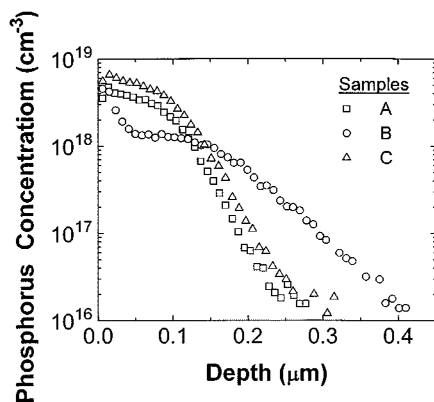

Fig. 1. Phosphorus doping profiles measured by SIMS. The x-axis denotes the depth in substrate.

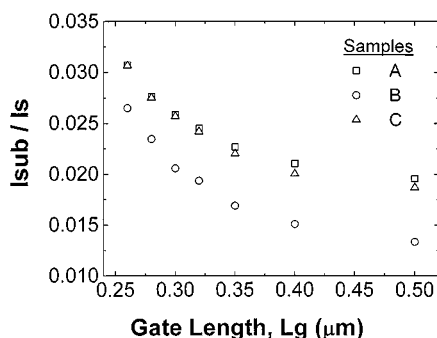

Fig. 2. Ratio of maximum substrate current to source current plotted against gate length. Vds = 3.6 V.

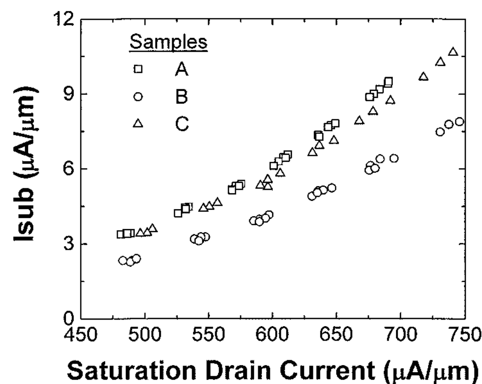

Fig. 3. Substrate current plotted against drain saturation current. The drain saturation current is measured at Vds = 3.3 V and Vgs = 3.3 V.

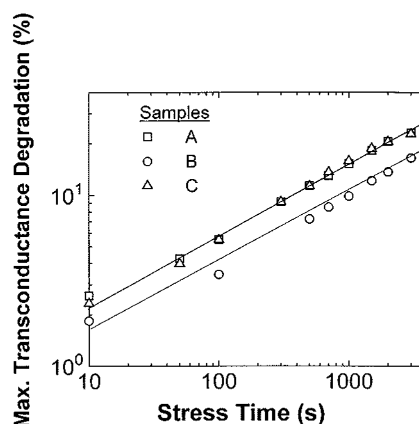

Fig. 4. Maximum transconductance degradation versus stress time. A power-law degradation rate is shown.

as device A except that the phosphorus dosage is increased by 20%. All the sample devices have a gate oxide thickness of 70 Å. The gate length is from 0.26 μm to 0.5 μm. The supply voltage for the I/O devices is 3.3 V.

III. Results and Discussions

The SIMS results for the phosphorus doping profile in the three sample devices are drawn in Fig. 1. The x-axis in the figure denotes the depth in substrate. Device B apparently has a more graded phosphorus doping profile due to TED. Adding phosphorus dose in the hybrid implant (device C) simply increases the doping level, but does not change the slope of the doping profile. The phosphorus TED effect on maximum subtrate current (Isub) is examined in Fig. 2. The substrate current in the figure in normalized to the source current. The measurement drain bias is 3.6 V (10% above the supply voltage for over-stress) and the gate bias is about one half of the drain bias. Devices A and C (without TED) have nearly the same substrate current while device B (with TED) has a much smaller substrate current. The subtrate current reduction is about 30% at $Lg = 0.35$ μm. The remarkable reduction in device B results from a more graded LDD junction, as shown in Fig. 1 and indicates that phosphorus TED can be utilized as a more effective way to improve hot carrier resistance as compared to other methods such as a straight phosphorus dose change. We also investigate the current driving capability of the three devices. It is found that drain saturation current (Idsat) of device B is slightly improved over device A and the series resistance in LDD region is not significantly affected since the doping concentration of hybrid LDD is dominant by arsenic implant. The maximum Isub versus the drain saturation current (Idsat) is plotted in Fig. 3 for different channel lengths. The Idsat is measured at $Vds = 3.3$ V and $Vgs = 3.3$ V. At the same driving current, device B always exhibits a smallest Isub. It should be mentioned that phosphorus TED has a minimal adverse effect on off-state drain leakage current. For example, for 0.35 μm gate length, the drain leakage current at $Vgs = 0$ V and $Vds = 3.3$ V is 0.22 pA/μm in device A, 0.25 pA/μm in device B and 0.30 pA/μm in device C. Threshold voltage roll-off degradation due to phosphorus TED is insignificant down to gate length of 0.3 μm. The result is not shown here.

The stress-time dependence of hot carrier induced maximum transconductance (Gm, max) degradation is shown in Fig. 4. The devices have a gate length of 0.35 μm. A maximum Isub stress at $Vds = 4.5$ V and $Vgs = 2.1$ V is used for accelerated degradation. All the devices follow a power-law degradation rate. The power factor is about 0.4, which is in agreement with published result [7]. From Fig. 4, we conclude that a significant improvement in the 10% Gm, max degradation lifetime by three times can be achieved owing to the phosphorus TED effect.

IV. Conclusion

A CMOS process flow to take advantage of phosphorus TED in forming a more graded LDD junction in I/O devices is proposed. By using this approach, substantial improvement in hot carrier effects has been demonstrated. This process can effectively widen the performance-reliability window for I/O device design while maintaining suitability for core device development.

Acknowledgment

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