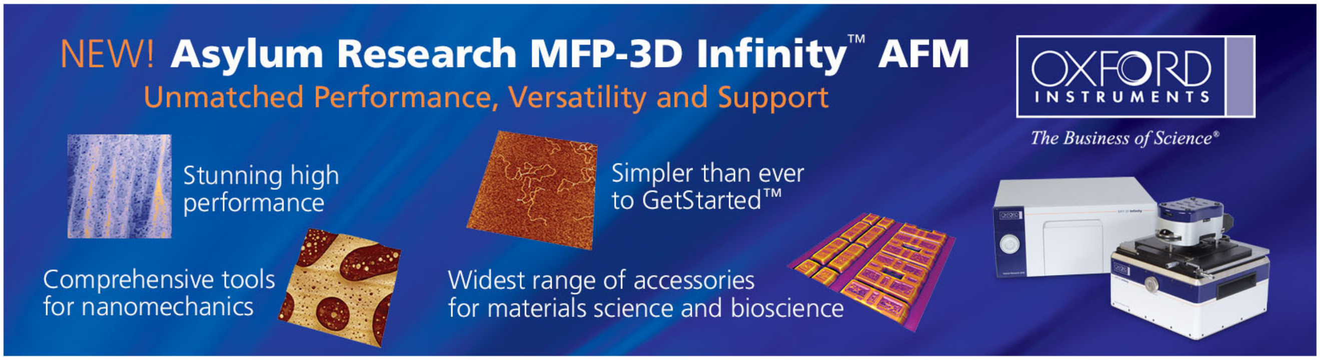
AIP Applied Physics Letters

Thermal stability of Cu/Ta/GaAs multilayers

Chang-You Chen, Li Chang, Edward Y. Chang, Szu-Houng Chen, and Der-Fu Chang

Citation: Applied Physics Letters **77**, 3367 (2000); doi: 10.1063/1.1328094
View online: http://dx.doi.org/10.1063/1.1328094
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/77/21?ver=pdfcov
Published by the AIP Publishing



APPLIED PHYSICS LETTERS VOLUME 77, NUMBER 21 20 NOVEMBER 2000

Thermal stability of Cu/Ta/GaAs multilayers

Chang-You Chen, Li Chang,[a] Edward Y. Chang, Szu-Houng Chen, and Der-Fu Chang
Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan 300, Republic of China

(Received 3 July 2000; accepted for publication 2 October 2000)

Copper metallization for GaAs was evaluated by using Cu/Ta/GaAs multilayers for its thermal stability. A thin Ta layer of 40 nm was sputtered on the GaAs substrate as the diffusion barrier before copper film metallization. As judged from sheet resistance, x-ray diffraction, Auger electron spectroscopy and transmission electron microscopy, the Cu/Ta films with GaAs were very stable up to 500 °C without migration into GaAs. After 550 °C annealing, the interfacial mixing of Ta with GaAs substrate occurred, resulting in the formation of $TaAs_2$. At 600 °C annealing, the reaction GaAs with Ta and Cu formed TaAs, $TaAs_2$, and Cu_3Ga, resulting from Cu migration and interfacial instability. © *2000 American Institute of Physics.* [S0003-6951(00)03047-3]

Copper metallization has become a hot topic in the silicon integrated circuits technology ever since IBM announced its success in silicon very large scale integration process.[1–3] Even though the use of copper as metallization metal has become very popular in Si devices, the use of copper as metallization metal for GaAs devices has not been reported yet. Traditionally, GaAs field-effect transistors (FETs) and monolithic microwave integrated circuits (MMICs) use Ti as adhesion layer, and Au as the metallization metal for transmission lines and ground plane metallization. The gold used in transmission lines and ground plane is usually plated to a thickness of 2–3 μm and more than 10 μm, respectively. The use of copper as the metallization metal for transmission lines and ground plane metallization has the following advantages over gold: lower resistivity, higher thermal conductivity, and lower cost. Low thermal conductivity and fragility of substrate have always been problems in GaAs devices, especially in GaAs power FETs which are usually required to dissipate much heat. To increase the heat dissipation, the wafer of the power GaAs FETs is usually thinned to 2–5 mils thick, which makes the substrate very fragile. Therefore, the use of thicker copper layer as a metallization metal for backside metallization for GaAs FETs and MMICs to provide higher mechanical strength and better thermal sink is a very attractive task. On the other hand, if Au is replaced with Cu for frontside transmission lines, the electrical conductivity can be improved to increase the speed.

It is well known that copper diffuses very fast into Si when it is in contact with Si substrate without any diffusion barrier.[4–6] As in the silicon case, copper also diffuses very fast into GaAs when deposited on the GaAs substrate without any diffusion barrier.[7] Since copper is a deep acceptor for GaAs, this causes degradation of electrical properties in the GaAs devices. Ta is currently an effective diffusion barrier for Cu metallization in Si technology, because it forms no compound with copper. On the other hand, Ta has good adhesion with GaAs and three times higher thermal conductivity than Ti.[8] Therefore, using Ta as diffusion barrier should be able to ensure the success of Cu metallization for GaAs. In this letter, the thermal stability of Cu/Ta/GaAs in blanket film structure was investigated.

Before metal film deposition, the GaAs substrates were cleaned with boiling acetone and isopropyl alcohol each for 5 min and dipped with $HF:H_2O_2:H_2O$ (1:2:20) for 20 s and $HCl:H_2O$ (1:4) for 1 min. The films were deposited by sputtering in a multitarget dc magnetron sputtering system. A tantalum film of 40 nm thickness was first sputtered onto the 3 in. (100) GaAs substrate, then a 100 nm Cu film and a 10 nm tantalum nitride films were subsequently sputtered onto this without breaking vaccum. The tantalum nitride film which served as a protective layer to prevent oxidation of the copper layer was deposited by reactive sputtering of Ta in the N_2/Ar mixture with 8% N_2 and 92% Ar. The base pressure was 2.6×10^{-5} Pa before sputtering, and the total sputtering gas pressure was 0.8 Pa during deposition of the films. The samples were annealed for 30 min at temperatures ranging from 400 to 600 °C in argon ambient. Sheet resistances of the samples were measured by a four-point probe. X-ray diffraction (XRD), Auger electron spectroscopy (AES), and cross-sectional transmission electron microscopy (TEM) were used for microstructural characterization.

Figure 1 shows the sheet resistances of the samples as-

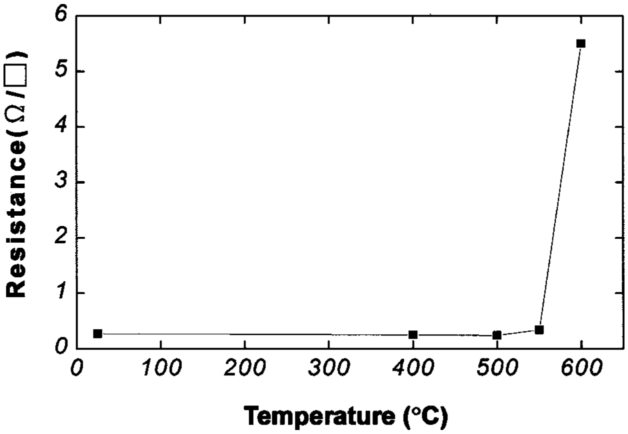


FIG. 1. Sheet resistance of the samples as-deposited and after annealing at various temperatures.

---

[a] To whom correspondence should be addressed; electronic mail: lichang@cc.nctu.edu.tw

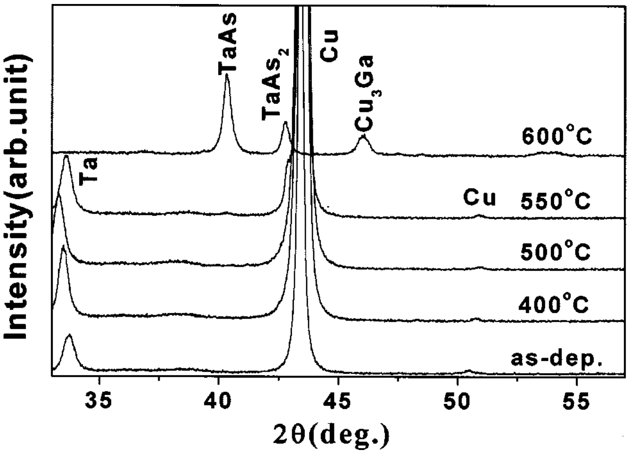


FIG. 2. XRD patterns of the samples as-deposited and after annealing at various temperatures.

deposited and after 400–600 °C annealing. The sheet resistance of the TaN_x/Cu/Ta/GaAs film structure initially drops a little after 400 and 500 °C annealing, which is apparently caused by grain growth and a decrease in defect density in the Cu and Ta films. The sheet resistance increased slightly upon annealing at 550 °C, which implies diffusion and/or reaction occurred. After 600 °C annealing, the sheet resistance drastically increased, suggesting that a significant diffusion and reaction had occurred between the layers. Figure 2 shows the XRD results. From the XRD data, it is clear that the peaks of Ta and Cu remain unchanged after 500 °C annealing, suggesting that Cu/Ta/GaAs interface is still quite stable up to 500 °C. After 550 °C annealing, it is found that the additional peaks can be identified as $TaAs_2$. Formation of $TaAs_2$ implies that reactions between the substrate and the Ta layer can take place at 550 °C. This is consistent with the increase of sheet resistance at 550 °C. After 600 °C annealing, the peaks of Cu and Ta disappeared, instead peaks identified to be phases of TaAs and Cu_3Ga (hexagonal structure with lattice parameters of $a = 0.2600$ and $c = 0.4229$ nm)[9] are seen, indicating that a significant diffusion and reaction had occurred among the layers. The $TaAs_2$ phase is still present with the peak intensity decreased. The decomposition of $TaAs_2$ into As and TaAs below 750 °C has been previously reported by Saini.[10] This result explains the drastically increased sheet resistance after 600 °C annealing. Additional evidence showing the stability to 500 °C has been obtained from AES depth profiles in Fig. 3. As can be seen from this figure, the distribution of the elements in the deposited films remain almost unchanged after 500 °C annealing. Figure 4 shows cross-sectional TEM micrographs of the TaN_x/Cu/Ta/GaAs structure. In Fig. 4(a), it shows that grain growth of the Cu and Ta occurred after 500 °C annealing, and there is no evidence of intermixing of Cu and the Ta barrier layer with the GaAs substrate. The microstructure of the sample annealed at 600 °C is shown in Fig. 4(b). The regions in dark contrast are identified as TaAs, and those in

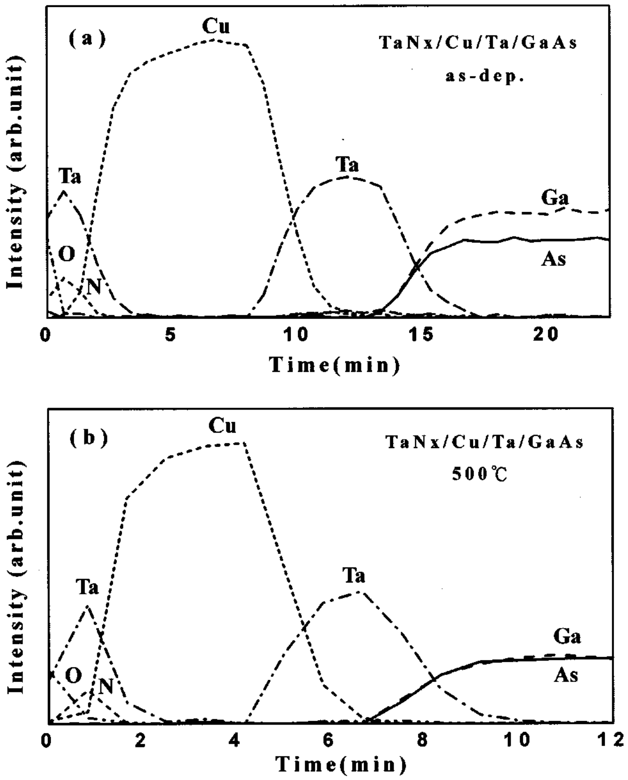


FIG. 3. Auger depth profiles of the samples (a) as-deposited and (b) after 500 °C annealing.

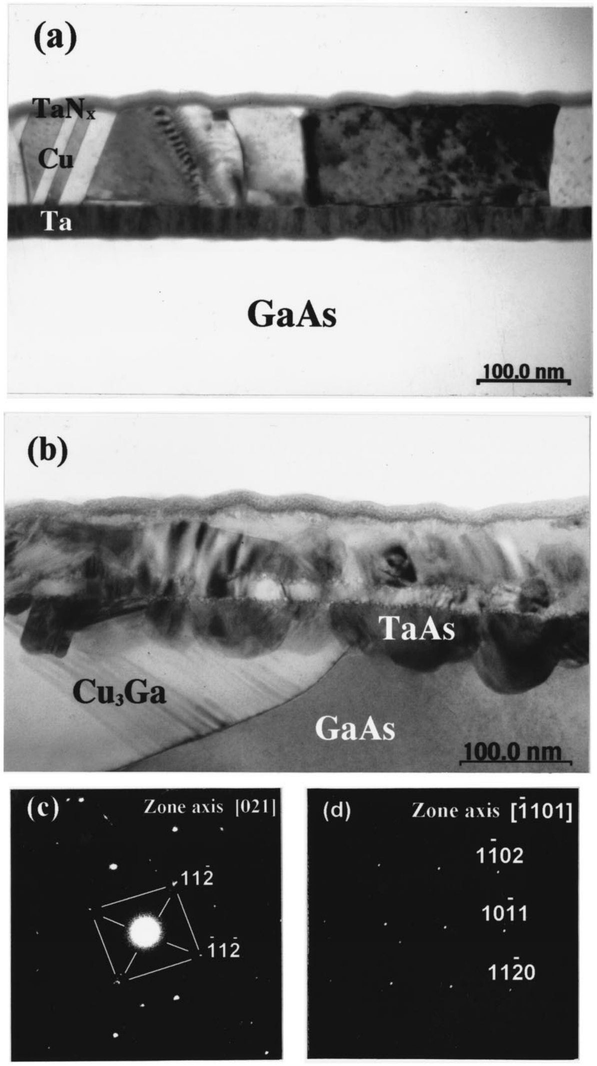


FIG. 4. Cross-sectional TEM micrographs (a) after 500 °C annealing, (b) after 600 °C annealing, (c) TaAs electron diffraction pattern, and (d) Cu_3Ga electron diffraction pattern.

white are Cu_3Ga by selected area electron diffraction pattern [Figs. 4(c) and 4(b)] and x-ray energy dispersive spectroscopy (EDS). The observation of Cu_3Ga as a large grain in the substrate and small grains close to the surface clearly demonstrates the severe diffusion of Cu and Ga at high temperature. The chemical analysis of EDS shows that the Cu_3Ga phase also contains a few percent of As. We are not able to identify the location of $TaAs_2$ as their size is too small to be seen in the scale of the image. However, it is speculated that they might locate at the Ta/GaAs interface. From the above results, it is suggested that Cu migration into GaAs substrate with Ta/GaAs interfacial reaction results in failure of the barrier at 600 °C.

Copper metallization on GaAs with Ta as the diffusion barrier layer has been shown to be able to be stable up to 500 °C. After 550 °C annealing, however, the interfacial mixing of Ta with GaAs substrate occurred, resulting in the formation of $TaAs_2$ phase, whereas the released Ga may be dissolved in Cu as the Ga solubility in Cu can be up to 22.2% according to Cu–Ga phase diagram.[11] After 600 °C annealing, Ta strongly reacted with GaAs to form TaAs, while Cu penetrated into GaAs to form Cu_3Ga. Also, $TaAs_2$ may gradually decompose to TaAs as TaAs could be more stable than $TaAs_2$ at high temperature. The surplus As might then go into Cu_3Ga. While further work is necessary to examine the details of the interdiffusion and reactions of the layers, the stability up to 500 °C should be good enough for the later stages of GaAs device processes. To verify the effectiveness of Cu metallization, we have applied the Cu/Ta layers to the backside metallization on GaAs MESFETs, it shows comparable performance with conventional Au/Ti layers.[12] It is believed that Cu can also be successfully applied to the frontside GaAs devices metallization with the proper modification of the current processes.

The work was sponsored jointly by the Ministry of Education and the National Science Council, Republic of China, under Contract No. 89-E-FA06-2-4. The authors would like to thank Professor Fu-Rong Chen and Professor Ji-Jung Kai of National Tsing Hua University for their help on TEM observations.

[1] K. Holloway and P. M. Fryer, Appl. Phys. Lett. **57**, 1736 (1990).

[2] K. Holloway, P. M. Fryer, C. Cabral, Jr., J. M. E. Harper, P. J. Bailey, and K. H. Kelleher, J. Appl. Phys. **71**, 5433 (1992).

[3] D. S. Yoon, H. K. Baik, and S. M. Lee, J. Appl. Phys. **83**, 8074 (1998).

[4] E. R. Weber, Appl. Phys. A: Solids Surf. **30**, 1 (1983).

[5] A. Cros, M. O. Aboelfotoh, and K. N. Tu, J. Appl. Phys. **67**, 3328 (1990).

[6] C. A. Chang, J. Appl. Phys. **67**, 566 (1990).

[7] P. H. Wohlbier, *Diffusion and Defect Data* (Trans Tech, OH, 1975), Vol. 10, pp. 89–91.

[8] C. Kittel, *Introduction to Solid State Physics*, 7th ed. (Wiley, New York, 1996), pp. 126 and 160.

[9] D. A. Mirzayev, V. M. Schastilivtsev, S. Y. E. Karzunov, T. R. Shron, and V. G. Ulynov, Phys. Met. Metallogr. **59**, 138 (1985).

[10] G. S. Saini, L. D. Calvert, and J. B. Taylor, Can. J. Chem. **42**, 630 (1964).

[11] T. B. Massalski and J. L. Murray, *Binary Alloy Phase Diagrams* (American Society for Metals, Metals, Park, OH, 1986), p. 1411.

[12] C. Y. Chen, E. Y. Chang, L. Chang, and S. H. Chen, Electron. Lett. **36**, 1317 (2000).