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Citation: *Applied Physics Letters* **77**, 3027 (2000); doi: 10.1063/1.1323735

View online: <http://dx.doi.org/10.1063/1.1323735>

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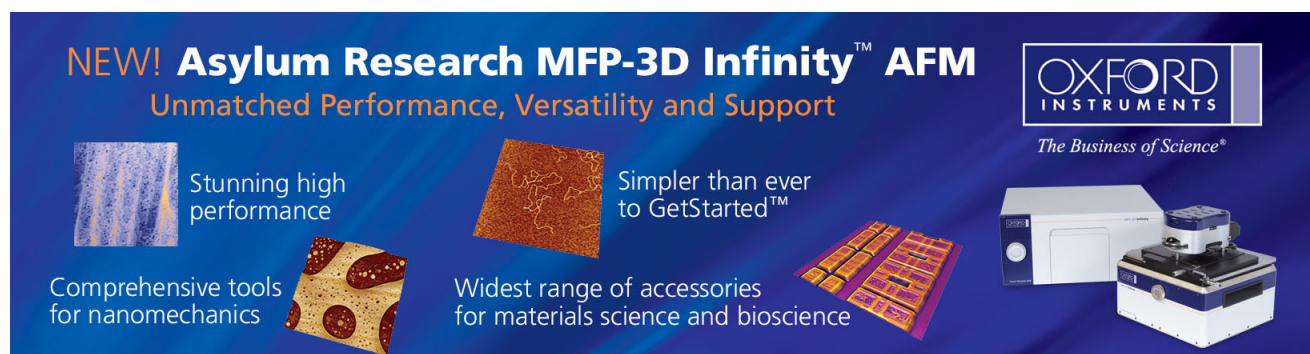
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Carrier distribution and relaxation-induced defects of InAs/GaAs quantum dots

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(Received 2 June 2000; accepted for publication 6 September 2000)

The carrier distribution and defects have been investigated in InAs/GaAs quantum dots by cross-sectional transmission electron microscopy (XTEM), capacitance–voltage, and deep level transient spectroscopy. Carrier confinement is found for 1.1- and 2.3-monolayer-(ML)-thick InAs samples. For 2.3 ML sample, XTEM images show the presence of defect-free self-assembled quantum dots. With further increase of the InAs thickness to 3.4 ML, significant carrier depletion caused by the relaxation is observed. In contrast to 1.1 and 2.3 ML samples in which no traps are detected, two broad traps and three discrete traps at 0.54, 0.40, and 0.34 eV are observed in 3.4 ML sample. The traps at 0.54 and 0.34 eV are found to be similar to the traps observed in relaxed $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ single quantum well structures. By comparing with the XTEM images, the trap at 0.54 eV is identified to be the relaxation-induced dislocation trap in the GaAs layer. © 2000 American Institute of Physics. [S0003-6951(00)02245-2]

The In(Ga)As/GaAs self-assembled quantum dots (QDs) have attracted significant interest both from the point of view of fundamental physics and for technological applications.^{1–4} The QDs were obtained by the so-called Stranski–Krastanov growth mode.⁵ The initial growth stage of the In(Ga)As/GaAs heterostructure has been studied by many workers.^{6–8} For instance, it has been reported that when InAs coverage increases to about 1.75 monolayer (ML), InAs strained film will be partially relieved and the growth mode changes from two-dimensional (2D) to three-dimensional (3D).⁷ The 2D to 3D transition during the initial stage of growth will not introduce any misfit dislocation.^{7,9,10} But as the InAs coverage increases to about 3 ML, island coalescence and defect incorporation will occur.^{7,11} Although the QDs structural and optical properties have been studied by atomic force microscopy,⁷ transmission electron microscopy (TEM),^{10,11} and photoluminescence (PL),¹² there has been no report on the detailed properties of the relaxation-induced defects. Investigation into this topic is necessary in order to understand the onset of relaxation and defect formation. In addition, this work is part of an ongoing investigation of the strain relaxation in $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ quantum wells.^{13,14}

The samples, with ultrathin InAs layer sandwiched by 0.3- μm -thick n -type GaAs layers, were grown on n^+ -GaAs (100) substrates by Varian Gen II molecular beam epitaxy. The thickness of the InAs layer was varied from 1.1, 2.3 to 3.4 ML. The InAs layer was undoped and the total 0.6- μm -thick GaAs layers were Si doped with a concentration of $6 \times 10^{16} \text{ cm}^{-3}$ to allow the depletion edge to sweep across InAs layer under reverse bias. The whole structure was grown at 550 °C without interruption, with an As_4 beam equivalent pressure of 1.2×10^{-5} Torr. The growth rates for GaAs and InAs were 0.98 and 0.23 ML/s, respectively. The growth was monitored by reflection high-energy electron diffraction (RHEED) and the QDs nucleation was observed for the 2.3 and 3.4 ML samples via the onset of a spotty RHEED

pattern. Schottky diodes were fabricated by evaporating Al on samples with a dot diameter of 1500 μm .

Figure 1 shows the room-temperature capacitance–voltage (C – V) data of the studied samples and their corresponding apparent carrier concentrations. The measuring frequencies were about 10^5 Hz. Carrier-confinement peaks with intensities about 8×10^{16} and $1.6 \times 10^{17} \text{ cm}^{-3}$ were observed, respectively, for 1.1 and 2.3 ML samples. When temperature was lowered, the peak intensities increased and widths narrowed, suggesting quantum confinement. Self-consistent simulation of C – V profile by Moon *et al.*¹⁵ shows that the broad C – V peak at high temperatures is attributed to the Debye averaging process between 2D and 3D electrons. As temperature is decreased, the 3D electron contribution becomes negligible and the apparent carrier distribution is mainly determined by a change of the position expectation value of 2D electrons under the sweeping C – V measurement. The small width of the C – V peak is the result of a very small change of the position expectation value of 2D electrons. On the other hand, significant carrier depletion far beyond the InAs layer was observed for 3.4 ML sample. This

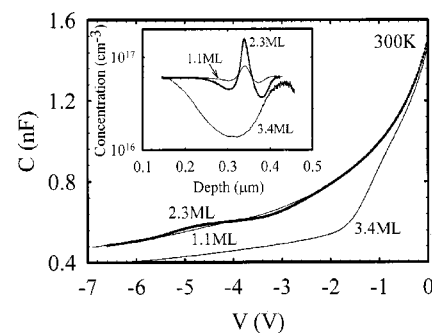


FIG. 1. Room temperature C – V data and the corresponding apparent carrier concentration for InAs/GaAs samples with InAs layer thickness of 1.1, 2.3, and 3.4 ML. The measuring frequencies were 10^5 Hz.

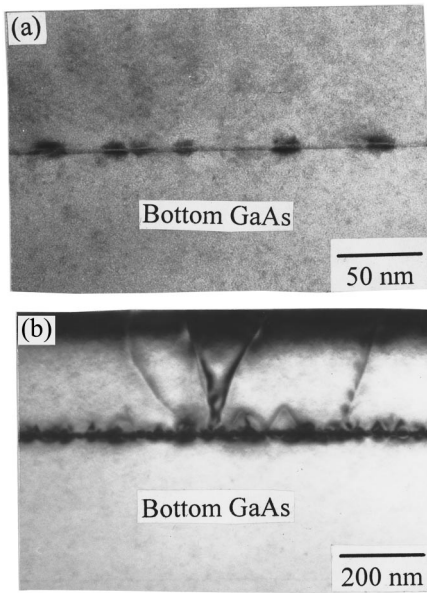


FIG. 2. The XTEM images for InAs/GaAs samples with InAs thickness of (a) 2.3 and (b) 3.4 ML.

carrier depletion is attributed to strain relaxation when the InAs thickness increases beyond its critical thickness. This critical thickness is consistent with the previously reported value of 3 ML for island coalescence and defect incorporation.^{7,11} Similar carrier depletion has been observed in $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ quantum well when the $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ thickness is beyond its critical thickness.¹⁴

Figures 2(a) and 2(b) show the cross-sectional TEM (XTEM) images of 2.3 and 3.4 ML samples, respectively. Quantum dots were clearly observed in the InAs layer for 2.3 ML sample. No defects (dislocations or stacking faults) either in the GaAs layers or in the InAs layer were observed. This indicates that during the initial 3D growth, self-assembled dots were formed coherently.^{7,9,10} On the other hand, for 3.4 ML sample, the XTEM image in Fig. 2(b) shows the presence of threading dislocations and stacking faults in the GaAs cap layer. It is also noted that misfit dislocations and cross-hatched stacking faults appear near the QDs boundaries. This result indicates that islands coalescence boundaries are favorable sites for dislocation nucleation.¹⁶ In contrast, the GaAs bottom layer is dislocation-free.

To further study their defects, all samples were measured by deep-level transient spectroscopy (DLTS) using a gain-phase analyzer HP4194A under dark condition. The filling pulse was set at 2 s and the measuring frequency was 10^5 Hz. While no traps beyond the detection limit were observed for 1.1 and 2.3 ML samples, several prominent traps were observed in 3.4 ML sample as shown in Fig. 3. In order to resolve traps from different depths, different bias voltage and filling pulse height were used: a small step voltage of -0.5 V was superimposed upon a direct current bias from 0, -0.5 , -1 , -1.5 , -2 , -2.5 , -3 , -3.5 to -4 V. From Fig. 3, three discrete traps E1, E2, and E5 and two broad traps E3 and E4 can be seen. They are (1) E1 trap, observed at ~ 300 K in Figs. 3(a)–3(b); (2) E2 trap, observed at ~ 275 K in Figs. 3(c)–3(d); (3) E3 trap, observed around 135 K in Fig. 3(e); (4) E4 trap, observed in Figs. 3(f)–3(g); and (5) E5

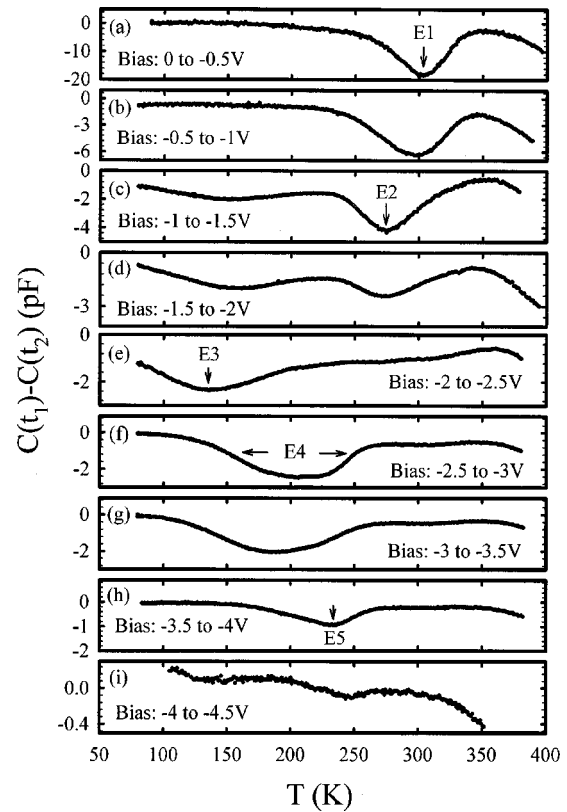


FIG. 3. The DLTS spectra for InAs/GaAs sample with InAs thickness of 3.4 ML. The measuring frequency is 10^5 Hz and $t_2/t_1 = 1.53$ s/0.153 s.

trap, observed at ~ 235 K in Fig. 3(h). The corresponding Arrhenius plots of the discrete traps E1, E2, and E5 are shown in Fig. 4. The activation energies (cross sections) were determined to be 0.54 eV (6.20×10^{-17} cm²), 0.40 eV (2.19×10^{-18} cm²), and 0.34 eV (2.48×10^{-18} cm²) for E1, E2, and E5 traps, respectively. The E3 trap appears as a broad continuum of states in the temperature range of 80–200 K, implying the presence of a defect band within the band gap. We speculate that this band is due to structural defects rather than point defects. Similar signals like E3 trap were observed in Figs. 3(c)–3(d) from 80 to 200 K. As for the broad E4 trap, it may consist of E5 trap judging from their closeness in temperature. Due to their broadness, no reliable activation energies could be obtained for E3 and E4

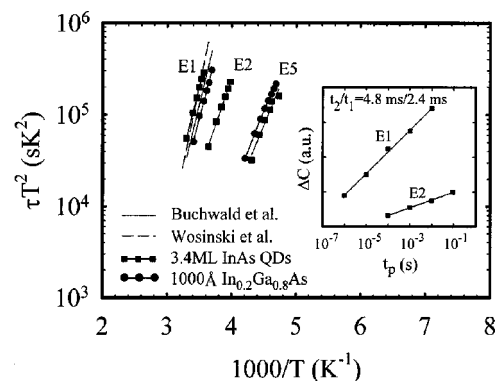


FIG. 4. The Arrhenius plot of traps E1, E2, and E5. Other works are included for comparison, including the trap observed in $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ single quantum well with 1000-Å-thick InGaAs and traps from Refs. 19 and 20. The inset shows the DLTS peak amplitudes of E1 and E2 traps vs filling-pulse duration time.

traps. The origin of E3 and E4 traps is not clear.

We believe that all the traps detected in 3.4 ML sample are due to relaxation-induced defects rather than electron emission from the QDs as previously observed in InAs/GaAs¹⁷ and InP/In_{0.5}Ga_{0.5}P¹⁸ materials. The photoluminescence emissions (not shown here) at 10 K related to the QDs were at 1.10 and 1.13 eV for 2.3 and 3.4 ML samples, respectively. Due to such small difference of 30 meV, any carrier emission from the QD states in 3.4 ML sample is likely to be observed in 2.3 ML sample. Since no DLTS signals were observed in 2.3 ML sample which contains QDs, we exclude the possibility that the trapping signals observed in 3.4 ML sample are the result of electron emission from the QDs. We speculate the reason why no electron emission from the QDs was observed was probably due to that the maximum measurable emission rate in our DLTS system is limited to ~ 10 s⁻¹.

In the E1 trap, the DLTS signals mainly come from the region close to the top of the GaAs cap layer. Comparing with the XTEM images, we assign this E1 trap to be the threading dislocation trap. We previously observed a similar trap at 0.53 eV ($\sigma = 1.1 \times 10^{-16}$ cm²) in relaxed In_{0.2}Ga_{0.8}As/GaAs single quantum well, as shown by the solid circles in Fig. 4. This result suggests that E1 trap is independent of In composition and is the relaxation-induced dislocation trap in the GaAs bulk layer. A similar trap at 0.58 eV has also been observed by Buchwald *et al.*¹⁹ in relaxed In_{0.083}Ga_{0.917}As/GaAs single heterojunction sample, further supporting this argument. Wosinski²⁰ also observed a similar trap (ED1) at 0.68 eV in plastic deformed bulk GaAs. Although there is a slight difference in the activation energy, this trap is close to E1 trap in the Arrhenius plot in Fig. 4. Moreover, the DLTS peak amplitude of E1 trap was found to have a logarithmic dependence on the duration time of filling pulse in the range of 10^{-6} – 10^{-2} s, as shown in the inset of Fig. 4. This logarithmic dependence is characteristic of dislocation-related traps and is attributed to the Coulombic repulsion of the carriers captured at the traps along the linearly arrayed dislocation lines.²⁰

From the turning bias of -1.7 V in the C – V curve as shown in Fig. 1, E2 trap seems to come mainly from the GaAs cap region below the Schottky depletion edge and the QDs. A logarithmic dependence of its DLTS peak amplitude on the duration time of filling pulse from 10^{-4} to 9×10^{-2} s was observed, as shown in the inset of Fig. 4 suggesting that E2 trap is likely another kind of dislocation trap.

As for E5 trap, from the applied bias, it seems to reside near the QDs. From the XTEM images, a lot of misfit dislocations were observed near the QD boundaries. In addition, we have observed a similar relaxation-induced trap at 0.33 eV ($\sigma = 1.4 \times 10^{-18}$ cm²) along the InGaAs/GaAs interface in a relaxed In_{0.2}Ga_{0.8}As/GaAs sample¹⁴ with a very thick InGaAs layer (1000 Å). This highly relaxed InGaAs/GaAs sample contains a lot of misfit dislocations. Consequently, we tentatively assign E5 trap to be the misfit dislocation trap. More experimental data are needed in order to make a more conclusive argument.

The authors would like to thank the National Science Council of the Republic of China for financially supporting this research under Contract No. NSC-89-2112-M-009-024.

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