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MODEL REDUCTION TECHNIQUES FOR SPEEDING UP THE THERMAL SIMULATION OF PRINTED CIRCUIT BOARDS

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Key Words: PCB, thermal simulation, thermal modeling.

ABSTRACT

This paper initiates a measuring method to reduce the traditional three-dimensional thermal circuit models into the two-dimensional compact ones. The new thermal models are represented by the equivalent circuits which can be simulated in the SPICE. Furthermore, the ambient temperature and the power of the components are also decoupled to equivalent voltage and current sources, respectively. Therefore, when the ambient temperature or the power of the component changes, the compact thermal models can still work without doing any regeneration work. The proposed technique can greatly reduce the simulation time of heat transfer of printed circuit boards. Furthermore, the reduced models can be connected to any place on the model of the printed circuit board. The proposed technique provides a systematic synthetic way to build up models of printed circuit boards.

I. INTRODUCTION

In space electronic circuits or in power electronic circuits, the electrical characteristics of power electronic circuits and devices are greatly influenced by the operating temperatures of semiconductor devices. Thus it is important to simulate the coupled electrical and thermal systems simultaneously in the circuit design process.

Many papers have been published dealing with the analysis of the temperature of printed circuit boards (PCBs). Pinto and Mikic (1986) employ the analytical method. Funk *et al.*, (1992) use a semi-analytical method to prodict the steady-state temperature of printed circuit boards (PCBs). In considering a possible design situation to repetitively use a circuit board model, Godfrey *et al.*, (1993) develop an interactive thermal modeling method. The models of the chip and board were decoupled. Thus, this technique can save much modeling time in a case which needs to generate repetitive numerical-models.

In the temperature analysis of the PCB, the main governing equations are the heat diffusion equations. The finite Element Method (FEM) was also used to solve heat diffusion equations (Schaller, 1988). Chen and Yip (1992) use SPICE circuit models to characterize the thermal and dynamic behavior of the PCB. They use the Finite Difference Method (FDM) and imitate the circuit nodal equations to transfer the finite difference equations to R-C-V-I circuit models. With the use of electro-thermal circuit models, the circuit and thermal behavior can be simulated simultaneously in a SPICE system (Pokala and Divekar, 1989). However, since the electro-thermal models are three-dimensional, the simulation calculation needs a lot of time and memory capacity. To improve the computation efficiency of the electro-thermal models, two methods are developed. One is

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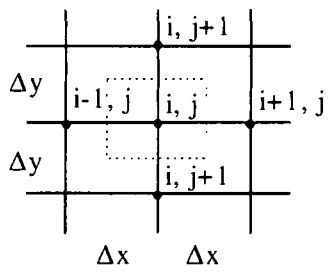

Fig. 1 The neighboring mesh points around the point (i,j)

a reduction technique which provides the theoretical supports to reduce the three-dimensional electro-thermal models into two-dimensional or even one-dimensional models (Vinke and Lasance, 1997). The other one employs the Asymptotic Waveform Evaluation (AWE) method which was proposed mainly for improving the computation speed of transient temperature response (Celik *et al.*, 1994; Chiprout and Nalhla, 1994; Lee *et al.*, 1990; Liu *et al.*, 1995).

In this paper, we propose a method which generates SPICE-styled reduced electro-thermal models of PCBs. These electro-thermal models can be run at high computation efficiency. Our simulation results have shown that our models can produce temperature simulations as accurate as those which are produced by the FDM three-dimensional models. The simulation speed of the proposed models is also much higher than that of the FDM three-dimensional models.

II. THE ELECTRO-THERMAL MODEL

1. Heat Diffusion Equations

The system concerning thermal conductivity is governed by the partial differential equations as follows,

$$\frac{\partial T}{\partial x}(k_x\frac{\partial T}{\partial x})+\frac{\partial T}{\partial y}(k_y\frac{\partial T}{\partial y})+\frac{\partial T}{\partial z}(k_z\frac{\partial T}{\partial z})=\rho C\frac{\partial T}{\partial t}+g\,, \qquad (1)$$

where k_x, k_y, k_z are the thermal conductivity in x, y, z directions, $T(x, y, z, t)$ is the temperature, $g(x, y, z, t)$ is the heat generating rate, ρ, is the material density, C is the material specific heat, and t is time.

The boundary conditions are also important to the thermal analysis. For devices on the earth, convection strongly affects the thermal activity in the components of circuits. Therefore, the convection governing equation is often applied in the thermal simulation. Newton's law of cooling depicts the outward energy transmitting rate as

$$q_c=hA(T_s-T_a), \qquad (2)$$

where h is the convection heat-transfer coefficient and T_s is the temperature of the surface of PCBs and T_a is the temperature of ambient air.

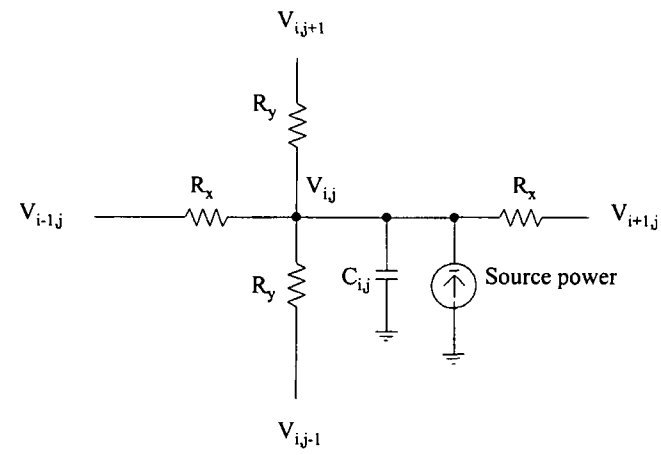

Fig. 2 The electro-thermal equivalent circuit at mesh (i,j)

2. Equivalent Circuit Representation

A practical method for solving the partial differential equations is to approximate the partial differential equations to finite difference equations. For a two-dimensional thermal object, the finite difference equations can be obtained by using x and y grid lines to divide the planar object into many tiny mesh panels. In the process of FDM each panel is presented by its center point, called the node. For example, Fig. 1 shows (1) a node (i, j), which is enclosed by the dot (grid) line segments and (2) four surrounding nodes. From Fig. 1 the associated finite difference equations can be obtained as

$$k_x\frac{T^p_{i+1,j}+T^p_{i-1,j}-2T^p_{i,j}}{(\Delta x)^2}+k_y\frac{T^p_{i+1,j}+T^p_{i-1,j}-2T^p_{i,j}}{(\Delta y)^2}$$

$$=\rho C\frac{T^{p+1}_{i,j}-T^p_{i,j}}{\Delta t}\,, \qquad (3)$$

The comparison of both Eqs. 2 and 3 with the conventional nodal equations gives an equivalent electro-thermal circuit representation as shown in Fig. 2, where each voltage $V_{i,j}$ represents the temperature of node (i,j), R represents the thermal resistance, and $C_{i,j}$ represents the thermal capacity of node (i,j).

III. THE TWO-DIMENSIONAL COMPACT MODEL OF IC COMPONENTS

In this section, we will introduce how we use the measuring method to obtain compact models of IC components. Typically the packages of IC components contain many distinct layers. Therefore, their electro-thermal steady-state models will have three-dimensional structures as shown in Fig. 3. The example of one fourth portion of the three-dimensional structure of a chip component is shown in Fig. 4, where I_s represents the power consumed by the chip, n is the number of the mesh panels within he chip area, and V_T represents the equivalent voltage of the ambient temperature. Since the bottom side of the

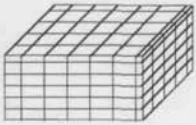

Fig. 3 Three-dimensional mesh structure of an IC component

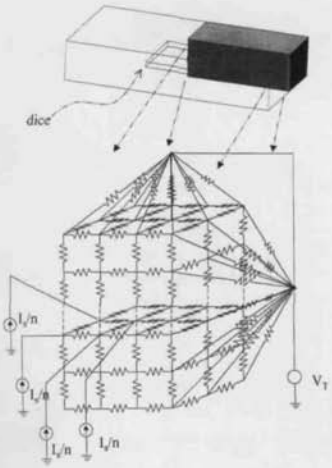

Fig. 4 One-fourth electro-thermal structure of an IC component

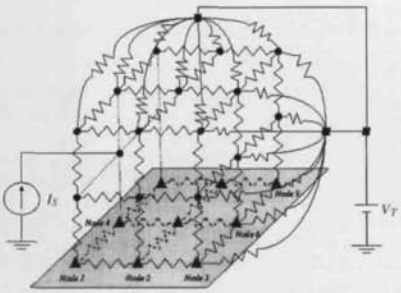

Fig. 5 The compact side

IC is assigned to touch the circuit board and both the front and left sides are actually inside the IC package, no air convection is counted for these three sides. This is the reason why ambient equivalent voltage V_T is not connected to these three sides.

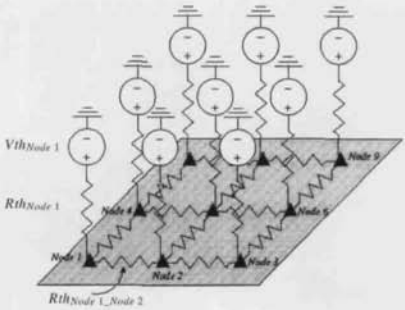

Fig. 6 The simplified equivalent compact circuit

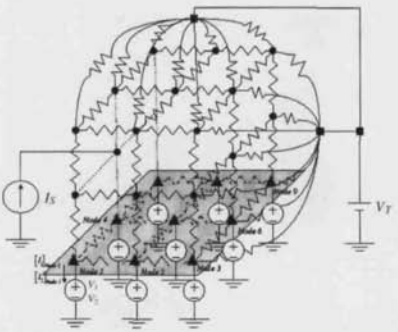

Fig. 7 Applying all the nodes to the original model with the same voltage

1. The Compacting Method

To simplify the demonstration, we will use Figs. 5 to 9 to demonstrate the proposed compacting method. The method is depicted as follows:

Step 1: Choosing the compacting side

The electro-thermal model of an IC component is considered having six sides. Choose the side which will face to board as the compact side. For example, the shadowed side shown in Fig. 5 is chosen to be the compacting side.

The succeeding work is to obtain the two-dimensional compact model as shown in Fig. 6, where Vth_{Node1} and Rth_{Node1} represent the Thévenin's equivalent voltage and resistance between node 1 and ground, respectively. The Rth_{Node1_Node2} is the neighboring resistance between node 1 and node 2.

Step 2: Obtaining the values of all the Thévenin's

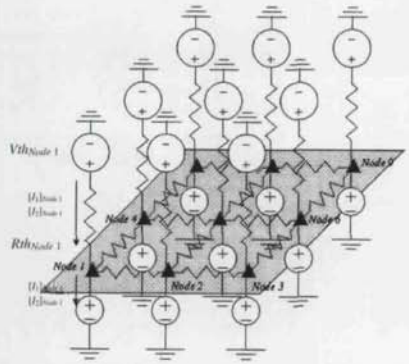

Fig. 8 Applying all the nodes to the compact model with the same voltage

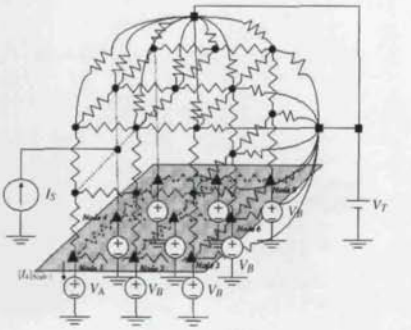

Fig. 9 Applying V_A to node 1 and V_B to all the other nodes of the original model

equivalent voltages and resistances

The Thévenin's equivalent voltages and resistances of each node in the compact side can be obtained by the process below

Procedure V_{th}**_and_**$R_{th}(M,A,V_{th},R_{th})$

Var M: The three-dimensional electro-thermal model
A: The compact side of M
$N(A)$: The total node number of A
V_{th}: Thévenin's equivalent voltage
R_{th}: Thévenin's equivalent resistance

for i=1 to $N(A)$ do
choose two constants V_1 and V_2
connect all the nodes in A with the voltage source V_{s1}, V_{s2}, ... $V_{sN(A)}$

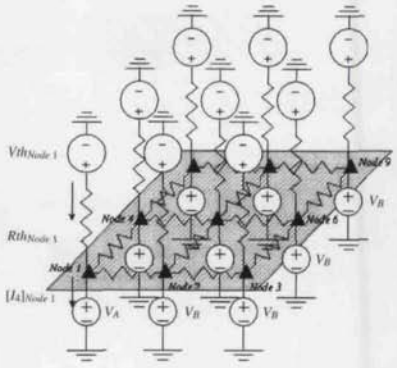

Fig. 10 Applying V_A to node 1 and V_B to all the other nodes of the compact model

which have the same voltage values of V_1
measure all the currents of V_{si}, i.e., $[I_1]_{Node\,i}$
change all the voltages of V_{si} to V_2

measure all the currents of V_{si}, i.e., $[I_2]_{Nodei}$
use the equivalent relation of Fig. 7 and Fig. 8 to construct Eq. (4)
Solve Eq. (4) to obtain $[Vth]_{Nodei}$ and $[Rth]_{Nodei}$

End Process

$$\begin{cases} [Vth]_{Nodei} = V_1 + [I_1]_{Nodei}[Rth]_{Nodei} \\ [Vth]_{Nodei} = V_2 + [I_2]_{Nodei}[Rth]_{Nodei} \end{cases} \quad (4)$$

Step 3: Obtaining the values of all the neighboring resistances

Similar to the procedure shown in step 2, each neighboring resistance, say the one which connects node 1 to a node i, can be measured and calculated by applying a voltage source V_A to node i and voltage sources V_B's to all the other nodes on the compacting side. The currents of the voltage sources are measured from Fig. 9 and denoted by I_3's. I_4's are the currents of branches of V_{th}-R_{th} and branches of voltage in Fig. 10. All the I_3's and I_4's of the nodes in the compact side are depicted in Table 1, which shows that

$$[I_3]_{Node1}-[I_4]_{Node1}$$
$$=([I_3]_{Node2}-[I_4]_{Node2})+([I_3]_{Node3}-[I_4]_{Node3})$$
$$+...+([I_3]_{Node9}-[I_4]_{Node9})$$
$$=I_{1,2}+I_{1,3}+...+I_{1,9} \quad (5)$$

Table 1 All the branch currents (unit: mA)

	$[I_3]_{Nodei}$	$[I_4]_{Nodei}$	$[I_3]_{Nodei}-[I_4]_{Nodei}$
Node1	7.0128	3.2932	3.7196
Node2	1.7016	3.4812	-1.7786
Node3	-0.2783	-0.0866	-0.1917
Node4	1.0481	2.4784	-1.4303
Node5	0.0816	0.2800	-0.1984
Node6	-0.6513	-0.6120	-0.0393
Node7	-0.5303	-0.4722	-0.0581
Node8	-0.7151	-0.6958	-0.0193
Node9	-0.7222	-0.7181	-0.0004
Total Currents	6.9479	6.9481	-0.0002

The percentage error obtained from Eq. (5) is only (0.0002/3.7196)×100(%)=0.0054%. Actually this small error comes from the calculation truncation and round-off errors. Therefore, Eq. (5) has already shown clearly that we need to consider all the possible current paths from node 1 to all the other nodes, i.e., there must exist neighboring resistors connecting node 1 to all the other nodes and they can be obtained by

$$R_{Node1\_Nodei} = \frac{V_3 - V_4}{[I_4]_{Nodei} - [I_3]_{Nodei}} \quad i=2, \ldots, 9 \qquad (6)$$

To obtain all the other resistances, a calculation similar to Eq. (6) is then applied to all the nodes on the compacting side until all the neighboring resistances are obtained.

Usually many neighboring resistances are very large so that they can be regarded as open circuits and omitted. Therefore, we can simplify the compact model further in different complex extents by neglecting the large resistances, each of which connect two nodes far away from each other. To express the neglect level, we have the following definitions of simplification levels.

2. More Simplified Models

Rectangular Wrapping Layer Consider all the orthogonal grid lines which connect all the nodes. A rectangular wrapping layer of a node i is an enclosed grid segment path which connects the neighboring nodes of node i. The first wrapping rectangular layer of a node i is the rectangular wrapping layer connecting the nodes nearest node i. The second rectangular wrapping layer is the layer connecting the nodes nearest the nodes in the first rectangular wrapping layer. By using the similar drawing method one can construct the third or higher order rectangular wrapping layers.

From the currents shown in Table 1 the neighboring resistance connecting the node-pair with a longer distance has a bigger resistance value. Therefore, we can simplify the compact model in the following ways,

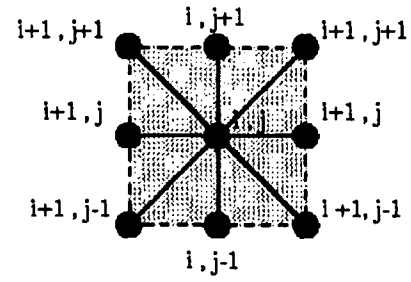

Fig. 11 The neighboring resistors of the order-1 simplified circuit

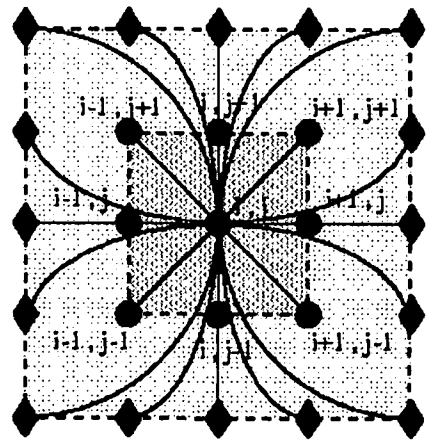

Fig. 12 The neighboring resistors of the order-2 simplified circuit

- **The order-1 simplified model** In the simplest compact model the nodes at two ends of any neighboring resistor lie in the first rectangular rapping layer. For instance, Fig. 11 shows all the neighboring nodes in the order-1 simplified model.
- **The order-2 simplified model** As shown in Fig. 12 all the neighboring nodes in the order-2 simplified model lie in the second rectangular wrapping layer.
- **The order-*n* simplified model** All the neighboring nodes in the order-n simplified model lie in the nth rectangular wrapping layer.

IV. ELECTRO-THERMAL MODELS FOR THE AMBIENT TEMPERATURE AND THE POWER OF THE IC COMPONENTS

During the operation of a circuit the ambient temperature may vary with some situations such as the poor convection environment or the temperature rise of the power components on the circuit board. Furthermore, considering the modeling flexibility, we expect that a powerful thermal simulation system should have the capability to build the thermal model of a circuit (board) in a handy way. Therefore, the system should have a library containing a variety of thermal models of components. Using this kind of system, the whole electro-thermal equivalent circuit can be easily built up by gluing all the component

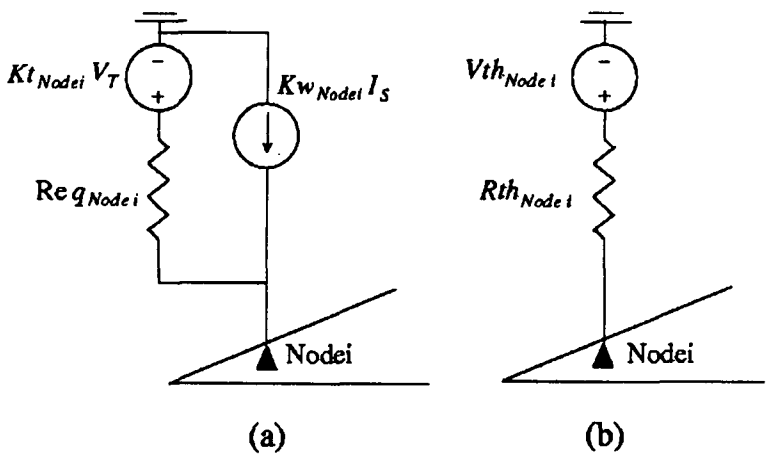

Fig. 13 (a) The decoupled equivalent circuits associated to the ambient temperature and chip power (b) the original Thévenin's equivalent power sources

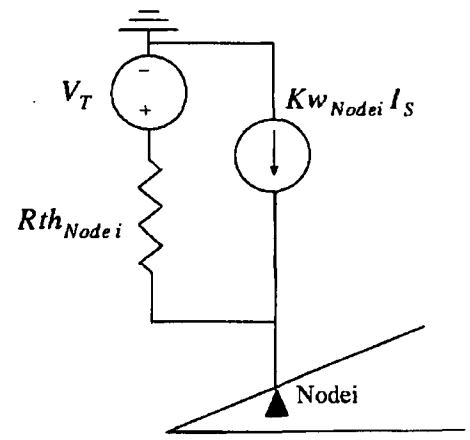

Fig. 14 The equivalent circuits associated to the ambient temperature and chip and chip power

models to the model of a circuit board. In this kind of system, optimizing the design of the library models becomes important. For this objective, we propose a technique to extract the equivalent power sources from the Thévenin's equivalent circuit branch obtained in Step 2 to the circuit shown in Fig. 13(a). By using the method proposed here, the (IC) components with the same package of features can use the same library model, which has the decoupled V_T, equivalent to ambient temperature, and I_S, equivalent to the chip power. Furthermore, both the V_T and I_S can be controlled by external sources.

We assume that the whole circuit system has only two kinds of heat sources, i.e., the power of IC chips and the ambient temperature. Therefore, a Thévenin's equivalent power source shall be produced by the supply power of the IC chip and the ambient temperature. Since the electro-thermal model of the chip power of an IC component is equivalent to a current source and also all the elements in the electro-thermal model are linear ones, the Thévenin's equivalent power source contributed by chip power to node i shall also be the current source, denoted as $Kw_{Nodei}V_s$ as shown in Fig. 13(a), where I_s is the electro-thermal equivalent current source of the chip power. Since the electro-thermal circuit of the ambient temperature is a voltage source, Thévenin's equivalent power source contributed by ambient temperature to node i shall be a voltage source, $Kt_{Nodei}V_T$. The statements above conclude that the circuits in Figs. 13 (a) and (b) shall be equivalent and satisfy the relation of

$$Vth_{Nodei}=Kt_{Nodei}V_T+Kw_{Noddei}I_s\mathrm{Re}q \tag{7}$$

Since Figs. 13(a) and (b) shall be equivalent even though the chip power is zero, Kt_{Nodei} must be one and Req_{Nodei} must be equal to Rth_{Nodei}. Thus, the final equivalent Thevenin's equivalent circuit is shown in Fig. 14 and Eq. (7) can be simplified to

$$Vth_{Nodei}=V_T+Kw_{Noddei}I_sRth \tag{8}$$

The last unknown parameter, Kw_{Nodei}, can be obtained by using the following procedures:

(1) applying any ambient temperatures, V_T', to each node i of the compact side,
(2) using the measuring method to obtain the corresponding Thvenin's equivalent voltages, $[Vth_{Nodei}]'$, and
(3) employing V_T', $[Vth_{Nodei}]'$ to Eq. (8) to obtain the value of Kw_{Nodei}.

V. EXAMPLES AND SIMULATION RESULTS

In the previous sections we have introduced our measuring method to obtain a compact electro-thermal model of a chip. In this section we apply the proposed compacting method to an IC example and compare the simulation results with the results obtained by a three-dimensional electro-thermal model. Furthermore, a popular PCB example with two chips (Liu, *et al.*, 1995; Funk, *et al.*, 1991) is also tested here.

1. An IC Example

The properties of an IC are depicted as follows. The package has the size of $x\times y\times z$=20mm×8mm ×2mm. In z-direction, the lead frame locates from 0.875mm to 1.125mm and circuit dice locates from 1.125mm to 1.375mm. The 1/4 portion of the IC package is shown in Fig. 15. We use dot grid lines to chop the IC into several mesh panels. The 1/4 portion of IC three-dimensional mesh structure is shown in Fig. 16. The panel sizes in both of the x and y directions are 1mm×1mm and 0.25mm in z direction. Each panel is represented by a dark node at the center of the panel. The total number of the mesh panels in the 1/4 portion of IC is 11×5×9.

Table 2 shows the parameters of the IC package with the circuit chip inside. The area of circuit chip is assumed covering ten mesh panels in the center part of IC and the power consumed by the IC is 0.125W.

Table 2 Parameters of the IC components

Components	chip	dice	leadframe
$K(W/°C)$	0.000628	0.06	0.0204
$h_i op(W/mm^2 \cdot °C)$	0.00005	0.00005	0.00005
$C_p(J/g°C)$	0.84	0.9	0.9
$\rho(g/mm^3)$	0.00144	0.0027	0.0027
$T_{initial}(°C)$	25	25	25
$T_{ambient}(°C)$	25	–	–
Location(mm)	–	[0,4.5]*[0,1.5]*	[0,5.5]*[0,1.5]*[0.875,1.125]
$[x_1,x_2]*[y_1,y_2]*[z_1,z_2]$	–	[1.125,1.375]	[5.5,10]*[0,0.5]*[0.875,1.125]
			[1.5,2.5]*[2.5,4]*[0.875,1.125]
			[3.5,4.5]*[2.5,4]*[0.875,1.125]
			[5.5,6.5]*[2.5,4]*[0.875,1.125]
			[7.5,8.5]*[2.5,4]*[0.875,1.125]
$P_{source}(W)$	0	0.125	0

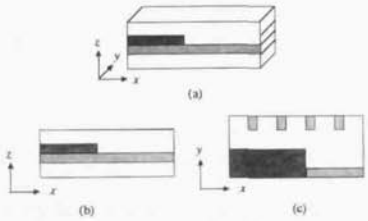

Fig. 15 The structure of 1/4 protion of the IC (a) the 3-D drawing (b) the side view of IC (c) the top view of IC

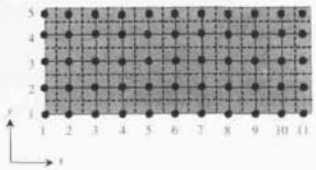

Fig. 16 The bottom side of the IC and its mesh panels and nodes

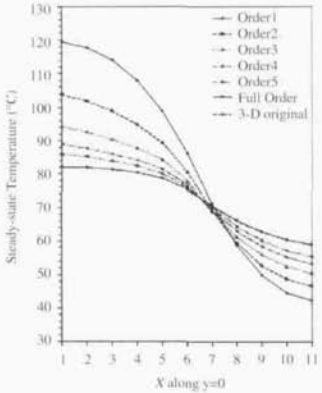

Fig. 17 The temperature distribution of the six simplified compact models along y=0

For simplification, each mesh panel of the circuit chip is assumed to consume the same power, in other words, 0.0125W for each chip mesh panel. The IC has been modelized and simplified to five compact ones. All of them have been simulated and the simulation results are shown in Figs. 17-20, where the percentage error is defined by Eq. (9),

$$Error(\%) = \frac{[T_{order n}]_{Node i} - [T_{3-D}]_{Node i}}{[T_{3-D}]_{Node i}} \times 100 \qquad (9)$$

The percentage error defined in Eq. (9) is calculated from the temperature difference between the n-order simplified compact model and the three-dimensional model. One can see that the higher the order of the model is, the less the simulation error, the shorter the computation time, and the less the required memory will be. Those results are shown in Table 3. Actually, if we use the full order model, i.e., all the possible neighboring resistors are considered, we will obtain a highly accurate model. This effect can be seen from Figs. 18 and 20. Moreover, if the 1-order model is taken, we will see that the computation performance is around fifteen times better than which is obtained from the three-dimensional model.

2. A PCB with Two Chips

Figure 21 shows the top view of the PCB with

Table 3 The performance comparison between three-dimensional model and six simplified compact models

model orders	total nodes	total components	CPU time (S)	memory size(KB)
order-1	111	284	0.76	201
order-2	111	548	0.97	369
order-3	111	830	1.31	391
order-4	111	1070	1.63	561
order-5	111	1220	1.85	745
full order	111	1595	1.97	889
3-D model	442	1308	5.29	1832

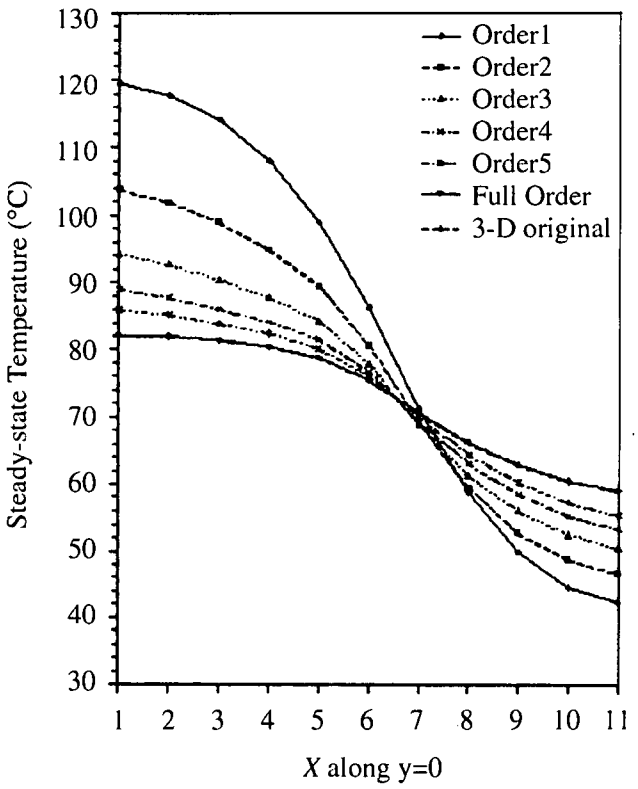

Fig. 18 The temperature percentage errors of the six simplified compact along y=0

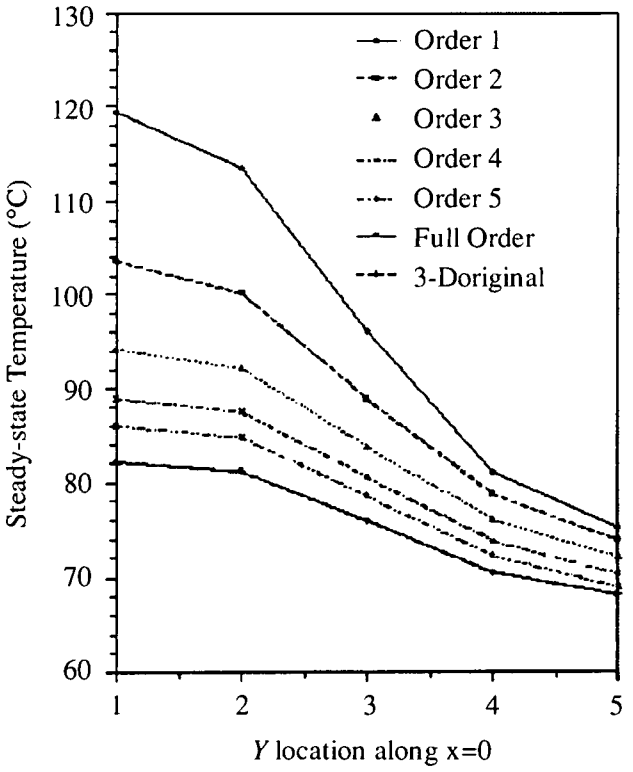

Fig. 19 The temperature distribution of the six simplified compact models along x=0

two chips. The radiation is not considered here. The property parameters of the whole board and chips are shown in Table 4 and Fig. 22. The mesh size is 1 mm in all directions, x, y, and z. The connection resistances between the models of IC chips and PCB are assumed to be very small in this article. To show the temperature simulation of the PCB, the temperature distribution along two lines of y=22 mm and y=27 mm are calculated. The simulation results are shown in Figs. 23-24. For this example one can see that both the order-1 and full order models give almost the same temperature distribution results.

VI. DISCUSSION

Our many simulation results have shown that (1) the full order compact model is as accurate as the three-dimensional electro-thermal model, (2) when a board contains very few chips, a simplest compact model can also produce the results as accurate as those which are produced by the three-dimensional models.

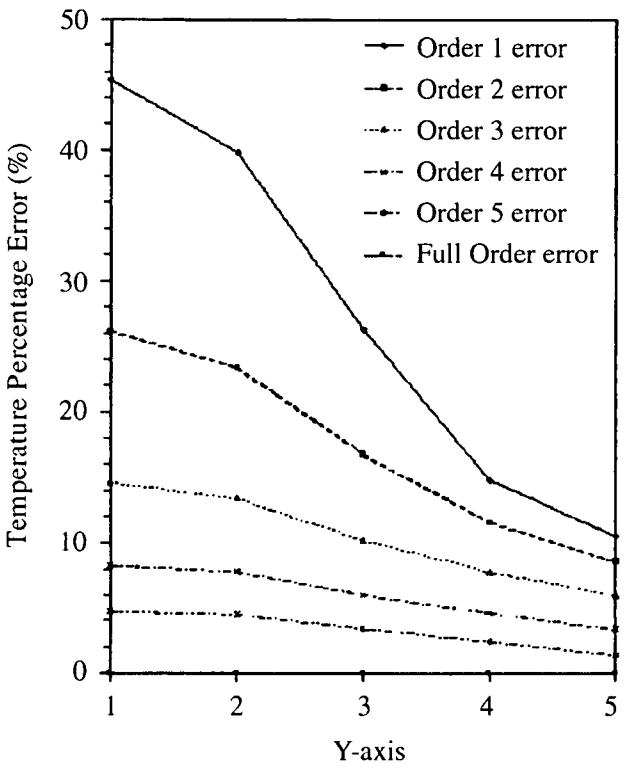

Fig. 20 The temperature percentage error distribution of the six simplified compact models along x=0

Table 4 The parameters of PCB and chips

Components	PCB	chip1	Chip2
k(W/°C)	0.0163254	Layer1 0.000669 Layer2 0.00433 Layer2 0.00433	Layer1 0.000669 Layer3 0.00433 Layer3 0.00433
h_{top}(W/mm²°C)	0.00000638	0.00000638	0.00000638
C_p(J/g°C)	2	1	1
ρ(g/mm³)	0.0023	0.002	0.002
$T_{initial}$(°C)	25	25	25
$T_{ambient}$(°C)	25	25	25
P_{source}(W)	0	1.25	1.3

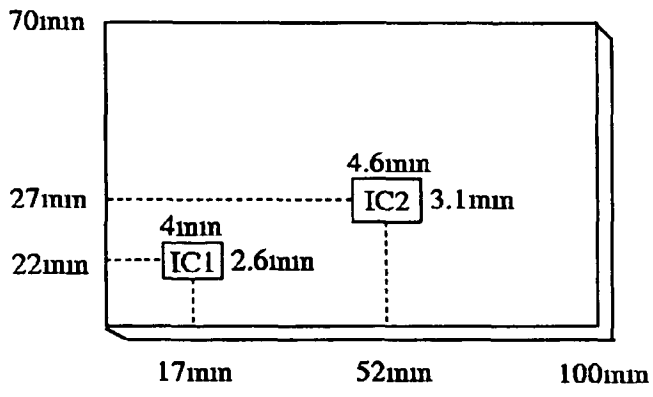

Fig. 21 The top view of the PCB

	Thickness (mm)	Conductivity (W/mm°C)
EPOXY	1.71	0.000669
CHIP	0.28	0.00433
ADHESIVE	0.038	0.00433
copper	0.081	0.328
filber card	1.575	0.00297

Fig. 22 The composition of the PCB and the chip on it

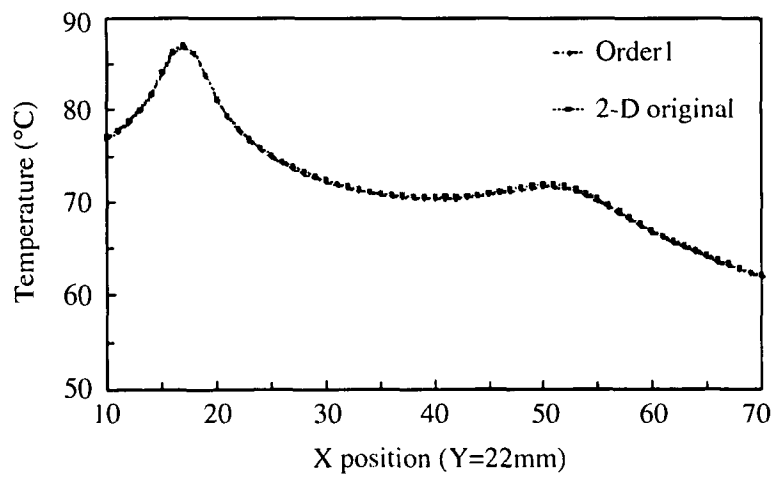

Fig. 23 The composition of the PCB and the chip on it

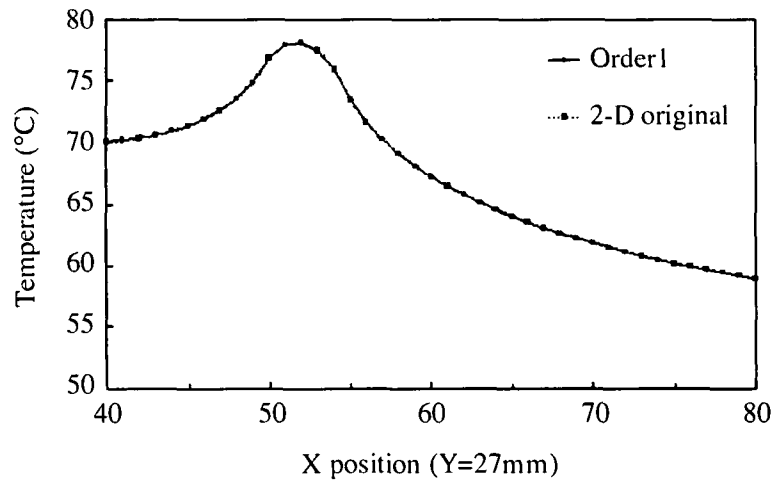

Fig. 24 The composition of the PCB and the chip on it

Our measuring method may also be fulfilled by using practical instruments in the future if the associated measuring instruments are developed.

Moreover, our compacting method can be used to build up the electro-thermal components library. As long as the library has been generated, the electro-thermal model of a PCB can be set up by simply connecting all the component models, which are stored in the library, to the PCB model such as what we have done in Section 5.2.

Since we consider that the wire locations on the PCB cannot be determined before the detailed routing results are obtained and the data needed for analyzing a PCB which is routed in multi-layers is huge, we use two-dimensional average thermal board models and compact component models to analyze the PCBs. Although the proposed compacting method can also be applied to simplify the three-dimensional thermal model of a PCB, one still needs huge memory size and the detailed routing data for the simplification process. Therefore, unless one can have either a very big computer memory or real measuring instruments to apply the proposed measure method to obtain the compact PCB thermal model, we suggest choosing the average thermal board models and the compact component thermal models to analyze the PCBs.

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加速電路板熱模擬的模型簡縮法

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摘　要

本篇首創一種使用量測的方法，將傳統三維熱模型濃縮成二維熱模型。這新的熱模型是一等效電路的型態，它可以在SPICE上做模擬。我們甚至更進一步的把熱源－(環境溫度和晶片功率)藉量測的方法各自分離成等效電壓源和電流源。因此在模擬時環境溫度和晶片功率都是可隨意改變，模擬過程中壓縮的熱模型仍可使用，不需再費時重造。這裡所推的方法能大大的縮短電路板熱模擬時間，甚至壓縮的熱模型可輕易的接上電路板熱模型的任何位置；這裡所提供的技術乃是用系統的綜合法構建出電路板的熱模型。

關鍵詞：印刷電器版，熱模擬，熱模型。