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Characteristics of TEOS Polysilicon Oxides: Improvement by CMP and High Temperature RTA N_2/N_2O Annealing

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The integrity of tetraethylorthosilicate (TEOS) polyoxide using chemical mechanical polishing (CMP) plus a high temperature rapid thermal annealing (RTA) step was studied in this work. The surface morphology of polysilicon is improved after a CMP process. Polyoxides deposited by low pressure chemical vapor deposition (LPCVD) TEOS in conjunction with CMP and RTA N_2/N_2O annealing exhibit a better current-electric field (J-E) curve, higher charge to breakdown ratio, and lower electron trapping rate. In addition, the composite bilayer (TEOS deposited and thermally grown by RTA) polyoxide film introduces an asymmetry of electrical leakage current, trapping characterization, and charge to breakdown, with respect to the injection of different polarity ($+V_g$ and $-V_g$).

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To obtain a longer data retention time for nonvolatile memories, polyoxides with a low-leakage current, high dielectric strength, and high charge to breakdown[1-3] Q_{bd} are required. However, a rough surface at the polyoxide/polysilicon interface and the nonuniformity of polyoxide thickness result in a high local electric field. This high local electric field causes the polyoxide to exhibit a high leakage current and lower dielectric breakdown field in comparison with the silicon dioxide grown from a single crystalline silicon substrate.[4-8] It is well known that the integrity of polysilicon oxide depends strongly on the oxidants used for growth or postoxidation annealing.[9-15] Polyoxide has been demonstrated to have an improved electric property when it is grown in N_2O ambient.[14,15] Such an improvement is due to the incorporation of nitrogen by using N_2O. In other words, oxide deposited by chemical vapor deposition (CVD) and annealed in N_2/N_2O has a relatively smooth surface at the polyoxide/poly-Si interface compared with that grown by thermal oxidation.[10-13] Such a smooth surface results from the fact that the grain boundaries of the bottom polysilicon do not propagate into the polyoxide film. Another approach to improving the surface morphology of poly-Si is to use an adequately controlled chemical mechanical polishing (CMP) process for bottom polysilicon film.[16,17] The planar surface morphology, after CMP, has been shown to result in an improved integrity of polyoxide.

Hence, in this paper, for the first time, the integrity of tetraethylorthosilicate (TEOS) polyoxide has been studied using CMP and a high temperature rapid thermal annealing (RTA) step. Polyoxides deposited by low pressure chemical vapor deposition (LPCVD) TEOS with subsequent steps using CMP and RTA show superior performance, for example, a better current-electric field (J-E) curve, higher Q_{bd}, and lower electron trapping rate. The characteristics of TEOS polyoxide annealed in N_2O at different temperatures are also discussed. Furthermore, the surface roughness and surface morphology of polyoxide/poly-Si interface are characterized using atomic face microscopy (AFM) and transmission electron microscopy (TEM) analyses. Finally, secondary-ion mass spectrometry (SIMS) analysis is performed to investigate depth profiles of nitrogen.

Experimental

In this work, n^+ poly-Si/ polyoxide/n^+ poly-Si capacitors were fabricated. Samples were fabricated on p-type silicon (100) wafers of which they were oxidized to grow 2000 Å silicon dioxide films. Subsequently, a 3000 Å poly-Si film, poly-1, was deposited at 620°C and doped by $POCl_3$ (with a sheet resistance of 50-70 Ω/□). The rugged surface of the poly-Si films were polished by using the CMP process,[16] and the wafer was cleaned in a scrubber and ultrasonic oscillator with $NH_4OH:H_2O_2:H_2O$ (1:1:10) solution to remove the particles and metallic contamination. Next, an additional RCA clean process was performed to ensure the cleanness of the surface. The polyoxide film, about 114 Å, was deposited by LPCVD TEOS at 700°C on both CMP and non-CMP samples. Then, the samples were split to receive high temperature RTA for 30 s in N_2 (850, 950°C) or in N_2O (750-1050°C) ambient. After that, poly-2 was deposited and doped to have a sheet resistance of 50-70 Ω/□ by $POCl_3$. Poly-2 was defined and etched to form the capacitors. All samples were thermally oxidized to grow a 1000 Å thick oxide using a wet oxidation process. Contact holes were opened and aluminum was sputtered and patterned to form electrodes connecting poly-2.

Table I lists all of the device types fabricated in this work along with their measurement data for breakdown field (E_{bd}) and Q_{bd}, performed under constant current stress of +10 mA for $+V_g$ injection and at −10 mA for $-V_g$ injection. The area of capacitors is 6×10^{-4} cm^2. The thickness of polysilicon oxide was measured by using the Keithley capacitance-voltage method. The surface roughness in root mean square (rms) was studied using AFM. To reveal the actual surfaces of our samples, the surface morphology was measured after the stripping of the TEOS polyoxide in diluted HF solution. Electrical characteristics and constant current stress were measured using an HP4145 semiconductor parameter analyzer. The surface morphology of the polyoxide was also studied by TEM. Finally, the depth profiles of nitrogen were investigated using SIMS.

Table I. List of the device types fabricated.

Sample ID	Thickness (nm)	Roughness rms (nm)	E_{bd} (MV/cm)		Q_{bd} (C/cm^2)	
			$+V_g$	$-V_g$	$+V_g$	$-V_g$
CMP As-deposited	11.7	0.75	12.93	12.68	4.51	1.32
As-deposited	11.4	5.13	12.83	12.67	3.01	1.24
CMP $850N_2$	11.7	0.82	12.96	12.86	7.69	1.87
$850N_2$	11.4	5.24	12.9	12.76	4.54	1.29
CMP $950N_2$	11.7	0.96	13.23	13.18	13.39	2.23
$950N_2$	11.4	5.34	12.93	12.92	7.25	1.96
CMP $750N_2O$	12.6	1.11	13.19	13.05	27.98	3.16
$750N_2O$	12.3	5.12	12.92	12.92	21.07	2.33
CMP $850N_2O$	13.6	1.25	12.88	12.63	33.07	4.57
$850N_2O$	13.3	5.3	12.7	12.56	24.2	4.04
CMP $950N_2O$	14.9	1.5	12.75	11.63	14.17	10.28
$950N_2O$	14.5	5.36	12.62	11.44	11.97	8.46
CMP $1050N_2O$	15.9	1.7	12.7	12.41	10.02	12.27
$1050N_2O$	15.5	5.35	12.6	12.32	9.18	10.08

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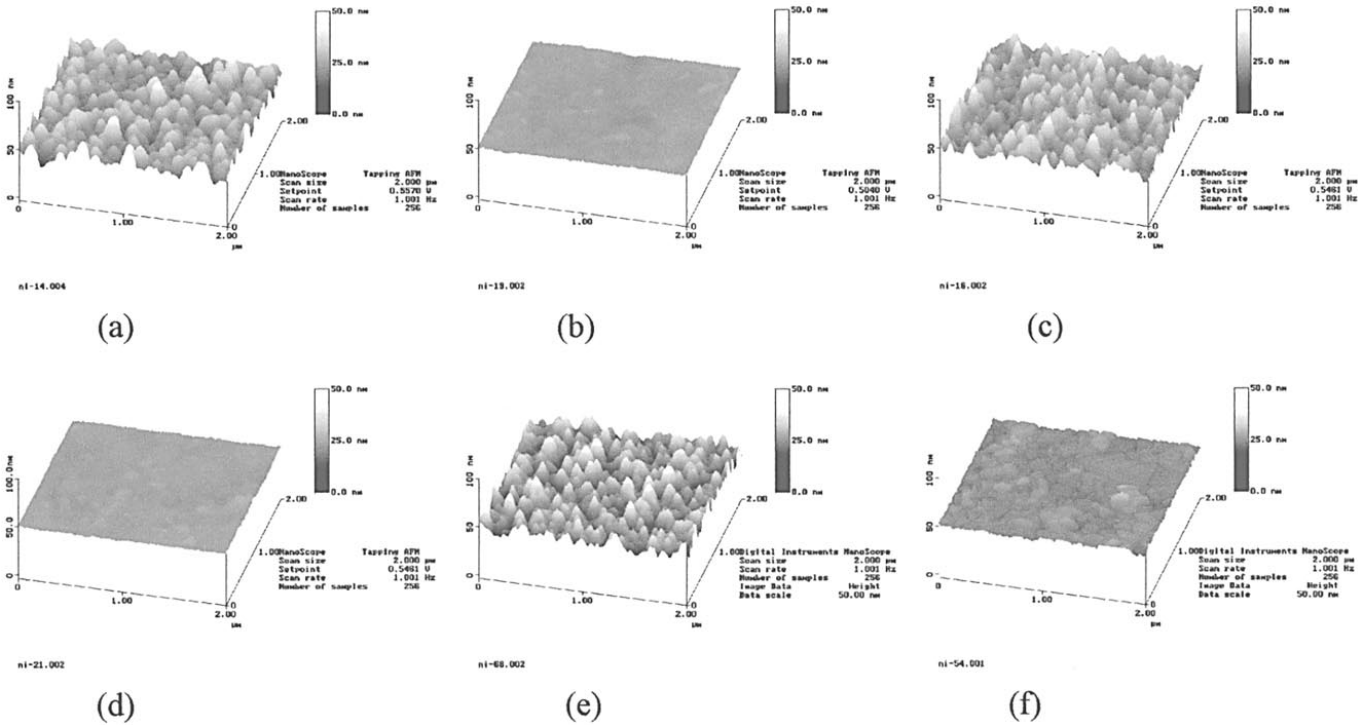

Figure 1. Surface image measured by AFM for (a) non-CMP as-deposited, (b) CMP as-deposited, (c) non-CMP sample after 850°C N_2 RTA annealing, (d) CMP sample after 850°C N_2 RTA annealing, (e) non-CMP sample after 850°C N_2O RTA annealing, (f) CMP sample after 850°C N_2O RTA annealing.

Results and Discussion

Table I lists various samples fabricated in this work along with their measurement data for surface rms, E_{bd}, and Q_{bd}, performed under +10 mA for + V_g injection and −10 mA for $-V_g$ injection.

Figures 1a-f depict the surface morphology images of polyoxide/poly-Si interfaces for samples investigated by AFM. To disclose the actual surface of the poly-Si layers after the deposition, dilute HF solution was used to strip the oxides. Figures 1a-b illustrate the original surface of non-CMP and CMP samples after the deposition of TEOS polyoxide. With the information provided by these two figures we find that the surface morphology can be improved significantly by using CMP. Figures 1c and e display the AFM image of the non-CMP poly-Si after annealing samples in N_2 or N_2O ambient, respectively. A rough and nonuniform surface was observed. CMP processed samples, after annealing in either N_2 or N_2O ambient, exhibited a smooth and uniform surface, as shown in Fig. 1d and f. As for the non-CMP samples, the initial surface roughness (5.1-5.2 nm) found in Fig. 1a of the polyoxide/poly-Si interface was almost the same as those after RTA annealing processed in N_2 or N_2O ambient (5.2-5.4 nm) as presented in Fig. 1c and e. As for the CMP samples, the initial surface roughness (0.7-0.8 nm) observed in Fig. 1b was only slightly increased as compared with those after RTA annealing both in N_2 (0.8-1.0 nm) or in N_2O ambient (1.2-1.5 nm), as shown in Fig. 1d-f, respectively.

Figures 2a and b present the cross section of TEM for non-CMP and CMP samples, while Fig. 2c and d show the corresponding samples which were annealed in N_2O ambient. As can be seen from these figures, the CMP samples in Fig. 2b and d have smoother surfaces than those of the non-CMP samples shown in Fig. 2a and c.

Figures 3a and b depict the SIMS depth profiles of nitrogen for the samples manufactured in this experiment. The actual percentage of N_2 was normalized with respect to the counts of Si in the sample. As shown in Fig. 3a, a significant amount of nitrogen existed at the TEOS polyoxide/poly-1 interface for the N_2O annealed sample despite the fact that a much smaller amount was found for the N_2 annealed sample and the control one. The nitrogen incorporated at the TEOS polyoxide/poly-1 interface has been reported to have the effects of improving TEOS quality.[12,13] Figure 3b indicates that the nitrogen profile of the CMP sample after RTA annealing in N_2O ambient exhibits the narrowest and largest peak distribution among all of the samples. It is evident that during the high temperature thermal oxidation the oxidant might diffuse into deeper distance through the grain boundary via the rough (or nonuniform) surface and create a broader and deeper N_2 distribution, similar to the conclusion derived from previous investigation.[17]

Figures 4a and b present the *J-E* characteristics of polyoxides. The *J-E* curve is calculated by using the initial current-voltage (*I-V*) curve of the polyoxide, where $J = I/$(area of capacitors) and $E =$

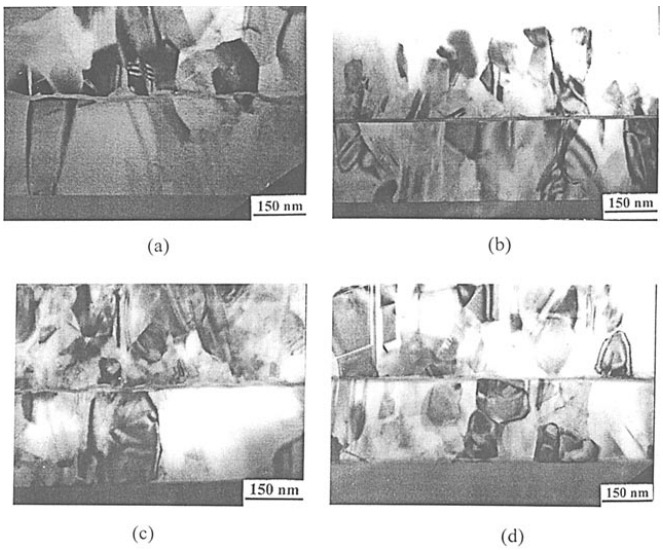

Figure 2. The TEM micrographs of (a) non-CMP as-deposited, (b) CMP as-deposited, (c) non-CMP sample after 850°C N_2O RTA annealing, (d) CMP sample after 850°C N_2O RTA annealing.

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V/(thickness of oxide). Obviously, for both N_2 and N_2O annealed polyoxides, CMP samples resulted in a lower leakage current than those of non-CMP samples under both positive ($+V_g$) poly-1 and negative ($-V_g$) poly-2 injection. This phenomenon is attributed to the high local electric field caused by the nonuniformity of thickness in the polyoxide film and the asperity at the polyoxide/poly-1 interface,[1] especially for the non-CMP samples.[16] In other words, the smooth surface of polyoxide/poly-1 of the CMP sample contributes to a smaller localized current density; therefore, under the same electrical field, an improved uniformity of localized electric field is obtained for CMP samples as compared with non-CMP samples.

The charge trapping characteristics of the polyoxide were also investigated. Figures 5a and b show the gate voltage shifts of samples under +10 mA ($+V_g$) and −10 mA ($-V_g$) constant current stress. It is noted that the voltage shift is reduced after high temperature RTA N_2/N_2O annealing. Furthermore, all of the CMP samples had smaller voltage shifts than those of non-CMP samples under either $+V_g$ or $-V$g stress based on these figures. This phenomenon suggests that CMP samples would trap fewer electrons than those of non-CMP samples. On the other hand, it is also expected that a rugged polyoxide/poly-Si interface (non-CMP) can easily generate certain localized trapping sites to induce local current, thus causing a higher electron trapping.

Figures 6a and b illustrate the Q_{bd} characteristics of these samples under +10 mA ($+V_g$) and −10 mA ($-V_g$) gate injections. It is worth mentioning that the Q_{bd} of the TEOS polyoxide is increased after annealing at high temperature RTA using N_2/N_2O. Also, the CMP sample demonstrates a larger Q_{bd} than that of the non-CMP sample. It can be inferred that the roughness existing at a polyoxide/poly-Si interface would provide various trap sites and lead to a higher current density with higher electron-trapping rate, capable of causing smaller Q_{bd} values. Furthermore, it should be noted that polyoxide annealed in N_2O ambient has better *J-E* curves, smaller voltage shifts, and larger Q_{bd} values as compared with the rest of samples. The mechanism of effecting these improvements is due to the incorporation of N_2 at the TEOS polyoxide/polysilicon inter-

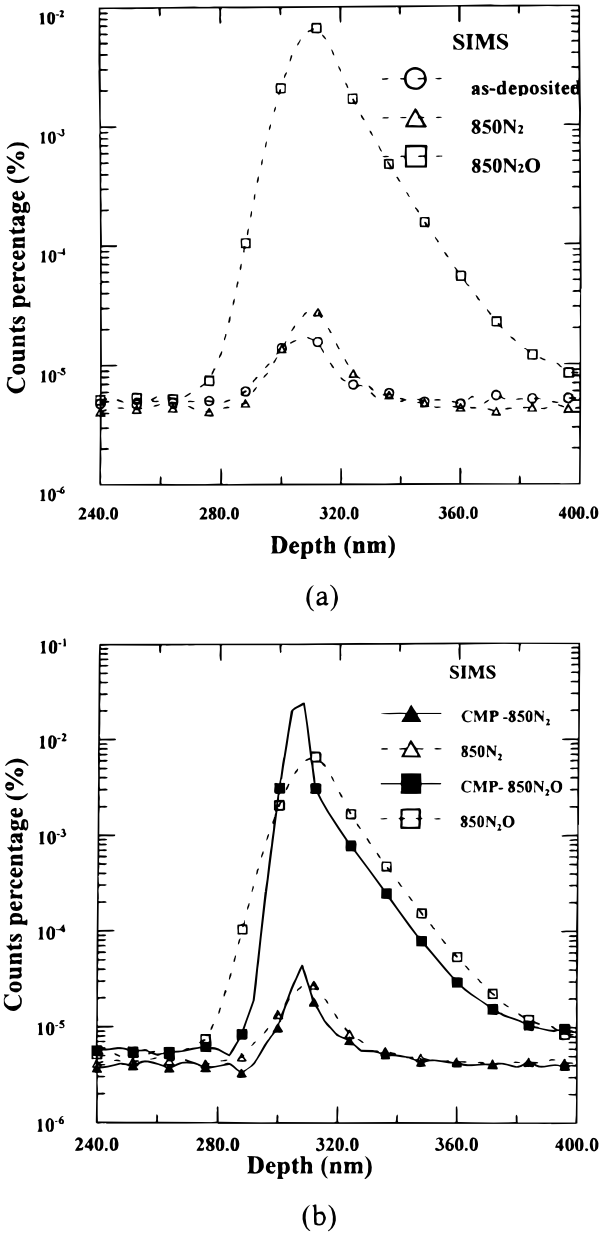

Figure 3. SIMS depth profiles of nitrogen in (a) non-CMP samples, (b) non-CMP and CMP samples after 850°C N_2/N_2O RTA annealing.

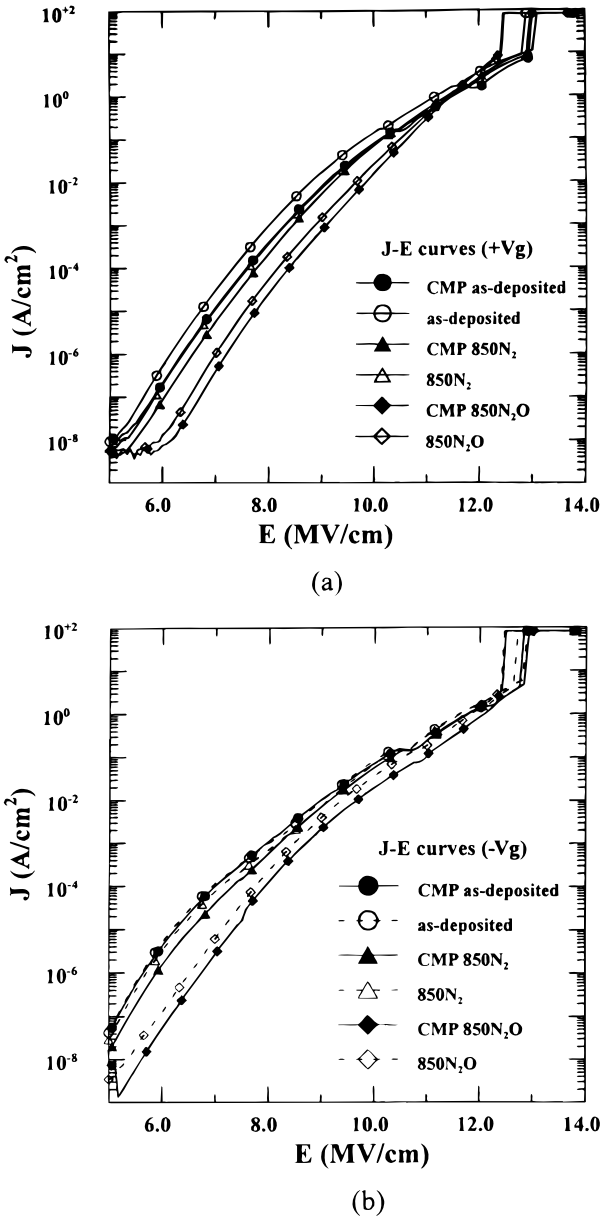

Figure 4. The *J-E* characteristics of TEOS polyoxides under (a) $+V_g$ injection, (b) $-V_g$ injection.

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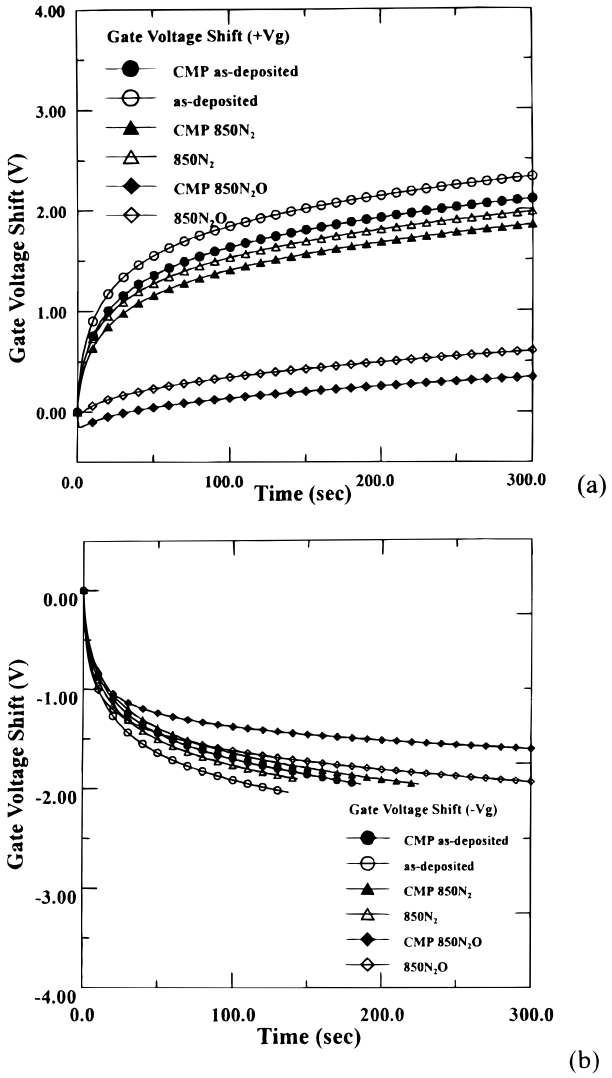

Figure 5. The charge trapping characteristics of TEOS polyoxides under (a) $+10$ mA/cm^2, (b) -10 mA/cm^2 constant current injection.

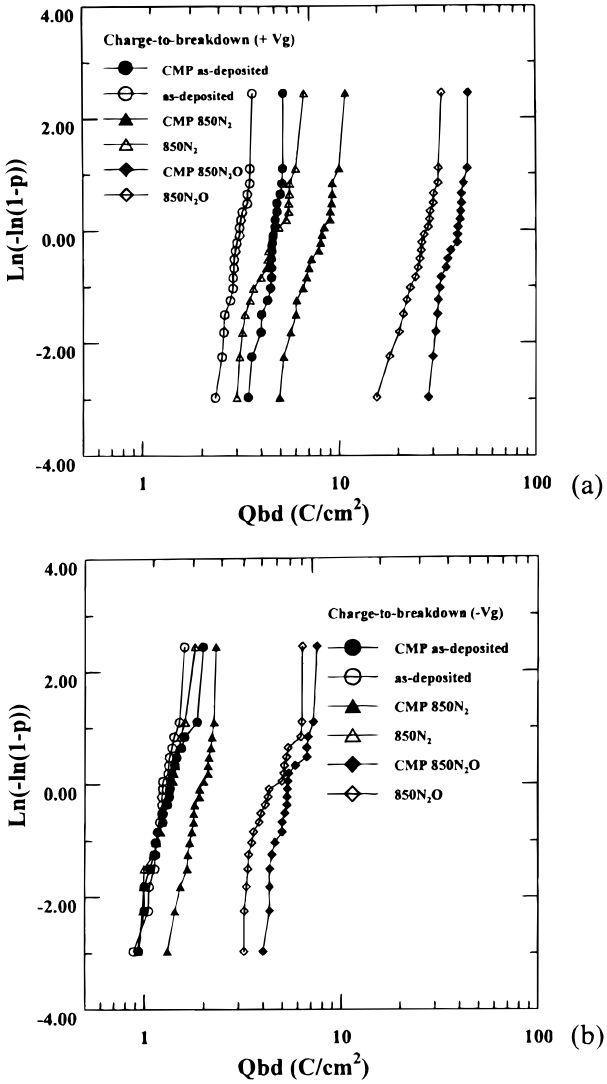

Figure 6. The Q_{bd} characteristics of TEOS polyoxides under (a) $+10$ mA/cm^2, (b) -10 mA/cm^2 constant current injection.

face,[12-15] as shown in Fig. 3a. In respect to CVD deposition of polyoxide, there are two factors which will affect its electrical characteristics. One of them is the surface roughness and the other is the intrinsic trapping in the CVD oxide. We believe that the quality of a TEOS oxide would be affected more by the intrinsic effects than by the surface roughness due to the fact that the thickness of TEOS deposited was about 11 nm thick in this experiment. After high temperature RTA, the trap located in TEOS oxide is reduced with its dependence on surface roughness being observed, as demonstrated by CMP850N2 and 850N2 samples in Fig. 6a, b. Moreover, RTA N_2 annealing with a temperature higher than 900°C can improve the quality of TEOS as shown in Table I, and this is consistent with Ref. 12.

From the results mentioned above, it is reasonable to suggest that adding an adequately controlled CMP process not only reduces the surface roughness of the poly-1 but also improves the inclusion of nitrogen during high temperature N_2O annealing. Although the incorporation of nitrogen at interface can improve the quality of polyoxide, the rough interface degrades the performance of non-CMP samples under both $+V_g$ and $-V_g$ gate injection. By adding the CMP process, bumps on the poly-1 surface[1] are removed and a smooth surface can be obtained. Moreover, the electrical properties of TEOS polyoxide can be improved after high temperature N_2/N_2O annealing. Consequently, a sequence combining high temperature N_2/N_2O annealing step and CMP process should result in an optimized approach to processing the TEOS polyoxide.

Figure 7 depicts the SIMS depth profiles of nitrogen of CMP samples after different N_2O annealing temperatures in this experiment. As shown in this figure, the amount of nitrogen is increased as the temperature of annealing is increased.

Figures 8 shows the thickness of polyoxide and the roughness of CMP samples after high temperature N_2O annealing. It is clear that the thickness of TEOS polyoxide increases as the N_2O annealing temperature increases. Besides, the surface of TEOS polyoxide/ poly-1 interface becomes much rougher at higher temperature N_2O annealing. At a high temperature N_2O annealing process, a thin thermal polyoxide will be grown between the TEOS polyoxide and poly-1 interface, hence, the total thickness of polyoxide will be increased. During the thermal oxidation of poly-Si, grain boundaries were oxidized more rapidly than the central part of the grains. V-grooves at the polyoxide/poly-Si interface are formed as a result of having different oxidation rates between grain boundaries and their associated grains.[5] At the same time, longer oxidation also increases the size of the grooves, the surface roughness at the polyoxide/poly-Si interface, and the nonuniformity of polyoxide film thickness.[1,5,14]

Figures 9a and b illustrate the *J-E* characteristics of TEOS polyoxides under $+V_g$ injection and under $-V_g$ injection. It is found that, for $+V_g$ injection, the leakage current of TEOS polyoxide is reduced

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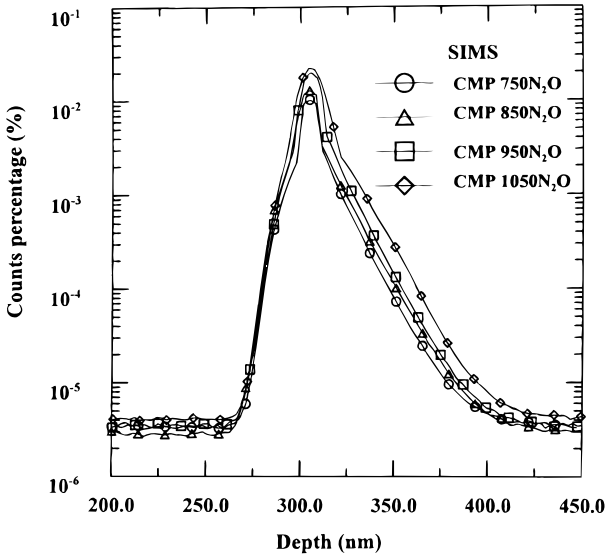

Figure 7. SIMS depth profiles of nitrogen in CMP samples after different high temperature N_2O RTA annealing.

but the reverse trend was found under $-V_g$ injection. However, the surface of the TEOS polyoxide/poly-1 becomes more rugged as the temperature of N_2O annealing is increased as shown in Fig. 8. As a result, the local electrical field is increased as well due to the increment of surface roughness and nonuniformity with respect to the polyoxide film.[1] Again, it can be seen that the breakdown field becomes worse for both $+V_g$ injection and $-V_g$ injection as the temperature of N_2O annealing is increased. Besides, the growth of a thin layer of thermal polyoxide at the TEOS polyoxide/poly-1 interface was found by using N_2O annealing at high temperature. This two-layer (TEOS deposited and thermally grown) polyoxide film may introduce an asymmetry[3] on the electrical leakage current for different polarity ($+V_g$ and $-V_g$) injection. Furthermore, the amount of nitrogen at the TEOS polyoxide/poly-1 interface is increased as the annealed temperature is raised, with which it may affect the asymmetry as well.

Figures 10a and b show the shifts of gate voltage for samples under constant current stress at +10 mA ($+V_g$) and −10 mA ($-V_g$) after annealing at different temperatures. For the $+V_g$ injection, samples annealed by RTA at lower temperature (750-850°C) have a smaller voltage shift than those annealed at higher temperature (950-1050°C). We attribute this result to the rugged interface between polyoxide/poly-1 that, apparently, forms a larger conducting area and a higher local current density, therefore inducing a higher trapping of electrons. In contrast, this is quite different for samples under $-V_g$ injection. It can be seen that the voltage shift is decreased as the temperature of RTA N_2O annealing is increased. This discrepancy may be attributed to the two-layer polyoxide film and/or the incorporation of nitrogen in the TEOS polyoxide. In this work, the thickness of N_2O-induced thermal polyoxide was around 1-4 nm. Under $+V_g$ injections, the electrons are injected into the polyoxide from the polyoxide/poly-1 interface. The leakage current is reduced because of high quality N_2O thermal polyoxides after high temperature N_2O annealing. As temperature increases, the thickness of the N_2O polyoxide increases. But the increment of surface roughness also reduces the electron breakdown field and increases the electron trapping rate. Under $-V_g$ injection, the TEOS polyoxide near the poly-2/polyox-

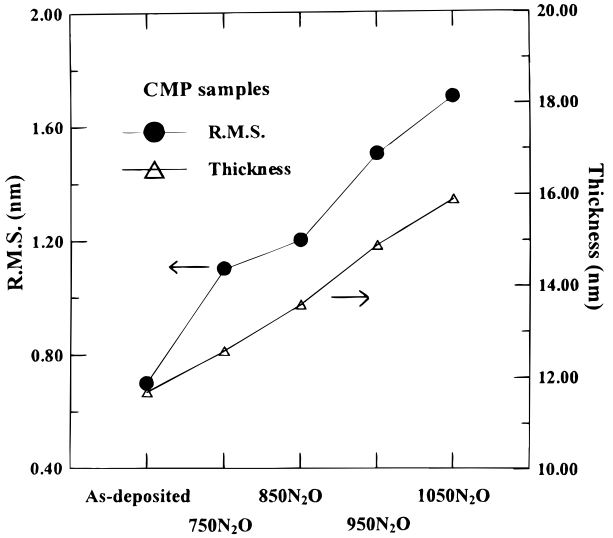

Figure 8. Thickness and roughness of CMP samples after different high temperature N_2O annealing.

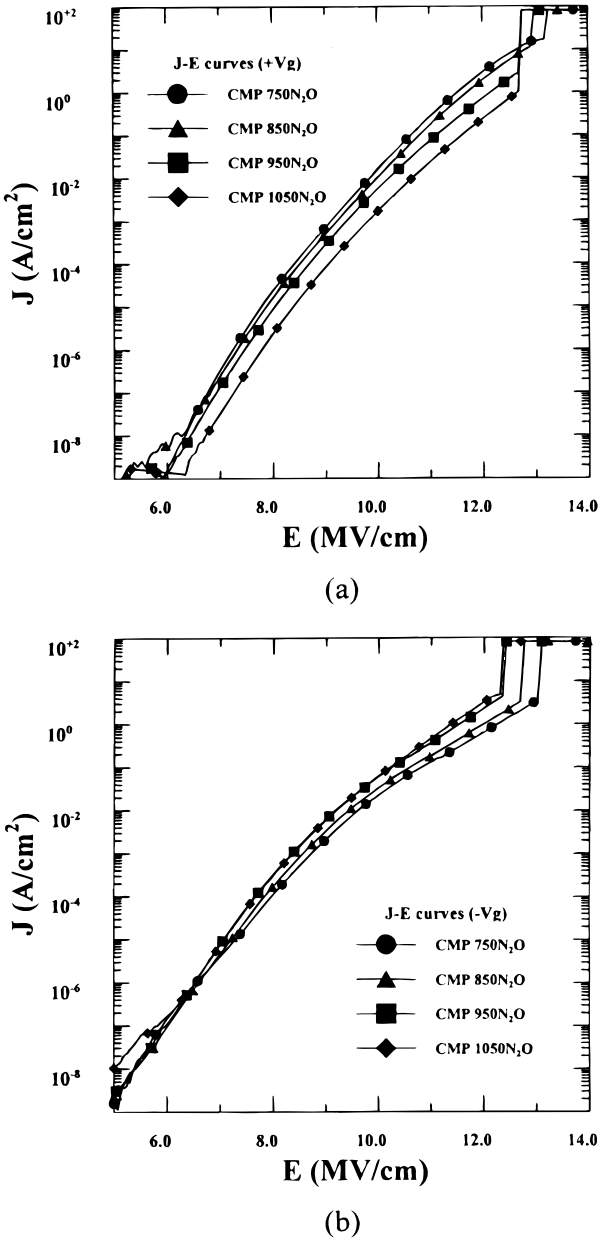

Figure 9. The *J-E* characteristics of TEOS polyoxides after different high temperature N_2O RTA annealing under (a) $+V_g$ injection, (b) $-V_g$ injection.

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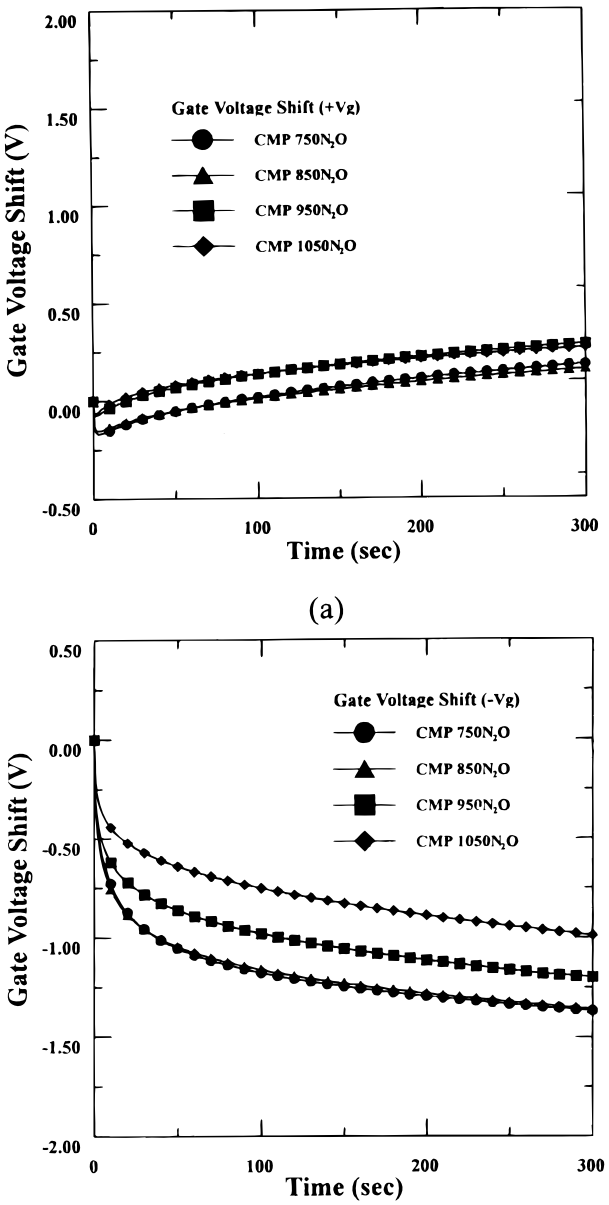

Figure 10. The charge trapping characteristics of TEOS polyoxides after different high temperature N_2O RTA annealing under (a) +10 mA/cm^2, (b) −10 mA/cm^2 constant current injection.

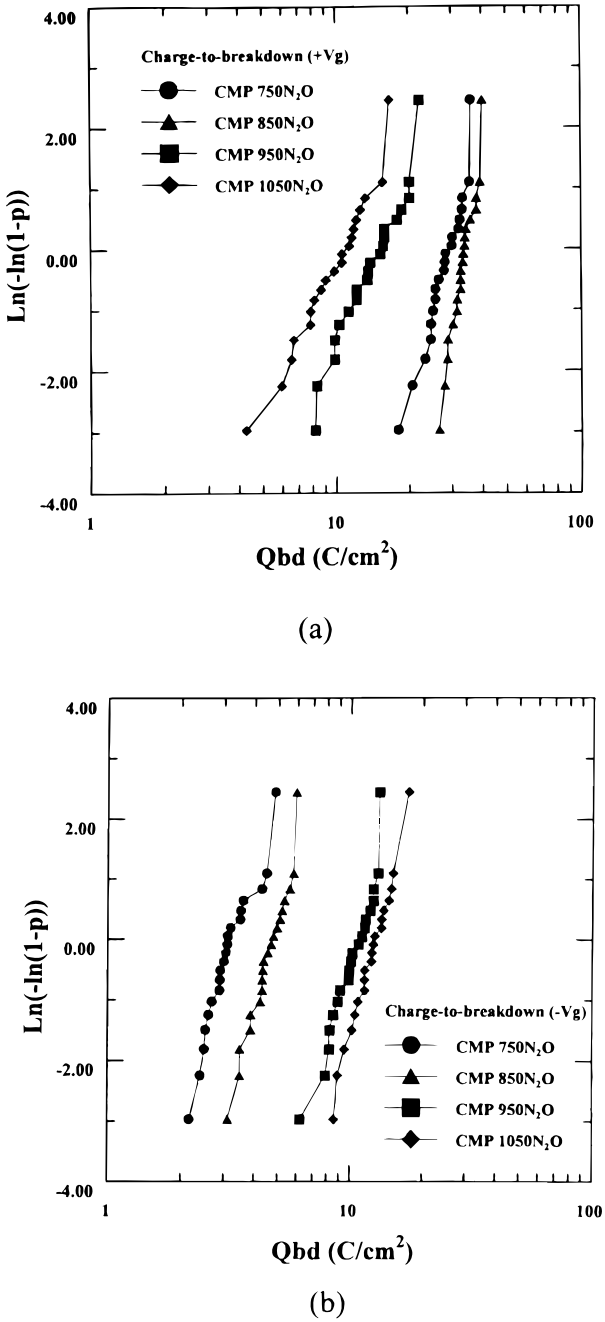

Figure 11. The Q_{bd} characteristics of TEOS polyoxides after different high temperature N_2O RTA annealing under (a) +10 mA/cm^2, (b) −10 mA/cm^2 constant current injection.

ide interface has a stronger effect than does the N_2O thermal polyoxide near the polyoxide/poly-1 interface in terms of influencing the electrical characteristics of the sample wafers. As the temperature of N_2O annealing is increased, the trapping rate of TEOS polyoxide reduces. This arises from the reduced growth of TEOS because of the competition with the growth of N_2O polyoxide, which makes the surface roughness of TEOS oxide the dominating factor for sample's electrical characteristics. So, the leakage current increases and the breakdown field reduces after high temperature annealing.

Figures 11a and b illustrate the Q_{bd} characteristics of these samples under +10 mA ($+V_g$) and under −10 mA ($-V_g$) gate injection. For the $+V_g$ injection, samples annealed at lower temperature (750-850°C) RTA have greater Q_{bd} than those annealed at higher temperature RTA (950-1050°C). It is, therefore, possible that a rougher polyoxide/polysilicon interface leads to a higher local current density plus a higher electron-trapping rate, subsequently causing smaller Q_{bd} values. Moreover, at a lower temperature annealing condition, 750-850°C, Q_{bd} can be increased further after another cycle of high temperature RTA annealing, but the reverse trend is found at the higher temperature annealing condition, 950-1050°C. This is quite different for samples under $-V_g$ injection. It can be seen that Q_{bd} is improved as the temperature of RTA N_2O annealing is increased. The largest Q_{bd} of polyoxide is obtained by 850°C RTA N_2O annealing for $+V_g$ injection and 1050°C RTA N_2O annealing for $-V_g$ injection. This matches with the trapping characteristics shown in Fig. 10a and b.

Conclusions

An adequately controlled CMP process not only improves the surface roughness of poly-1 but also improves the incorporation of nitrogen during the process of N_2O annealing at high temperature. The electrical characteristics of TEOS polyoxide are improved after high temperature N_2/N_2O annealing. Experimentally, the combination of high temperature N_2/N_2O annealing step and CMP results in

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an optimized process for TEOS polyoxide. In this work, we find that the increment of annealing temperature can cause the surface between TEOS polyoxide and poly-1 to become more rugged and the total thickness of polyoxide to grow thicker due to the increase of growth rate of polyoxide. Concurrently, the incorporation of N_2 is increased with increasing RTA temperature. As the result, this bilayer (TEOS deposited and thermally grown by RTA) polyoxide film may introduce an asymmetry of electrical leakage current, trapping characterization, and Q_{bd} for different polarity ($+V_g$ and $-V_g$) injection. Consequently, the optimized high temperature annealing process for TEOS polyoxide is acquired at 850°C using RTA N_2O annealing for $+V_g$ injection and at 1050°C using RTA N_2O annealing for $-V_g$ injection.

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