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The Effect of Copper on Gate Oxide Integrity

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We have studied the effect of copper contamination after the front-end metal-oxide-semiconductor capacitor fabrication on gate oxide integrity. The significant effect of Cu contamination on the pretunneling current, in combination with insensitive dependence of the Fowler-Nordheim tunneling current, oxide charge density, and breakdown field on the Cu concentration, suggests that the current leakage mechanism may be due to neutral traps generated by Cu inside oxide. In addition to pretunneling oxide leakage, a small amount of Cu contamination increases the interface trap density that may degrade the device performance.
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Copper (Cu) contamination[1-8] in Si complementary metal-oxide-semiconductor (CMOS) based devices has attracted much attention recently, because Cu may come from either the front-end or back-end process. It has been reported that Cu can affect the threshold voltage of MOS transistors,[1] and form precipitate or silicide at the Si/SiO_2 interface.[5,8] The oxide breakdown voltage is reduced under a condition of high contamination levels,[2,5,8] but, for slight contamination, significant electrical degradation only occurs at the field overlap edge[3] with little effect on the area gate oxide breakdown.[4,6,7] While most previous works have primarily focused on the front-end preoxidation Cu contamination, Cu contamination introduced by Cu interconnection processes, such as Cu electroplating and chemical mechanical polishing (CMP) becomes an important concern. In this article, we have examined the gate oxide integrity[9,10] of Cu-contaminated MOS capacitors, which received thermal treatment at 400°C after contamination. While the breakdown field and interface trap density deteriorate after Cu contamination, the degradation is insensitive to the Cu concentration of the contamination solution in the study. On the other hand, the strong dependence of the pretunneling leakage current on the contamination concentration is observed. The pretunneling current increases monotonically with the amount of Cu contamination and is very similar to stress-induced leakage current (SILC).[11-13] Electrical measurements suggest that the possible mechanism of the pretunneling current leakage is attributed to the generation of neutral traps by Cu contamination.

Experimental

Four-inch, p-type Si(100) wafers with a resistivity of 10 Ω-cm were used in this study. The wafers were cleaned in a 3:1 solution of H_2SO_4 and H_2O_2, a high purity deionized water rinse, an RCA clean, a 1% HF etch, and a final deionized water rinse. After the growth and patterning of the 3000 Å field oxide, gate oxides of 50 Å in thickness were grown by dry oxygen at 900°C. A 3000 Å thick poly-Si was deposited on the gate oxide with subsequent n-type doping using phosphorus. The standard aluminum contact was formed by sputtering, and MOS capacitors of 100 × 100 μm were fabricated. Therefore, the fabricated device structure is 5000 Å Al/3000 Å poly-Si/50 Å gate oxide/Si substrate. Cu was introduced by immersing devices into a $CuSO_4$ solution for 60 s. Cu concentration of 10 ppb and 10 ppm were used in this study. The contaminated MOS capacitor was further annealed at 400°C for 0.5 h (10 ppb contamination) or 1 h (10 ppm contamination) in a nitrogen gas ambient.

Results and Discussion

Figures 1a and b show the current density-voltage (J-V) characteristics and the accumulative distribution, respectively. Although no effect of Cu contamination concentration on the Fowler-Nordheim (F-N) tunneling current can be found, strong pretunneling current dependence on the Cu contamination is observed. The phenomena of increasing the pretunneling current without changing the F-N tunneling current is very similar to SILC effect of gate oxides. The leakage current in the pretunneling region is attributed to trap-assisted tunneling that saturates or becomes incomparable to F-N tunneling at higher gate bias. Furthermore, a monotonic increase of the pretunneling current with increasing the Cu concentration was measured. This effect is similar to SILC, in which a higher leakage cur-

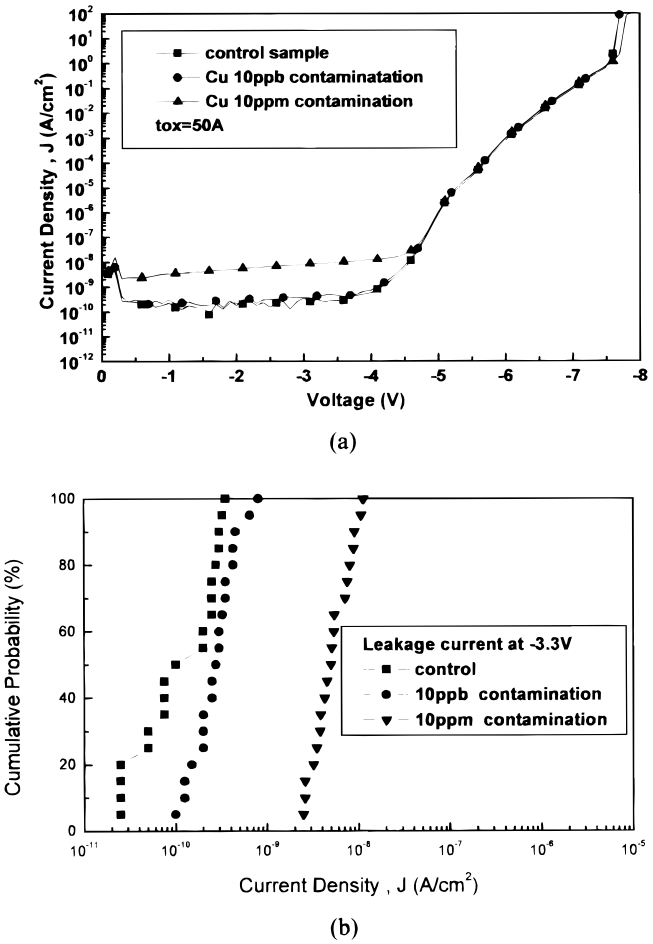

Figure 1. (a) The leakage current density for various copper contamination. (b) Current density distribution for various copper contamination at −3.3 V bias. The contamination is performed by contacting the devices with 10 ppb or 10 ppm $CuSO_4$ solution for 60 s and annealing at 400°C for 0.5 h (10 ppb contamination) or 1 h (10 ppm contamination) in N_2 ambient.

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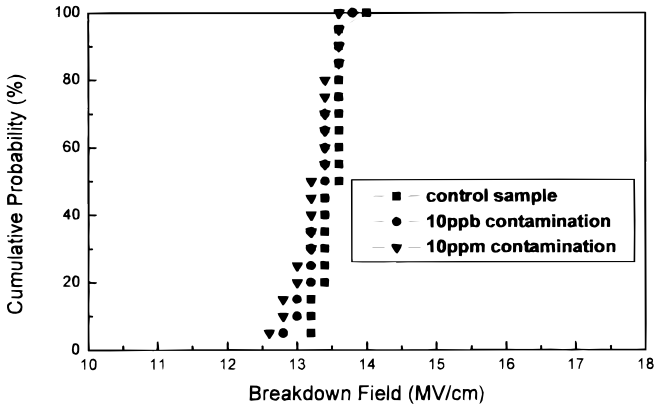

Figure 2. Gate oxide breakdown electric field distribution.

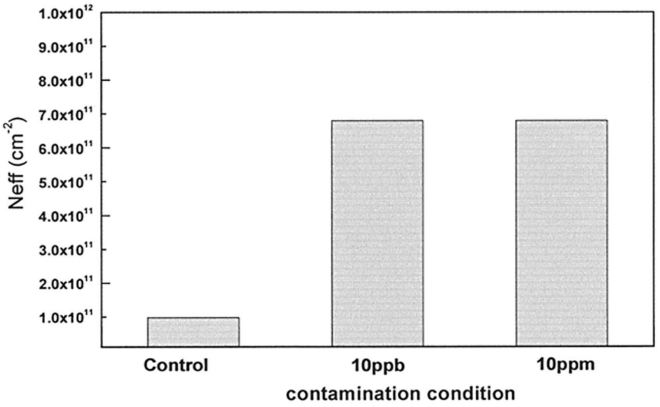

Figure 4. Oxide charges comparison among different contaminated conditions.

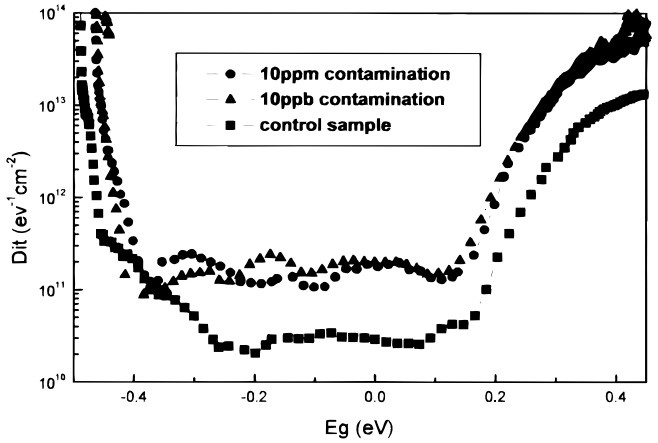

Figure 3. Interface trap density for various copper contamination.

rent may be induced with a higher oxide trap generation under a stronger or longer stress condition.[11-13]

To further examine the effect of Cu contamination on gate oxide integrity, we have measured the breakdown field of the gate oxide as a function of the Cu concentration of the contaminant solution. As shown in Fig. 2, Cu contamination has no obvious effect on the oxide breakdown field. This may be due to a small amount of Cu generating traps inside the oxide and is similar to preoxidation Cu contamination reported previously.[4,6,7] It is important to note that the weak dependence of the breakdown field on the Cu concentration, in combination with a strong relationship between the measured pretunneling current and the Cu concentration, is also consistent with SILC, where no hard breakdown field degradation occurs.[9-13]

The interface trap density derived from the C-V measurement is shown in Fig. 3. A low interface trap density of 3×10^{10} eV^{-1}/cm^2 is measured for the control sample that is typical for thermal oxides. After Cu contamination, the interface trap density increases. This is attributed to the presence of Cu precipitation at the interface between the Si substrate and the gate oxide.[5] According to Fig. 3, the interface trap density seems not to have an obvious dependence on the Cu concentration. Since the interface trap density is strongly related to the low frequency transistor noise, the increased interface trap density can degrade the device performance to an unacceptable state for ultralarge scale integrated (ULSI) applications.

The oxide charge density as a function of the Cu contamination is shown in Fig. 4. Although the oxide charge density is higher for the contaminated device than for the control sample, there is no noticeable dependence of oxide charge density on the Cu concentration. Therefore, the higher leakage current observed in Fig. 1 is not due to the oxide charge. It is reported that SILC may be due to neutral traps formed by hole injection into the oxide.[12,13] The negligible dependence of the oxide charge density on the Cu concentration also suggests that neutral traps formed by Cu inside the oxide matrix may be responsible for the higher pretunneling leakage current. The reason why such effect is not observed in the preoxidation contamination may be due to different mechanisms. Cu can be oxidized to form Cu oxide and join the SiO_2 matrix in preoxidation contamination, while in the present paper elemental Cu or the Cu ion is present inside the SiO_2 matrix instead of the Cu oxide form.

Conclusions

We have studied the effect of Cu contamination on gate oxide integrity after front-end MOS capacitor fabrication. The strong dependence of pretunneling current on the Cu concentration, in combination with insensitive F-N tunneling current, oxide charge density, and breakdown field to the Cu contamination level, suggests that the mechanism may be due to neutral traps generated by Cu inside the oxide.

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