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A 1.2-V Operation Power Pseudomorphic High Electron Mobility Transistor for Personal Handy Phone Handset Application

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A 1.2 V GaAs power pseudomorphic high electron mobility transistors (PHEMT's) for personal handy phone system (PHS) handset application was developed. The power PHEMT has a dual delta doped AlGaAs/InGaAs/GaAs based structure with compact device layout. The 6.72 mm device exhibits maximum power added efficiency (PAE) of 43.62% at 1.2 V drain bias with an output power of 22.18 dBm. Under 1.9 GHz $\pi/4$-shifted quadrature phase shift keying (QPSK) modulated PHS signal, the device shows an adjacent channel leakage power (P_{adj}) of -56.86 dBc at 600 kHz apart from the center frequency and a linear efficiency of 41.31%. This is the first report on the 1.2-V operation power PHEMT for PHS handset application so far.

KEYWORDS: PHS, low voltage handset application, GaAs, power PHEMT

1. Introduction

Digital wireless communication system has become more and more popular in recent years due to it's capability for voice and data communication. To meet the system requirements, many efforts were made to develop high power density, high efficiency, and low distortion devices for the system applications. GaAs based devices such as metal-semiconductor field-effect transistors (MESFET's)[1,2] and pseudomorphic high electron mobility transistors (PHEMT's)[3,4] and heterojunction bipolar transistors (HBT's)[5,6] with outstanding performance have been demonstrated for digital wireless communication applications. Recently, 1.9 GHz Japanese personal handy phone system (PHS)[7–12] has been introduced to more than 10 countries due to its capability for both voice and data communication. The PHS handsets require the power devices have low operating voltage, high power added efficiency (PAE) and low adjacent channel leakage power (P_{adj}) in order to carry high bit rate voice and data communication and to decrease the number of the battery cells used to make the handset smaller and lighter. However, operation at low bias voltage generally causes poorer linearity and power efficiency for the power devices if the devices were not properly designed.

In recent years, several works on 1.9 GHz low voltage operation PHS power devices have been reported.[7–12] In Kunihisa's work,[7] a 3.0 V biased PHEMT with PAE of 41.7% and an output power of 22 dBm at a quiescent current of 127 mA was demonstrated. In Nagaoka's work,[8] a 2-V operation power MESFET with power added efficiency of 38.5% and output power of 21.0 dBm with a quiescent current of 162.9 mA was attained.

In this work, 1.2-V operation PHEMT's for PHS application were developed. Under 1.9 GHz PHS standards and 1.2 V drain bias, the device shows a P_{adj} of -56.86 dBc at 600 kHz apart from 1.9 GHz with PAE of 41.31% at an output power of 22 dBm and the quiescent drain current is 100 mA. This is the first 1.2 V operation power PHEMT reported. The excellent performance of the device is due to the use of dual delta-doped pseudomorphic AlGaAs/InGaAs/GaAs structure and the use of compact device layout.

2. Device Structure and Fabrication

Dual delta-doped AlGaAs/InGaAs/GaAs pseudomorphic structure was used in this study to achieve high transconductance and high power density at low voltage operation. Figure 1 shows the structure of the device used. The epitaxial layers of the device were grown by molecular beam epitaxy (MBE) on a 3-inch (100)-oriented semi-insulating GaAs substrate. As shown in Fig. 1, the undoped InGaAs channel layer is sandwiched between an upper 35 Å and a lower 40 Å undoped AlGaAs spacer layer. Below the lower silicon delta doping layer, there is a 10-period of AlGaAs/GaAs supperlattice to suppress the substrate leakage current and reduce the output conductance. The two dimensional electron gas (2-DEG) formed in the InGaAs quantum well is from the upper and lower delta doping layers. The two delta-doping layers are with doping levels of 5×10^{12}/cm^2 and 3×10^{12}/cm^2, respectively. This achieves high current density and high transconductance requirements for low voltage operation device. A heavily silicon doping capping layer is on the top to provide good ohmic contacts and reduce the source resistance.

The size of the device layout was also reduced to further decrease the source resistance and improve the performance of the device for low voltage operation. Interdigitated configuration was used to reduce the device area and a tight source to drain spacing was used to reduce the source resistance. The device size is $300 \times 580\,\mu$m^2. The source to drain spac-

Material	Layer	Thickness
N+ GaAs	Cap Layer	40 nm
i AlGaAs	Atomic Doping Layer	30 nm
i AlGaAs	Upper Spacer	3.5 nm
i InGaAs	Conducting Channel	10 nm
i GaAs	Lower Spacer	4 nm
i AlGaAs	Atomic Doping Layer	25 nm
IGaAs		55 nm
AlGaAs/GaAs	Superlattice	
iGaAs	Buffer Layer	
	S. I. GaAs Substrate	

Fig. 1. The epitaxial structure of the AlGaAs/InGaAs/GaAs PHEMT.

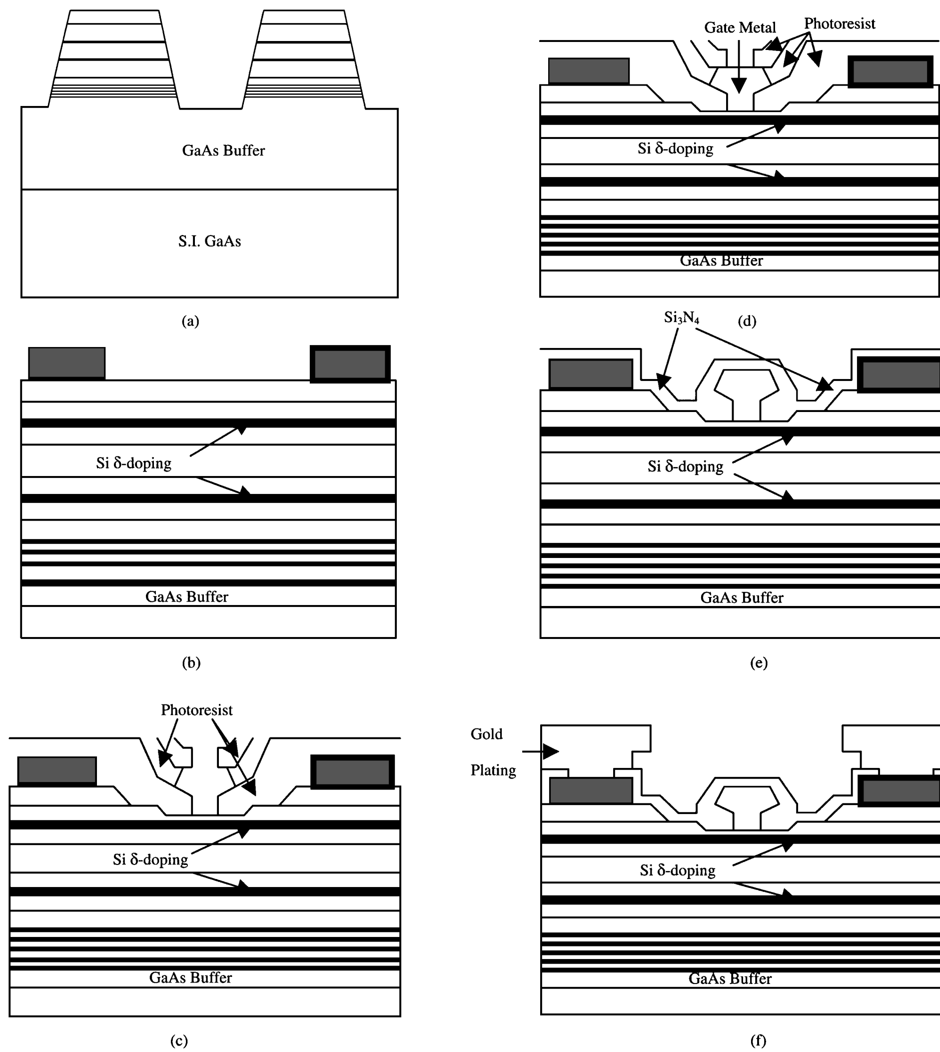

Fig. 2. Schematic process flow of the GaAs power HEMT. (a) Mesa isolation. (b) Ohmic metallization. (c) Gate recess. (d) Gate formation. (e) Device passivation by Si_3N_4. (f) The complete GaAs power HEMT with airbridge.

ing is 4 μm. The developed PHEMT's have a gate width of 6.72 mm with 120 μm-wide fingers. The gate length of the device is 0.5 μm. Different device sizes from 3 mm to 6.72 mm were evaluated. The 6.72 mm device gives best efficiency performance at same output power level due to large periphery. Figure 2 shows the process flow of the PHEMT's in this study. In Fig. 2(a), the mesa isolation was done by wet etching using HF based solution. Figure 2(b) shows the ohmic metal contacts of the device. The compositions of the ohmic contacts were Au/Ge/Ni. The ohmic metal was deposited by electron-beam evaporation and followed by rapid thermal annealing (RTA) at 300°C for 10 seconds. The gate was formed by deep UV lithography. A tri-layer photoresists system was used to obtain T-shaped gate. Before gate metal deposition, gate recess was performed to increase breakdown voltage as shown in Fig. 2(c). The gate metal was deposited by electron-beam evaporation, as shown in Fig. 2(d). The gate metal used was Ti/Pt/Au. In Fig. 2(e), silicon nitride was used for device passivation and was deposited by plasma enhanced chemical vapor deposition (PECVD). In Fig. 2(f), gold-plated airbridges were formed for electrode connections. Finally, the wafer was thinned to 4mil thick and the fabrication of the power PHEMT's was completed.

3. Device Performance

The DC and RF characteristics of the finished PHEMT's were measured. The pinch-off voltage is -1.1 V. The breakdown voltage defined at a drain to gate current density of 100 μA/mm is around 11 V. Figure 3 shows the I–V curve of the device with different gate bias voltages. The saturation

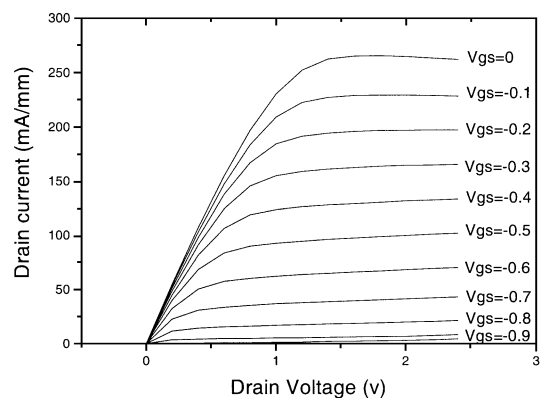

Fig. 3. The I–V characteristics of the PHEMT with gate bias voltage from 0 V to pinch-off.

drain to source current (I_{dss}) is 265 mA/mm. The maximum transconductance measured at $V_{ds} = 2$ V is 354 mS/mm. At low drain bias voltage, the transconductance of the PHEMT is also high. Figure 4 shows the transconductance of the PHEMT at 1.2 V drain bias voltage. This demonstrated the device is suitable for low voltage operation. Both the high current density and high transconductance were attributed to the optimized dual delta-doped heterojunction structure and the device layout.

The manufactured 6.72-mm-wide GaAs power PHEMT was tested at a frequency of 1.9 GHz and under a drain bias of 1.2 V. The device was operated at class AB condition with a quiescent drain current of 100 mA. Figure 5 shows the output power, PAE and power gain as a function of the input power for the device. The optimum load impedance is 4.85-j7.03 Ω and source impedance is 4.23-j2.09 Ω. The PHEMT exhibits a maximum PAE of 43.62% with an output power level of 22.18 dBm and a gain of 6.68 dB. The linear gain of the device was 11.78 dB and output power at 1-dB compression was 18.81 dBm with a PAE of 31.37%.

The device also has an excellent performance under $\pi/4$-shifted quadrature phase shift keying (QPSK) modulated PHS standard signal. The center frequency of the input PHS signal is 1.9 GHz. Figure 6 shows the device power performance and distortion characteristics under different drain bias at 2.4 V and 1.2 V with constant 100 mA quiescent drain current. The device meets the specifications of PHS applica-

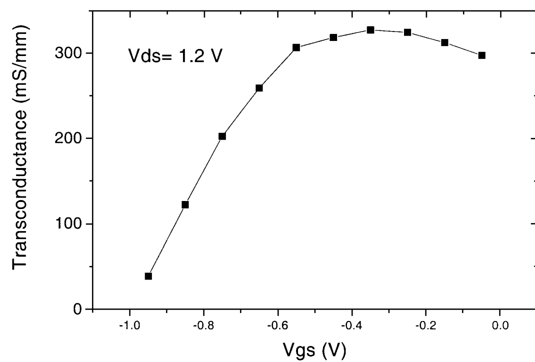

Fig. 4. Tansconductance of the device as a function of gate bias voltage V_{gs} at $V_{ds} = 1.2$ V.

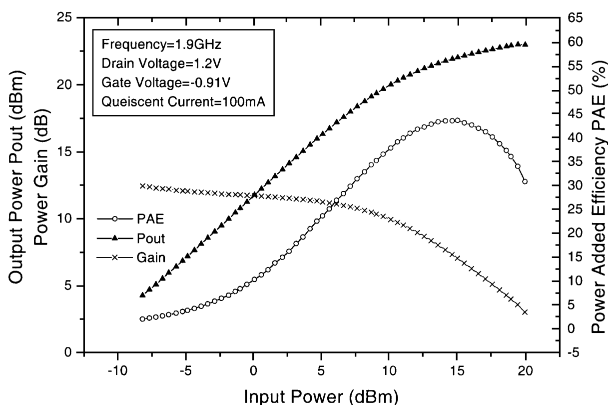

Fig. 5. Output power, power-added efficiency and power gain as a function of input power for the PHEMT at $V_{ds} = 1.2$ V and at a frequency of 1.9 GHz.

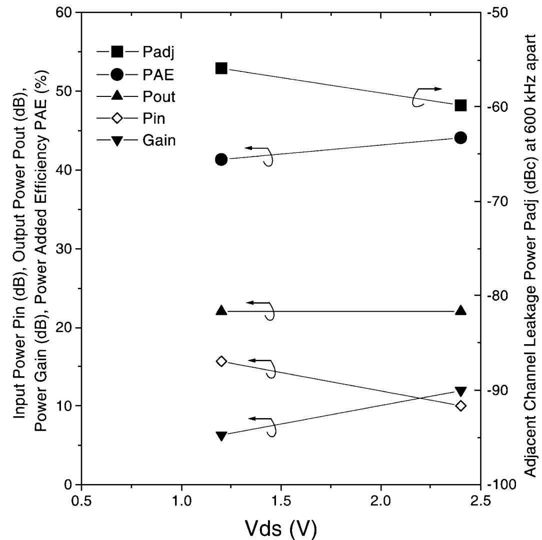

Fig. 6. Output power, power-added efficiency, power gain and adjacent channel leakage power under 1.2 V and 2.4 V drain bias and with constant 100 mA quiescent drain current.

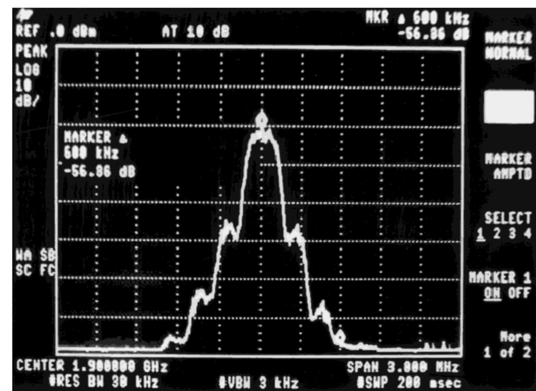

Fig. 7. Adjacent channel leakage power spectrum under 1.9 GHz PHS signal for the PHEMT at $V_{ds} = 1.2$ V.

tion with drain bias voltage of 2.4 V and 1.2 V. Under low drain bias of 1.2 V and with a low quiescent drain current of 100 mA, the device has high PAE and low distortion. When output power equals to 22 dBm, the device shows an P_{adj} of −56.86 dBc at 600 kHz apart from the 1.9 GHz center frequency. The power gain at this point is 6.3 dB, and linear PAE is 41.31%. Figure 7 is the P_{adj} spectrum for the device under $\pi/4$-shifted QPSK modulated PHS standard signal. The measured results demonstrated that the 6.72-mm PHEMT meets the PHS specifications and can be used for 1.9 GHz 1.2 V PHS handset application with excellent performance.

4. Conclusions

A 1.2-V very low voltage operational PHEMT device was developed. The device with dual delta-doped AlGaAs/InGaAs/GaAs structure shows high drain current density and high transconductance. The size of the device layout was optimized to decrease the source resistance and improve the performance of the device for low voltage applications. When tested under 1.9 GHz and at 1.2 V drain bias, the device provided maximum PAE of 43.62% with an output power of 22 dBm. When tested at 1.2 V drain bias and under

1.9 GHz π/4-shifted QPSK modulated PHS signal, the device shows an output power of 22 dBm with an P_{adj} of −56.86 dBc at 600 kHz apart from 1.9 GHz and the linear PAE is 41.31%. This is the first report on the 1.2-V operation power PHEMT for PHS application. The device developed should also be applicable for other digital wireless communication systems.

Acknowledgement

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