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Copper voids improvement for the copper dual damascene interconnection process

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Abstract

The mechanism of copper (Cu) voids formation from electro-chemical plating (ECP) followed by Cu chemical mechanical polishing (CMP) are studied in Cu dual-damascene interconnection. The formation of Cu voids at metal lines is the main problem that causes not only the failure of via-induced metal-island corrosion but also yield loss. The galvanic theory and Cu lifting mechanism are proposed to explain the dependence of Cu-void performance on the Cu grain size and the benzotriazole (BTA, $C_6H_5N_3$) flow rates. In the integration process of Cu interconnects, it is found that the smaller Cu grain size in ECP conditions and less BTA flow rate in CMP processes cannot only reduce the number of Cu voids but also improve the wafer yield.
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1. Introduction

Copper (Cu) has been applied in sub 0.13 μm semiconductor metallization processes because of its low resistivity and better reliability [1–4]. Actually, the Cu interconnection is fabricated by a dual-damascene process that includes via/trench etching, deposition of tantalum nitride (TaN_x) and Cu seed layer, Cu electro-chemical plating (ECP), and Cu chemical mechanical polishing (CMP). A high-yield approach requires a defect-free Cu film after the formation of metal/via. However, some crucial defects such as Cu voids and pits are always present after the Cu-CMP process because the Cu metal is easily corroded.

Guldi et al. [5] have showed that Cu pits and voids could be observed using an electron-beam inspection tool. Lu et al. [6] have reported that the Cu voids with a swirl-distributed map were caused by ECP and associated with surface organic contamination. Pre-ECP rinsing could effectively remove the surface organic contamination, then improve the wettability of a seed layer and eliminate the swirl defects. Reid et al. [7] have ascribed the formation of the Cu voids to factors such as Cu seed layer coverage, plating waveform (DC, reversed-pulse), and additive chemistry formulation. Alers et al. [8] have revealed that the Cu line voids after Cu CMP will influence electromigration (EM) resistance. Song et al. [9] have reported that the Cu micro voids were generated during the ECP process and subsequent annealing process resulting in yield loss. Wrschka et al. [10] have demonstrated that adding a passivating agent in a CMP process could prevent the formation of corrosion-induced defects. Kondo et al. [11,12] have revealed the presence of galvanic corrosion which occurred when electrochemically different materials are electrically connected and immersed into a slurry during Cu CMP.

From this brief review, it can be seen that there is no clear understanding on the routes of Cu voids during the via-formation process that includes via etching, trench etching, barrier/seed layer depositions, and ECP/CMP processes. In our previous work [13], the Cu voids at the via bottom were the major factors resulting in the failure of stress migration and EM testing.

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Eliminating the metal voids in the metal lines reduces via induced metal island corrosion and improves yield. In this present work, the mechanism of the formation of Cu voids of the dual-damascene interconnections was investigated. The way of weak-point in current Cu interconnection processes is also addressed precisely.

2. Experiment

A Cu interconnection was fabricated by 0.13 μm technology using cobalt-salicide process, dielectric deposition with fluorosilicate glass, an etching stop layer with silicon nitride and Cu dual-damascene process. A via structure consisted of metal chains and via holes is shown in Fig. 1. A stacked film containing a 15-nm-thick tantalum nitride/tantalum (TaN_x/Ta) layer, a Cu seed layer, and an ECP-Cu film was used in the via fabrication of the dual-damascene process. Cu grain size and CMP polishing conditions were varied to evaluate their effects on the

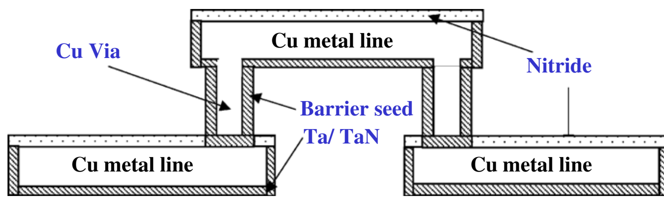

Fig. 1. Dual damascene via scheme with TaN_x as a barrier and Cu as a metal material.

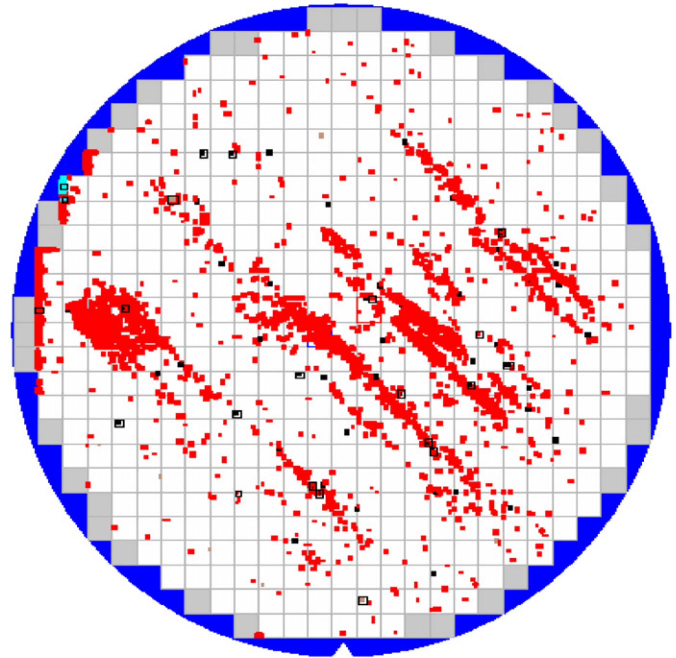

Fig. 3. In-line KLA-Tencor defect-scanning tool can be the methodology for metal Cu voids captures.

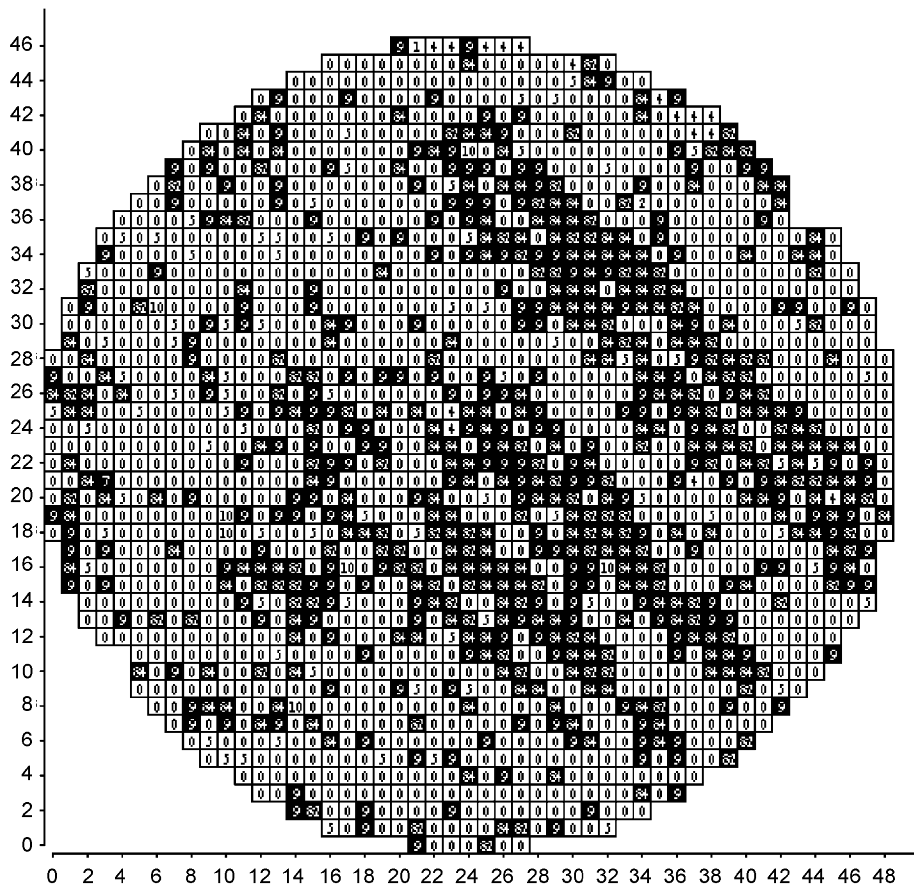

Fig. 2. Bin map corresponding to the yield loss after bin function evaluating and testing at the room temperature (25 °C).

formation of Cu voids. Cu grain size was varied from 0.64 to 0.83 μm by reducing 20% plating current.

After the Cu-CMP process, defect maps of test wafers were obtained using a KLA-Tencor defect-scanning tool. Samples for wafer-yield testing were examined using a bin function evaluation at room temperature without any package processes. Cu voids and grains were also observed by focus ion beam (FIB), scanning electron microscopy (SEM) and transmission electron microscopy (TEM). In addition, the chemical analysis was examined using energy dispersive X-ray spectroscopy (EDX).

3. Results and discussion

The wafer underwent bin function testing at room temperature on the wafer testing level and the bin map corresponding to the yield loss is shown in Fig. 2. We can see that the yield loss (black part) mainly occurs at wafer center with a special map (fallout around the wafer center). Fig. 3 displays the defect map measured from the in-line defect-scanning tool KLA. The cross-sectional TEM image shows that the defect is a Cu void at via bottom at the failure site, as shown in Fig. 4. The defect map of the Cu void is nearly the same as the yield-loss map. Therefore, it is suspected that the yield loss results from the Cu-void defects. The defect inspection after step-by-step checking reveals that the Cu voids clearly appeared after the metal Cu CMP processes as shown in Figs. 5–7. Furthermore, the voids were generated at the grain boundaries of Cu grains and the cap nitride layer neither caved in nor collapsed above the metal/Cu void in Fig. 7. The EDX analysis shows the presence of oxygen signal in the Cu voids

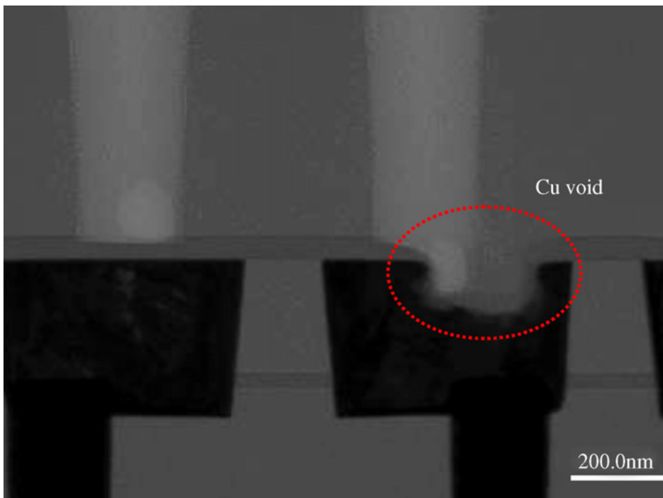

Fig. 4. TEM cross-sectional profile of failure analysis shows Cu voids are the root cause of the yield killing.

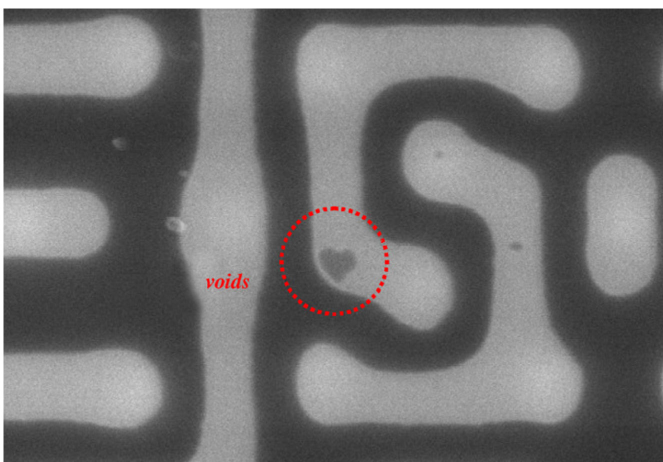

Fig. 5. Top-view SEM shows the metal Cu voids.

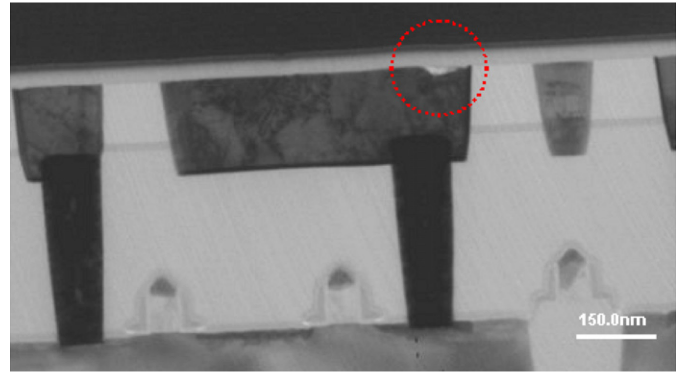

Fig. 6. Cross-sectional TEM showed the Cu voids caused metal voids.

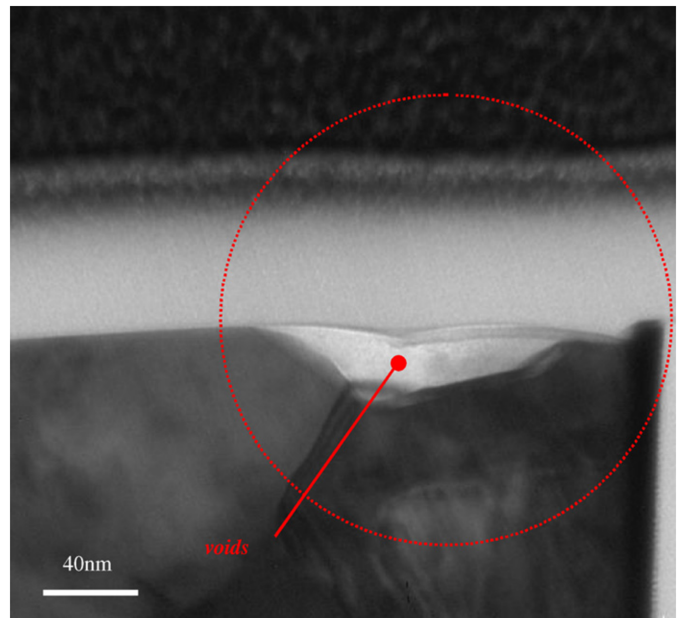

Fig. 7. Cross-sectional TEM showed the cap nitride layer neither caved in nor collapse above the metal/Cu voids.

revealing that the Cu oxidation is formed at the grain boundary as shown in Fig. 8. The Cu oxidation will result in higher metal resistance and the yield loss in the bin function test.

Inhibition of Cu corrosion is very important for Cu metallization process. Generally, benzotriazole (BTA, $C_6H_5N_3$) is used as the corrosion inhibitor mixed with CMP slurries [14,15]. BTA forms stable coordination compounds with Cu as shown in Fig. 9. The BTA inhibitor used in the CMP process is crucial to the formation of Cu interconnection. Therefore, the texture evolution of the wafers with various Cu grain sizes from 0.64 to 0.83 μm were studied at BTA flow rates of 100, 300, and 500 ml/min to investigate the effect of BTA and/or BTA derivatives on the formation of Cu voids. The different Cu grain sizes from various Cu-ECP process conditions are shown in Fig. 10(a)–(d). In this present work, the Cu grain size is measured and counted by averaging all grains along two diagonal lines on SEM images. Table 1 shows that the extent to which the number of Cu voids depends on the Cu grain size and the BTA flow rate. Larger grains and higher BTA flow rate are associated with more Cu voids. The vacancies between Cu grains are formed after the Cu-ECP process. Larger copper grains are associated with the

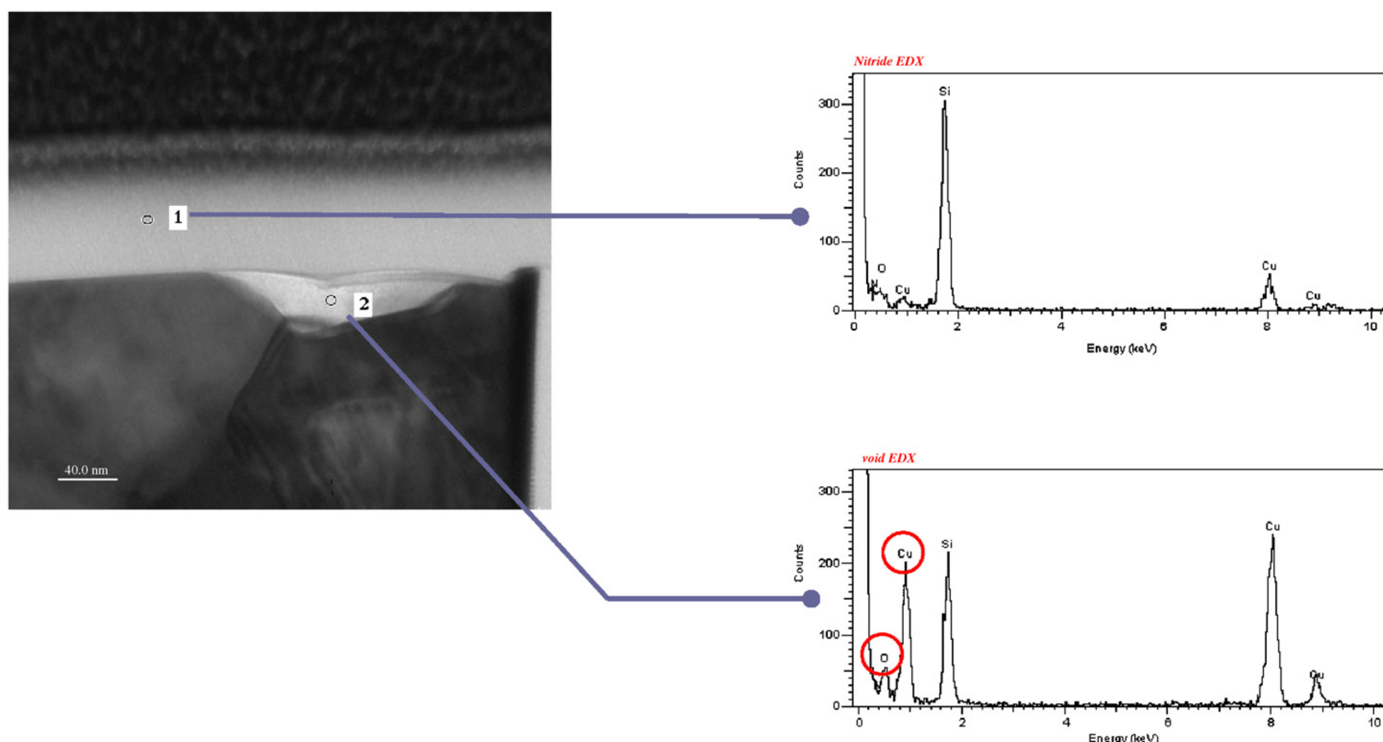

Fig. 8. EDX analysis of Cu void with oxygen material reveals the Cu oxidation formation at the grain boundary.

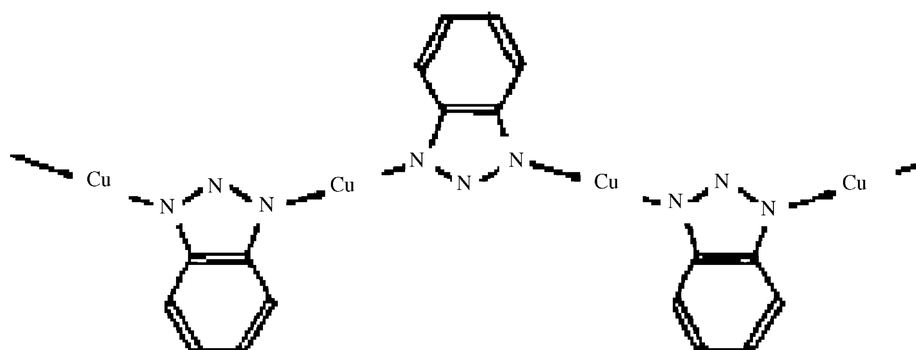

Fig. 9. Average Cu grain sizes from different Cu electro-chemical plating (ECP) process conditions are: (a) 0.64 mm; (b) 0.69 mm; (c) 0.75 mm and (d) 0.83 mm.

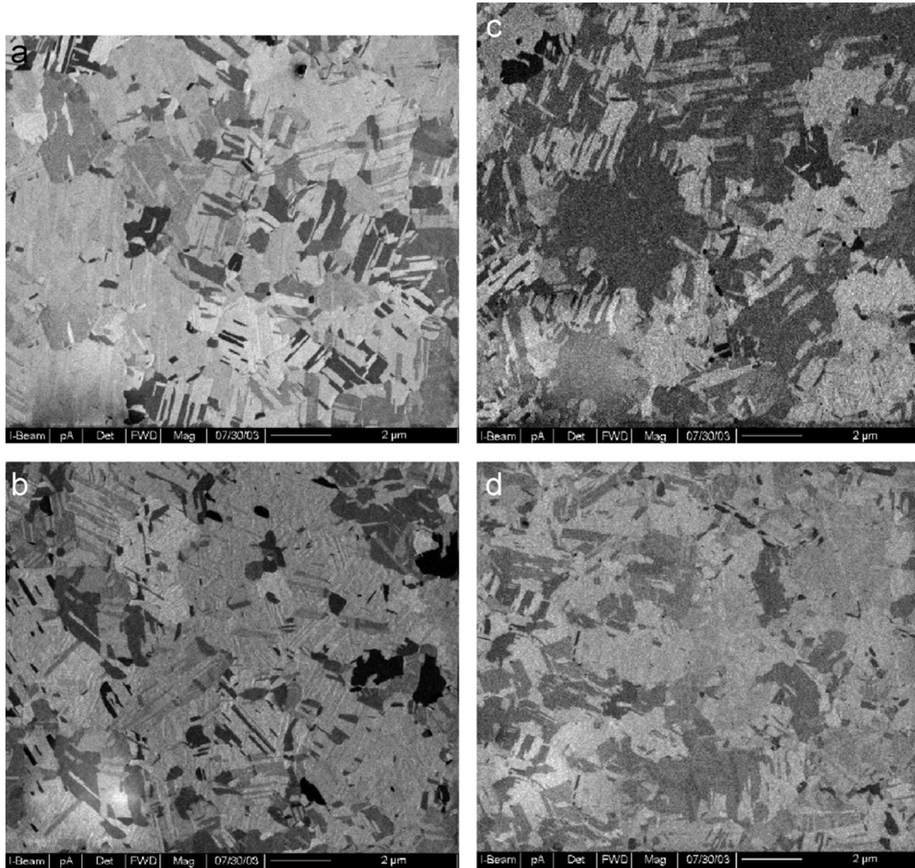

Fig. 10. BTA forms stable compound with Cu and this thin polymeric film protect Cu surface from corrosion.

Table 1
The extent to the copper voids depends on copper grain size and BTA flow rate

BTA flow rate (mL/min)	Cu grain size			
	0.64 μm	0.69 μm	0.75 μm	0.83 μm
100	Free	Free	Low	Medium
300	Free	Low	Medium	Severe
500	Low	Medium	Severe	Severe

formation of larger vacancies due to larger tensile stress. As a result, the performance of corrosion or void is worse for the Cu film with a larger grain size due to more corrosive for tensile Cu films. The study elucidates that the content of the CMP processes is critical to the formation of Cu voids. The BTA inhibitor is necessary for the prevention of Cu oxidation in the Cu-CMP process. However, too much BTA used in the Cu-CMP process will cause Cu-void formation. Undoubtedly, the defect level could be truly improved by less BTA flow rate in the CMP process.

The galvanic corrosion occurs when electrochemically different materials are electrically connected and immersed into an electrolyte [11,12]. The mechanism of void formation is related to galvanic corrosion. In this study, the galvanic theory and Cu lifting mechanism are proposed to explain this dependence of Cu-void performance on the size of Cu grains and the BTA flow rate as shown in Fig. 11(a) and (b). The vacancies between Cu grains are formed after the Cu-ECP process. Larger Cu grains are associated with the formation of more vacancies. There is an electrochemically potential difference between the small grains and the large grains. As a result, the performance of corrosion or void is worse for the Cu films with a larger grain size. In addition, the BTA or BTA derivatives will react with Cu to form BTA–Cu bonds, which change the electrochemical potential of Cu grains, then enhancing Cu corrosion.

4. Conclusion

This work explores the influence of Cu grain size and the quantity of BTA in the Cu-CMP slurry on the extent of the Cu voids. The optimization of the BTA content in the Cu-CMP slurry is critical to the continuous improvement of process integration on the elimination of Cu voids, especially beyond 0.13 μm technology. In the process integration of Cu interconnects, the suitable Cu grain size in ECP conditions, and less BTA flow rate in CMP processes can not only eliminate voids but also improve yield.

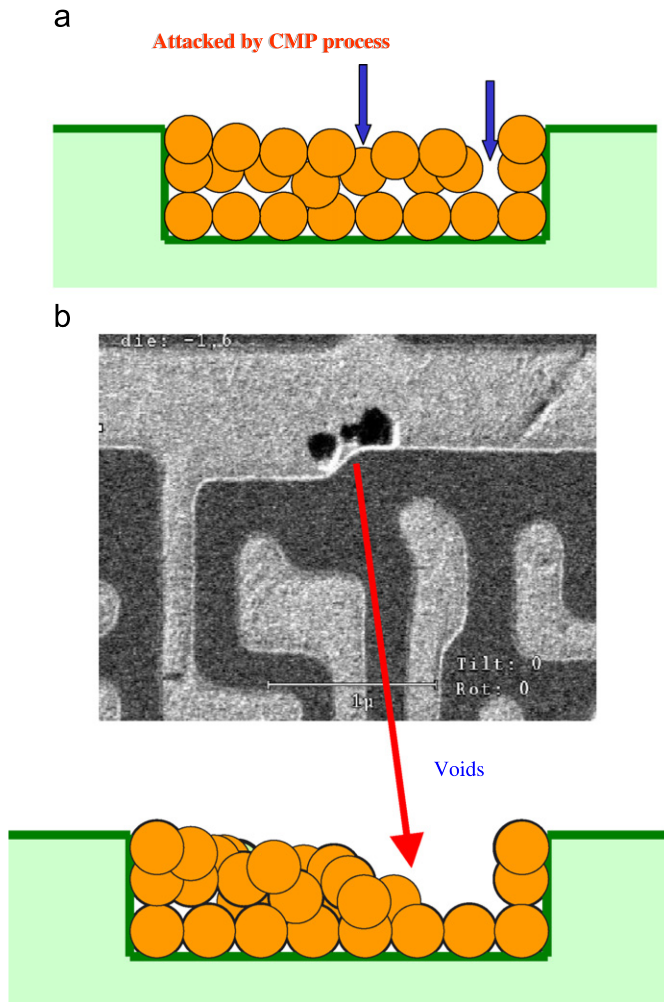

Fig. 11. Lifting theory briefly indicates the main mechanism of the correlation of Cu grain size, voids formation during (a) CMP process and (b) post-CMP process.

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