Fabrication of Very High Resistivity Si with Low Loss and Cross Talk

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***Abstract*—We have used proton and As$^+$ implantation to increase the resistivity of conventional Si (10 Ω-cm) and Si-on-quartz substrates, respectively. High resistivity of 1.6 MΩ-cm is measured that is close to intrinsic Si and semi-insulating GaAs. Very low loss and cross coupling of 6.3 dB/cm and −79 dB/cm (10 μm gap) at 20 GHz are measured on these samples, respectively. The very high resistivity and improved rf performance are due to the extremely fast ~1 ps carrier lifetime stable even after a 400 °C annealing for 1 h. Little negative effect on gate oxide integrity is also observed as evidenced by the comparable stress-induced leakage current and charge-to-breakdown for 30 Å oxides.**

***Index Terms*—Cross talk, high resistivity Si, RF loss.**

I. Introduction

In spite of the rapid tec hnology evolution for Si rf transistors [1]–[5], the most important issue to realize high performance MMIC is the passive transmission line loss due to much lower substrate resistivity compared to semi-insulating GaAs [6]–[9]. The low resistivity (10 Ω-cm) results in substantial energy loss and dielectric attenuation that impose a severe limitation on transmission lines and inductors at rf frequency. Although high resistivity Si (1–10 kΩ-cm) [10]–[14] has been studied, the loss is still relatively high due to limited resistivity as compared with GaAs. Further, few papers have mentioned the low resistivity related cross coupling that is important for low-noise and power device integration and mixed signal IC. In this work, we have studied both transmission line loss and cross coupling on our developed extremely high resistivity Si of 10 K-1 MΩ-cm fabricated by ion implantation. We have used As$^+$ implantation on Si-on-quartz (SOQ) and high-energy proton implants to penetrate the entire Si [15] to overcome the problem of limited implant depth in our previous study [16]. The proton implantation has little effect on oxide integrity that can be integrated into VLSI back-end process.

II. Experimental

Conventional 10 Ω-cm Si substrates and SOQ wafers with a 2000 Å top Si on 350 μm thick quartz are used in this study. Proton and As$^+$ implantation are performed on standard Si and SOQ with doses of 10^{15} to 10^{16} cm^{-2}, respectively. To meet the requirement of penetrating the entire Si, a proton energy of 10 MeV is required that gives an implanted depth of 698 μm. To study the thermal stability of implanted Si, As$^+$ and proton implanted wafers were annealed at 400 and 600 °C in nitrogen ambient for 1 h. Coplanar transmission lines with 200–1000 μm length and coupled transmission lines with 1000 μm length and 10–60 μm spacing are fabricated on various processed substrates using 1 μm thick Al with 30 μm width. Conventional Si substrate with 1.5 μm thermal oxide was also used as references. Two-port s-parameters up to 20 GHz were measured using HP8510B network analyzer with ground-signal-ground probes. RF loss and cross coupling are extracted from the measured s-parameters after de-embedding from a dummy pad. Pump-probe measurement generated by femto-second laser pulse is used to obtain the carrier lifetime from reflectance response [16], [17]. Stress-induced leakage current (SILC) and charge-to-breakdown (Q_{BD}) are measured for 30 Å oxides to study the influence of gate oxide integrity by ion implantation.

TABLE I
Measured Resistivity After As$^+$ or Proton Implants on Different Substrates

Substrate	SOQ	SOQ	Conventional Si Substrate	Conventional Si Substrate
Implantation type and dose (cm^{-2})	None	As$^+$ 10^{16}	Proton 10^{15}	Proton 10^{16}
Resistivity (Ω-cm) As-implanted	10	36,000	7,200	1.6×10^6
Resistivity (Ω-cm) 400°C annealed	10	32,000	6,600	1.2×10^6

III. Results and Discussion

We have first measured the resistivity from current–voltage (*I–V*) characteristics and summarized in Table I. The high resistivity after ion implantation may be due to implantation created high defect densities that effectively trap free carriers and increase resistivity. The higher resistivity obtained by As$^+$ implantation than proton, at the same dose of 10^{15} cm^{-2}, is due to the heavier mass of As$^+$ and resultant higher damage and traps in Si. The measured 1.6 MΩ-cm resistivity after proton implantation is close to GaAs and intrinsic Si. The high resistivity stable after 400°C annealing for 1 hr can be considered to integrate into VLSI back-end process.

We have further evaluated transmission line loss. As shown in Fig. 1, the loss decreases monotonically as increasing resistivity, and proton implanted Si owns the very low loss of 6.3 dB/cm. The small difference between SOQ with and without implant

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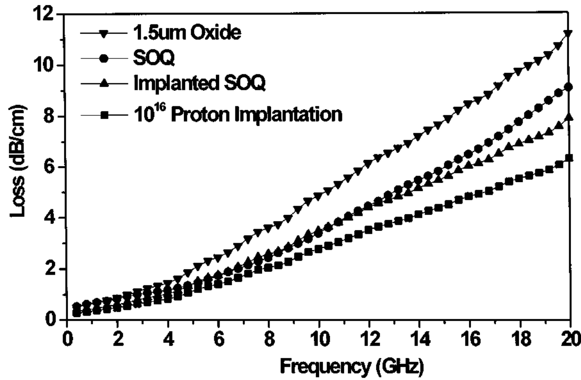

Fig. 1. Transmission line loss for various substrates with different resistivity. The transmission lines length, width, spacing, and Al metal thickness are 1000 μm, 30 μm, 10 μm, and 1 μm, respectively.

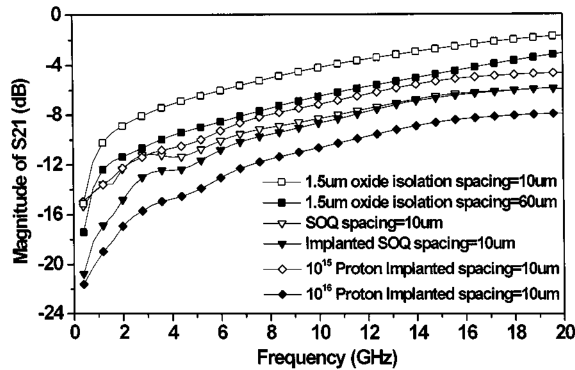

Fig. 2. Cross coupling for various substrates with different resistivity.

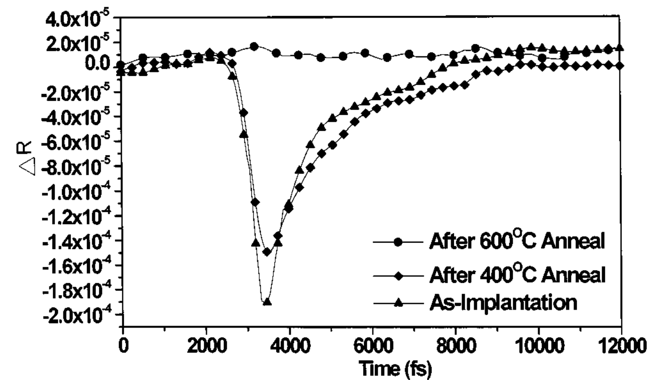

Fig. 3. Reflectance spectra of proton-implanted and different temperature annealed samples.

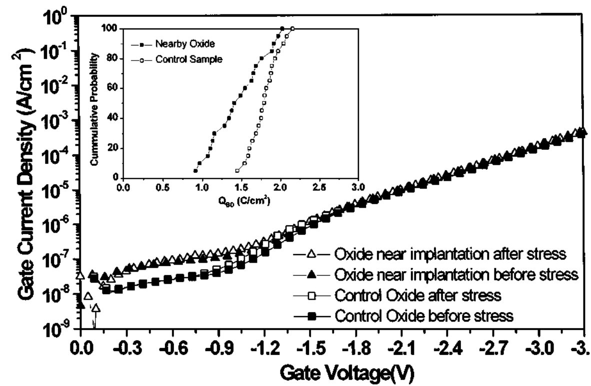

Fig. 4. Stress-induced leakage current and charge-to-breakdown distribution for control MOS devices and devices nearby implantation region. The oxide thickness is 30 Å.

is due to the thin top Si that has a large depletion region by Al contact and thus improves the loss. The measured loss in this work is very competitive with published data in literature that proves implantation is a prominent process technology to reduce loss even we use a thinner Al line compared to other studies.

We have studied the implantation effect on cross coupling. As shown in Fig. 2, the coupling effect becomes worse as decreasing spacing from 60 μm to 10 μm for conventional Si (10 Ω-cm) with 1.5 μm oxide. The strong coupling suggests that the 1.5 μm oxide is still insufficient to obstruct the E-M field penetration. The cross coupling can be greatly reduced by the using As^+ implanted SOQ or proton implanted Si. The proton-implanted wafer shows the best coupling resistance of -79 dB/cm that is due to the extremely high resistivity shown in Table I. The close value between SOQ with and without implant may be due to the depletion effect by Al line.

To study trap recombination rate, we have measured the carrier lifetime from reflectance spectra. As in Fig. 3, carrier lifetimes of 1.1 and 1.3 ps are measured for as-implanted and 400 °C annealed Si, respectively, which suggests that high resistivity can be maintained as long as frequency is less than 1 THz. The high defect density and fast recombination rate can trap free carriers that give high resistivity and improved rf performance. The reason why no signal can be measured after 600 °C annealing is due to the recrystallization produced long lifetime beyond measurement range.

We have further studied the proton implantation on gate oxide integrity [18], [19] that is very important for process integration. Fig. 4 shows the *J–V* characteristics of 30 Å oxides before and after stress and the cumulated Q_{BD} distribution. As shown in Fig. 4, proton implantation has little effect on SILC for oxides nearby implantation region under a metal mask even after a -4.0 V stress for 1000 s with a total charge injection of 2 C/cm^2. In contrast, the MOS capacitors with direct implantation show high resistivity behavior that is due to the damaged Si substrate. The little side effect by proton implantation is also evidenced by the comparable Q_{BD} of devices nearby implantation region with control MOS capacitors, which is also consistent with little SILC influence by implantation. The slightly lower Q_{BD} of nearby MOS devices may be due to proton scattering into the metal mask with proximity contact on Si and damaging the underneath MOS capacitors. Further process development is required for thick metal pattern directly on backend dielectrics.

IV. Conclusions

We have achieved high resistivity and extremely low loss and cross coupling, which is due to $\sim$1 ps lifetime stable after 400 °C annealing. This process is compatible with current VLSI back-end process with little side effect on gate oxide integrity.

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