Reduced Reverse Narrow Channel Effect in Thin SOI nMOSFETs

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***Abstract*—The effects of narrow channel width on the threshold voltage of deep submicron silicon-on-insulator (SOI) nMOSFETs with LOCOS isolation have been investigated. The reverse narrow channel effect (RNCE) in SOI devices is found to be dependent on the thickness of the active silicon film. A thinner silicon film is found to depict less threshold voltage fall-off. These results can be explained by a reduced oxide/silicon interface area in the transistor width direction, thus the boron segregation due to silicon interstitials with high recombination rate is reduced.**

***Index Terms*—Reverse narrow channel effect (RNCE), silicon-on-insulator (SOI).**

I. Introduction

REDUCED body effects, freedom from latch-up, and excellent soft-error immunity have made silicon-on-insulator (SOI) technologies very attractive for future high-speed operation of complementary metal-oxide-semiconductor field effect transistors (CMOSFETs). SOI MOSFETs also offer significant power reduction as compared with bulk MOSFETs due to the reduced parasitic capacitance [1]. Meanwhile, the demand for low-power applications has called for the use of transistors with narrow-channel width [2]. It is therefore technologically important to study the characteristics of narrow-channel SOI MOSFETs suitable for low-power and high-speed digital and analog circuit applications. Previously, there have been many studies comparing the characteristics of fully-depleted and partially-depleted SOI CMOSFET's. Fully-depleted SOI CMOSFETs have been shown to depict improved isolation/integration density, reduced parasitic capacitance, improved radiation hardness, simpler fabrication process, reduced junction leakage, and larger current gain during low-voltage operation [3]. More recently, reverse short channel effect (RSCE) in SOI MOSFETs has also been reported to depend on the silicon film thickness (Tsi) [4], [5]. Several recently papers have considered various aspects of the width effect of SOI MOSFET's [6]–[10]. However, to the best of our knowledge, the dependence of the reverse narrow channel effect (RNCE) on the Tsi has never been reported in detail. In the present paper we report, for the first time, the effects of silicon film thickness on the RNCE. A model is also proposed to explain the observed phenomenon.

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II. Experimental

N^+ poly-Si gate n-channel MOSFET's were fabricated using boron doped $\langle 100 \rangle$-oriented separation by implanted oxygen (SIMOX) wafers with Tsi ranging from 40 to 190 nm. The buried oxide thickness was 400 nm. Local oxidation of silicon (LOCOS) was performed to fully consume the active silicon layer in the isolation region. Channel implant was performed by BF_2 (50 keV, 6×10^{12} cm^{-2}), followed by the growth of a 4 nm gate oxide at 800 °C with *in-situ* HF-vapor cleaning. Afterwards, a 200-nm poly-Si layer was deposited, patterned, and etched to form the transistor gates. A shallow n^+ S/D extension implant with As (5 keV, 1×10^{15} cm^{-2}) was then performed, followed by the formation of a low pressure CVD (LPCVD) TEOS spacer. Then, an As implant at 10 keV with a dose of 5×10^{15} cm^{-2} was performed to form the n^+-doped source/drain regions. After the deposition of passivation oxide and contact formation, wafers received a rapid thermal annealing (RTA) at 1000 °C for 10 s. Wafers were then processed through a standard backend flow through metallization. Finally, wafers were sintered at 400 °C for 30 min in forming gas.

III. Results and Discussion

Fig. 1 shows the measured n-channel threshold voltage roll-off value (with reference to 20 μm wide device) at $V\text{sub} = 0$ V as a function of channel width for the T-gate test structure (as shown in the inset of Fig. 2) with different active silicon film thickness. Here ΔVth is defined as $Vth(W) - Vth$ ($W = 20$ μm). The threshold voltage is measured at $Vd = 50$ mV at the intercept point on the Vg axis of the Id versus Vg curve extrapolated from the point of maximum slope. Although devices with thick silicon film depict serious reverse narrow channel effect (i.e., drastic Vth fall-off with decreasing channel width), the threshold voltage fall-off is alleviated as the silicon thickness is decreased. It is worthy to note here that since a fixed channel implant was performed for all splits with different active silicon film thickness, the thinner film actually received a heavier dopant concentration, which in turn should be more susceptible to Vth fall-off. Fig. 2 shows the body effect factor (γ) ratio {Gamma($W = 0.6$ μm)/Gamma($W = 20$ μm)} versus the silicon film thickness for both T- and H-gate test structures (as shown in the inset of Fig. 2). It should be noted that the H-gate devices are edgeless (i.e., the active channel

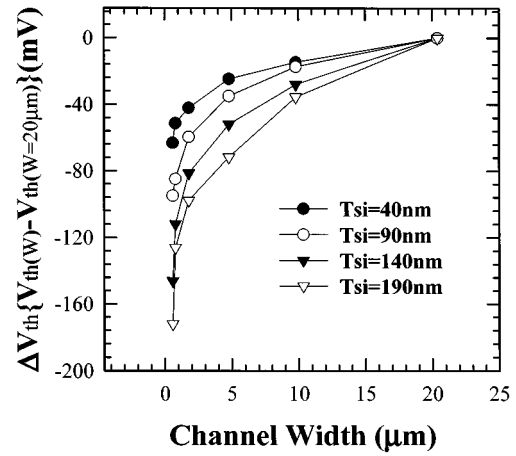

Fig. 1. Threshold voltage roll-off value as a function of the channel width for samples with various silicon film thicknesses. The ΔVth is defined as $Vth(W) - Vth$ ($W = 20$ μm).

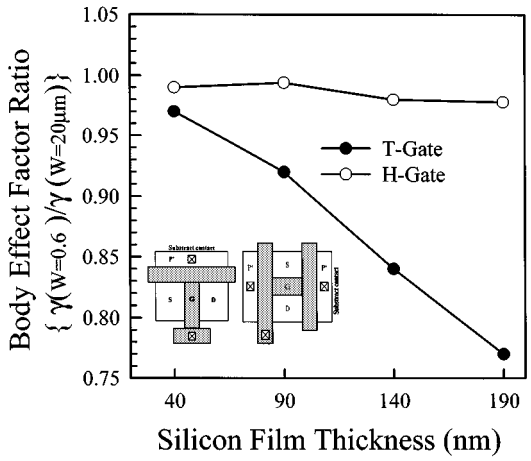

Fig. 2. Body effect factor (γ) ratio {Gamma($W = 0.6$ μm)/Gamma($W = 20$ μm)} versus the silicon film thickness for T- and H-gate devices.

region does not interface with LOCOS isolation edge). In contrast, the T-gate devices have a LOCOS-isolation edge in the width direction as shown in the inset of Fig. 2. In the case of H-gate devices, γ ratio is almost independent of Tsi, depicting a value close to one. This is believed to be primarily due to their edgeless feature, so that they are immune to any effects due to boron segregation into the isolation oxide in the width direction [11]. Therefore, γ ratio is almost close to one irrespective of Tsi. On the other hand, T-gate devices not only depict lower γ ratio than H-gate devices but also show an apparent dependence on Tsi. Obviously, the difference in the behavior between T-gate and H-gate devices must be due to the existence of edge oxide. However, the dependence of γ ratio for T-gate on Tsi is somewhat unexpected.

To explain this intriguing phenomenon, a physical model is proposed as shown in Fig. 3. It is well known that silicon interstitials generated by source/drain implantation tend to move toward the Si/SiO_2 interface and recombine there during subsequent thermal processing [12]. This is the so-called transient enhanced diffusion (TED) that causes RSCE and RNCE [12], [13]. In the case of RNCE there is probably an enhanced segregation

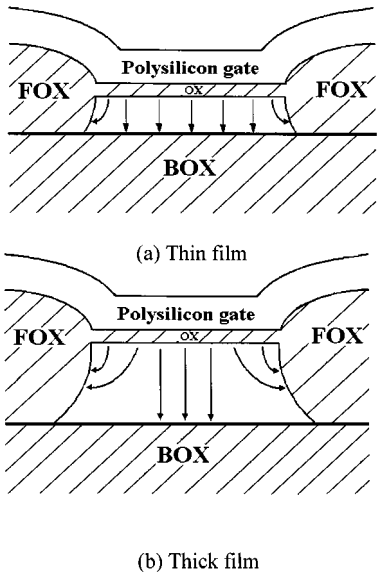

Fig. 3. Schematic shows the mechanism of RNCE for thin and thick SOI MOSFETs.

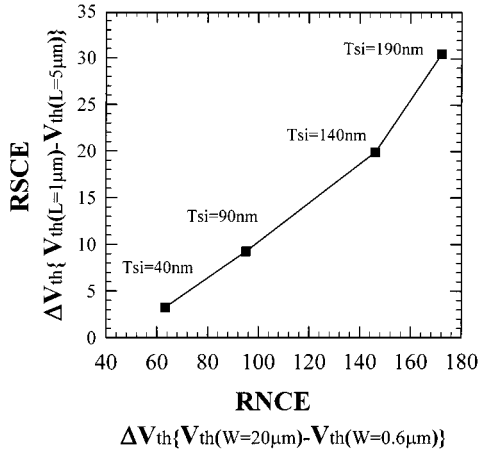

Fig. 4. Relationship between RSCE and RNCE for different silicon film thickness.

at the LOCOS oxide due to the combination of interstitial and local stress gradients. Fig. 3 shows a schematic of the 2-D flux of excess interstitials caused by implantation damage or arsenic deactivation. The recombination of the diffusion-enhancing interstitials at the Si/SiO_2 interface in the width edge gives rise to the observed Vth fall-off dependence in the width direction and the reduction of RNCE in thinner Tsi SOI devices as show in Fig. 1. A thinner Tsi and its corresponding smaller cross-sectional silicon/oxide interface area in the width edge results in a smaller number of interstitials arriving and recombining there. Thus, a larger ratio of channel boron atoms diffuse and segregate into the buried oxide instead of the isolation oxide in the width edge, thus leading to the reduction of RNCE in SOI devices with thinner Tsi. Fig. 4 shows the relationship between RSCE and RNCE for different Tsi devices. It is clearly shown that the reduced RSCE in thin Tsi devices is accompanied with reduced RNCE. This is consistent with previous reports that the reduced RSCE in thinner SOI devices is primary due to the decrease of the lateral distribution of Si interstitials resulted from

their high recombination velocity at the buried oxide [5]. Vth shift due to RSCE is in fact in proportion to the Vth shift due to RNCE as shown in Fig. 4. This result supports our proposed model that Si interstitials with higher recombination velocity at the buried oxide will reduce the lateral redistribution in both length and width directions.

IV. Conclusion

In this letter, we have investigated the effects of silicon film thickness on the reverse narrow channel effect of SOI nMOSFETs. Devices with thinner Tsi show a reduced reverse narrow channel effect as well as reverse short channel effect. Furthermore, Vth shift due to RSCE is found to be proportional to the Vth shift due to RNCE as Tsi increases. The experimental findings can be explained by a decrease of cross-sectional silicon/oxide interface area in the width edge so that the boron segregation into oxide due to silicon interstitials is reduced, leading to a reduced RNCE in SOI nMOSFETs with thinner silicon film.

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