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A Behavior-Level Fault Model for the Closed-Loop Operational Amplifier

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In this paper, a simple behavior-level fault model, which is able to represent the faulty behavior of the closed-loop operational amplifier (OP), is presented. The fault model, derived from the macro equivalent circuit of the OP but verified with transistor level simulation, consists of the offset fault and the limited-current fault. It can represent the faulty behavior of the closed loop OP of all the transistor parametric (soft) faults and many of the catastrophic (hard) faults. Due to its simplicity, the proposed fault model (1) significantly reduces the complexity of fault simulation, and (2) makes closed-form analysis of the faulty behavior of the closed loop OP feasible when the closed loop OP is used as a basic building block of a complicated circuit. Although derived for DC, it can also be applied to AC fault analysis.

Keywords: fault simulation, fault model, macro-modeling, operational amplifier, analog/mixed testing, Monte Carlo

1. INTRODUCTION

Analog testing, basically, is classified into two approaches, namely, the specification-driven approach [1] and the fault-model-driven approach [2-6]. For the specification-driven approach, the device under test (DUT) is declared to be faulty if the output function is out of specification under some testing stimuli. In the fault-model-driven approach, the DUT is claimed to be faulty if faulty behavior of the associated fault model occurs. In the later approach, a fault list is constructed carefully, and input stimuli are selected intelligently so that the deviation caused by the defects can be easily observed and measured. The fault list is constructed based on the fault model adopted. The fault model can not only describe the fault effect more clearly and offer clues to derive the test stimuli, but also makes it more feasible to modify the input stimuli and estimate its fault coverage by means of analog fault simulation. Therefore, fault models with the advantages of high speed and less memory are always desired. They have been built at different levels, such as the behavior-level, the

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macro-level, the circuit-level and the defect-level. For example, at the behavior-level, the linear error model [7-8], the impulse response fault model [9], and the functional fault model [10] have been proposed and analyzed.

Since the OP is the most important and primitive element in the analog circuit, many fault models for OP have been presented. For example, at the macro-level, hierarchical fault modeling [11], fault modeling from the defect simulation [12], and fault macro-modeling [15] for analog/mixed-signal circuits have been proposed. Another model incorporating testing strategies for analog/mixed circuits [13-14] has been proposed too. They are all for the open-loop OP.

In this paper, a behavior fault model for the closed-loop OP is proposed. For most linear applications, the OP is used in the closed loop. An advantage of using the behavior closed-loop fault model is that when a fault is injected, the OP is treated at the higher level during simulation or test generation. This speeds up fault simulation and test generation. The fault model proposed is very simple but covers the fault effects of parametric faults and catastrophic transistor short/nearly-open faults at the transistor-level of the OP. The model lumps all the fault effects into an offset voltage fault and a limited-current fault when the OP is operating in the inverting and non-inverting closed loop configurations. The fault model is developed through DC analysis but can be applied to fault simulation for AC analysis if the fault effects caused by the transistor level faults do not significantly affect the frequency response of the OP, i.e., if the OP can still be modeled as a single pole amplifier. Also, it can be used in statistical fault analysis [18] to reduce the number of the parameters for Monte Carlo analysis.

2. DC FAULTY BEHAVIORS OF THE CLOSED-LOOP OP

In this section, DC faulty behavior is investigated by using an exhaustive transistor-level fault simulation on the benchmark OP [16] operated under three different configurations. The simulated circuits are shown in Fig. 1, where (a), (b) and (c) are the three configurations, namely, the inverting, the non-inverting, and the unit gain buffer configuration, respectively, and (d) is the transistor level circuit of the OP used in the three configurations. The injected faults are single faults and include all the parametric faults (W, L and V_t ±10% variation of each transistor) and all the catastrophic faults (short and nearly open for each transistor).

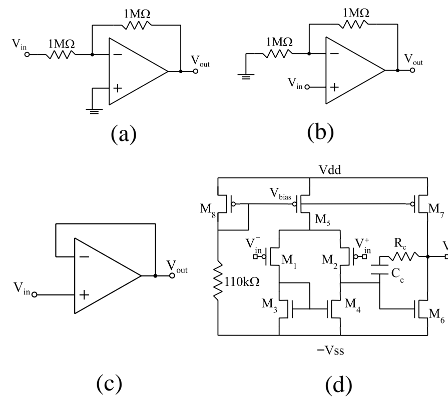

Fig. 1. Simulated circuits for DC fault analysis: (a) inverting configuration; (b) non-inverting configuration; (c) unit gain buffer; (d) benchmark OP [16] at the transistor-level.

The simulation results are shown in Figs 2 and 3 for both the good circuit and the faulty circuits, respectively. In Fig. 2, the offset voltage, F_{os}, between two input terminals of the fault free OP is plotted with respect to the input voltage V_{in}, for three configurations. It can be seen that even for the fault free OP, there are small quantities of offset voltage for each configuration. These offset voltages come from the intrinsic unbalance, although small, between two input stages in the designed circuit, and they basically shows a linear relationship with respect to the input voltage. Fig. 3 shows the same input offset voltage plots with respect to the input voltage for the faulty circuits with 40 catastrophic injected faults. According to the different faulty behaviors, they can be classified into four types. For each type of behavior, there is a representative fault. The representative faults are M_4

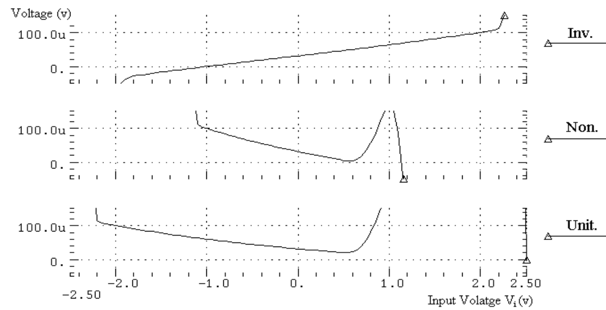

Fig. 2. The input offset voltages plots in terms of the input voltage for the (a) inverting configuration, (b) non-inverting configuration, and (c) unit gain buffer configuration for the fault free OP.

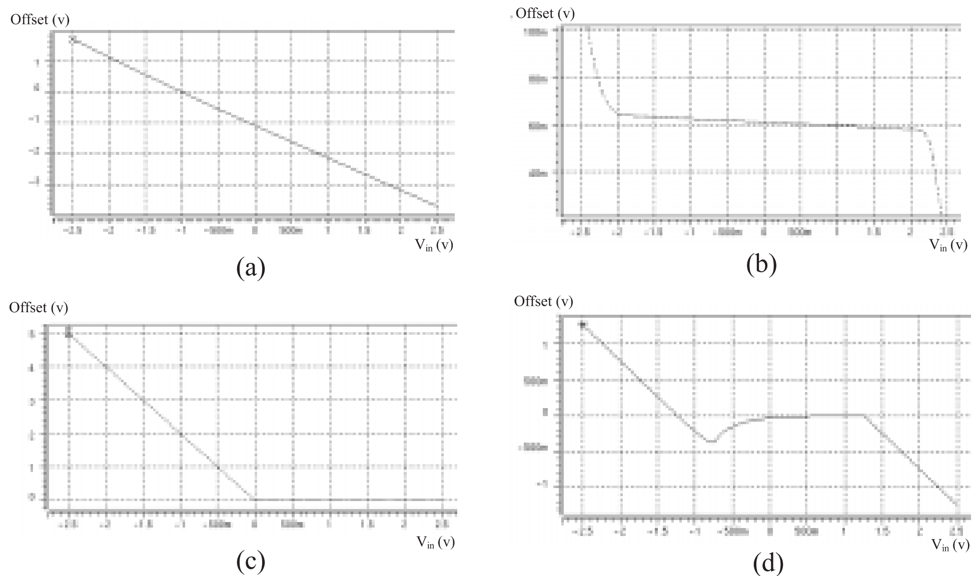

Fig. 3. DC input-offset relationship for four types of representative faults: (a) Type I faults: the input-offset voltage is linear in the full input swing; (b) Type II faults: the input-offset voltage is similar to the fault free case but with a narrower input voltage range; (c) Type III faults: piecewise linear; (d) Type IV faults: the input-offset voltage is nonlinear in terms of the input voltage.

drain-to-gate short (type I), M_5 drain-to-source short (type II), M_7 drain open (type III) and M_5 drain-to-source short (type IV), respectively. The former three faults are for the inverting configuration, and the fourth fault is for the non-inverting configuration. As shown in Fig. 3, Type I faults cause the full swing linear input-offset relationship (Fig. 3(a)). For this type of fault, if the faulty offset voltage just cancels out the input voltage, then the output sticks at a fixed voltage. Therefore, the output stuck-at fault is a Type I fault. As shown in Fig. 3(b), a Type II fault, similar to that of the fault free OP, has a linear region in the input-offset relationship, but the linear input-offset region is not full swing. For this type of fault, there are two reasons why the linear region does not cover the full input swing. The first is that when the input voltage in one of the inputs of the OP is high (or low), some transistors of the OP will go out of the saturation region, and the gain of the OP will be degraded. For example, when the input rises to $V_{dd}-V_{bias}$, transistor M_5 enters into the triode region. This explains why the unit gain buffer is left out of the linear region at the higher voltage as shown in Fig. 2. The other reason is output voltage saturation. Because the closed-loop gain is 2 for the non-inverting configuration, when the input is close to $V_{dd}/2$ or $-V_{ss}/2$, one of the output transistors will enter into the triode region. This will cause the linear region of the input-offset relationship to be narrower than that of the inverting configuration. All the parametric faults belong to this type (Type II) of fault. Type III faults (Fig. 3(c)) have a piecewise linear region which is much narrower and the magnitude of the offset is much larger than that of Type II faults. For this type of fault, the output current of the OP is limited. For example, the M_7 drain open fault shown in Fig. 1(d) causes the OP to be unable to support the normal current. When the OP is used in the inverting configuration, the output voltage can not be charged to high when the input voltage is lower than 0. As a result, the faulty offset voltage increases rapidly and monotonically as the input reaches a voltage for which the output stage of the OP can not supply or sink its normal current. This type of faults called "limited-current fault." This type of fault affects the slew rate of the OP. For Type IV faults, there is no linear input-offset relationship as shown in Fig. 3(d).

For all the above four types of faults, the percentage of each type of faults in terms of the total number of transistor catastrophic faults for each configuration are shown in Table 1. (Recall that the previous DC transistor-level fault simulations proved that all soft faults belong to Type II faults.)

Table 1. The percentages of transistor level hard (catastrophic) faults for the four classified types in terms of their input-offset behaviors.

Circuit Configuration	40 Catastrophic Faults			
	Type I	Type II	Type III	Type IV
Inverting	65%	15%	20%	0%
Non-inverting	57.5%	10%	25%	7.5%
Unit Gain Buffer	52.5%	10%	22.5%	15%

3. OFFSET FAULT MODEL

In order to describe the previously mentioned fault behaviors using a fault model, the macro-level equivalent circuit of the OP as shown in Fig. 4 is used, where the OP is operated in the inverting configuration. For this equivalent circuit, R_{id}, R_{icm}, R_o are the differen-

tial mode input resistance, the common mode input resistance, and the output resistance, respectively; V_{os} is the input offset voltage; R_{ss} and R_{dd} are the resistors representing the shorting defects of the output to the power supplies V_{dd} and V_{ss}, respectively; A is the open loop gain; R_1 and R_2 are external resistors. For an ideal fault free OP, R_{id}, R_{icm}, R_{ss}, R_{dd} and A will be infinite, and R_o and V_{os} will be zero. When an OP is not ideal or a transistor level fault as mentioned in the previous section occurs, one or more of the above parameters will have finite value and/or will be affected. It is necessary to derive the input-output relationship from this circuit to see how the transistor level faults will affect the input-output relationship through these parameters.

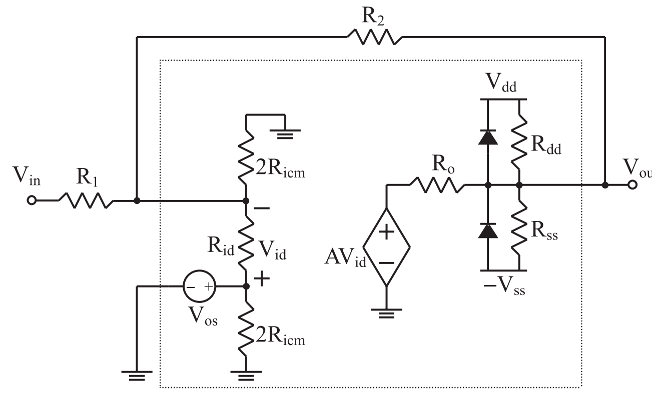

Fig. 4. The macro equivalent circuit of the OP in the inverting configuration.

After superposition, the result is:

$$V_{out} = -\frac{R_2}{R_1}\left[V_{in} + \frac{-R_2}{D+R_2}V_{in}\right] + \frac{R_2\|D}{R_1\|R_2\|2R_{icm}\|BR_2}V_{os} + \frac{SF}{R_{dd}}V_{dd} - \frac{SF}{R_{ss}}V_{ss}, \tag{1}$$

where

$$R_{11} = R_1\|2R_{icm}\|R_{id},$$

$$SF = R_{dd}\|R_{ss}\|R_0\left\|(R_2+R_{11})\right\|\frac{R_0(R_{11}+R_2)}{AR_{11}},$$

$$B = \left(\frac{A}{R_0} - \frac{1}{R_2}\right)(R_{id}\|R_1\|R_2\|2R_{icm}) \text{ and}$$

$$D = B(R_2\|R_0\|R_{dd}\|R_{ss}).$$

Eq. (1) can be simplified into the following form:

$$V_{out} = A_{CL}(V_{in} + mV_{in} + k) \tag{2}$$

where

$$A_{CL} = -\frac{R_2}{R_1} \text{ is the closed-loop gain,}$$

$$m = \frac{-R_2}{D+R_2},\ k = aV_{os} + bV_{dd} + cV_{ss},$$

$$a = \frac{R_2 \| D}{A_{CL}(R_1 \| R_2 \| 2R_{icm} \| BR_2)},$$

$$b = \frac{SF}{A_{CL}R_{dd}} \text{ and } c = -\frac{SF}{A_{CL}R_{ss}}.$$

Eq. (2) is the input-output transfer function of the OP in the inverting configuration taking the non-ideal effects, such as the input offset voltage, the finite gain, and the finite input and output resistances, into account. The above nonideal property of the circuit can be modeled as an ideal OP with an input offset voltage: $F_{os} = mV_{in} + k$, as shown in Fig. 5(a), where m is a parameter related to the closed-loop gain and k is a parameter related to the offset of the circuit when the input is zero and a transistor level fault exists in the OP. The values of both m and k are independent of the magnitude of the input.

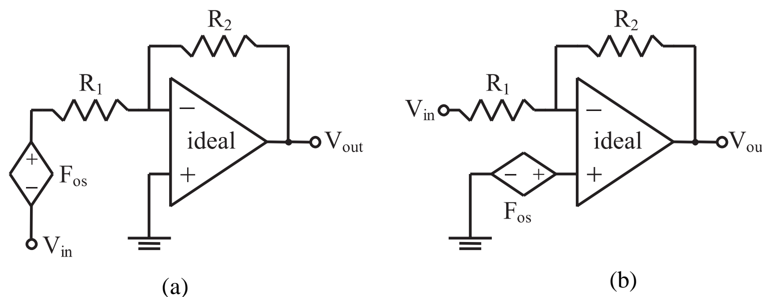

Fig. 5. Behavior-level offset fault model for the OP in the inverting configuration: (a) the offset placed at the circuit input; (b) the offset placed at the OP input.

The above equation means that any variation(s) in R_{icm}, R_{id}, R_o, R_1, R_2, R_{ss}, R_{dd}, V_{os}, or A, which, as stated previously, come from the transistor level faults of the OP, can be lumped into the two parameters, m and k. The more serious the transistor level faults, the more faulty the behavior of the circuit, and the larger the values of m or k. For example, a "node short" transistor fault between two nodes of the OP, causing the output to always stick at some voltage, makes R_{ss} and R_{dd} in Fig. 4 very small. In this case, m is −1, and k is just the output stuck-at voltage. But for an ideal OP, $A \to \infty$ and $V_{os} \to 0$, which cause B, D, R_{dd} and R_{ss} approach to be infinite, $m \to 0$ and $k \to 0$.

The offset fault model shown in Fig. 5(a) can be shown in another form as in Fig. 5 (b), where the offset is connected directly to the positive input of the OP with different m and k. In both circuit forms shown in Figs. 5(a) and (b), the parameters m and k well describe the faulty behaviors of Type I faults for the full input swing and of Type II and Type III faults for the middle segment of the input swing mentioned in the previous section.

For the OP operating in the non-inverting configuration, a similar analysis can be done to obtain an equation similar to Eq. (2) using node analysis with only the following parameters:

$$A_{CL} = 1+\frac{R_2}{R_1} \text{ and } m = \frac{-R_2}{D+R_2} + \frac{D}{D+R_2} \times \frac{R_1 \| R_2}{2R_{icm} \| BR_2}.$$

The unit gain buffer configuration is a special case of the non-inverting configuration with $R_1 \to \infty$ and $R_2 \to 0$ in Eq.(1) with

$$A_{CL} = 1,\ m = \frac{-U}{U+R_f},\ a = \frac{R_f}{U+R_f} \text{ and}$$

$$SF = R_{dd} \| R_{ss} \| R_0 \| R_{id} \| 2R_{icm} \left\| \frac{R_0}{A} \right.,$$

where , $U = R_{id} \left\| \frac{R_0}{A} \right., R_f = R_{dd} \| R_{ss} \| 2R_{icm} \| R_0$.

The behavior-level offset fault models for the non-inverting configuration and for the unit gain buffer configuration are shown in Figs. 6(a) and (b), respectively.

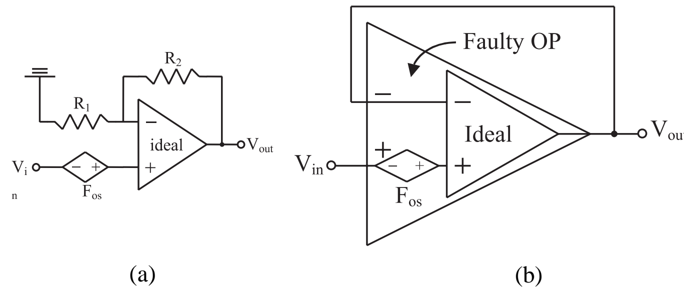

Fig. 6. Behavior-level offset fault model for the closed-loop OP: (a) in the non-inverting configuration; (b) in the unit gain buffer.

4. LIMITED-CURRENT FAULT MODEL

In the previous section, the voltage-control voltage source of the macro-equivalent circuit shown in Fig. 4 is assumed to always be AV_{id} when deriving the behavior level fault model. However, in reality, there is a limit on the output current that an OP can supply. It is limited by the driving capability of the output stage of the OP, especially the faulty OP.

Fig. 7 shows the conceptual relationship of the output current with respect to the differential input V_{id} of the OP of the circuit of Fig. 1(a), where the fault-free OP has a finite open-loop gain and a small offset since it not an ideal OP and the faulty OP has a smaller gain with a much larger offset. Both OP's have limits on their output currents. When the input of the OP reaches a value for which the OP can not supply a current, the two inputs of the OP cease to be virtual-short and begin to act as two open nodes. The differential input V_{id} will arbitrarily increase to satisfy the KCL and KVL laws of the circuit with the nearly constant output current of the OP. That is, the OP does not work normally. For the OP with Type III faults, its output driving currents, I_{max}, I_{min}, (the maximum and minimum currents), deviate from their normal values, so the whole closed-loop circuit no longer works, and the faulty OP operates abnormally.

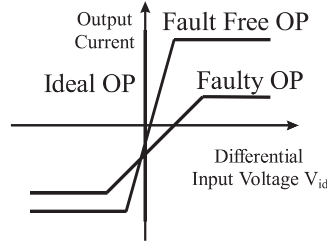

Fig. 7. Conceptual relationship explaining the limited-current fault.

Therefore, to take into account the above effect, the fault model shown in Fig. 5(b) is modified to get those shown in Fig. 8, where both the offset fault and the limited-current fault are included. The model has 4 parameters: m, k, I_{min} and I_{max}. When the output current $I_{min} < I_o < I_{max}$, the two differential inputs of the ideal OP are still virtual-short ($V_{id} = 0$) together with the faulty offset voltage $F_{os} = mV_{in} + k$ as shown in Fig. 8(a). When $I_o > I_{max}$ or $< I_{min}$, I_o equals I_{max} or I_{min} and $V_{id} \neq 0$; i.e., the two inputs of the ideal OP will be treated as open nodes as shown in Fig. 8(b). According to Table 1, the fault model shown in Fig. 8 can cover all the transistor-level soft faults and 92.5% of the hard faults of the OP. The faults which can not be modeled are M_{4dg} (drain to gate short), M_{5ds} (drain to source short), M_{1g} (gate nearly open) for the non-inverting configuration and M_{2dg}, M_{4dg}, M_{5ds}, M_{1g}, M_{3s} and M_{5g} for the unit gain buffer.

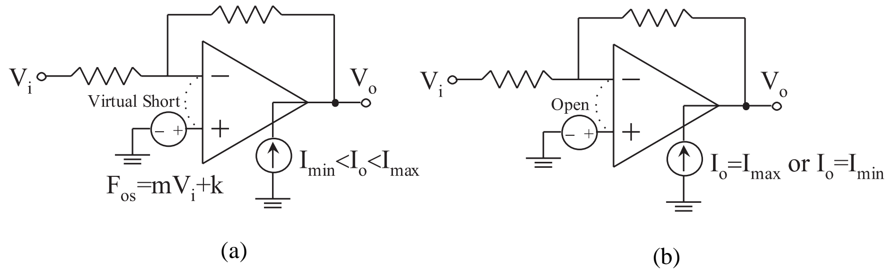

Fig. 8. The proposed complete fault model, including (a) offset fault; (b) limited-current fault for the inverting configuration.

5. VERIFICATION OF THE MODEL USING TRANSISTOR LEVEL SIMULATION

Since the above model was derived from the macro equivalent circuit of the OP shown in Fig. 1, it was appropriate to verify the model using transistor level simulation.

First, transistor level simulations of the three OP configurations were performed for DC as well as sinusoidal AC with some transistor parametric faults injected into the OPs. The outputs were then compared with those obtained using behavior level simulation with the corresponding offset faults injected at the inputs of the OP circuits. During the simulations, if the input of the OP was outside the allowable input range, i.e., $V_{in} < V_{min}$ or $V_{in} > V_{max}$, the limited-current fault model Fig. 8(b) was applied. Table 2 shows the results of this comparison of DC and AC under different frequencies, where the amplitude

Table 2. DC and AC analysis of soft faults in thhe inverting configuration.

Faults	DC Analysis					10Hz		10kHz		100kHz		1MHz		10MHz	
	m	k	V_{min}	V_{max}	A.E(%)	A.E(%)	P.E.(°)	A.E(%)	P.E.(°)	A.E(%)	P.E.(°)	A.E(%)	P.E.(°)	A.E(%)	P.E.(°)
Fault Free	-3.3e-5	-1.4e-5	-2.45	2.45	7.5e-3	6.0e-2	0	0.068	0.032	0.236	0.094	3.46	7.57	72.0	143
V_{t1}+50%	-2.8e-5	0.9	-2.5	1.55	8.2e-3	7.9e-2	0.136	0.130	0.123	0.219	0.256	7.95	6.80	59.8	143
V_{t2}+50%	-2.1e-5	-0.9	-1.55	2.5	2.4e-3	8.5e-2	0.330	0.102	0.398	0.165	0.487	3.25	8.72	60.4	144
V_{t3}+50%	-2.7e-5	-0.88	-1.6	2.5	3.4e-3	7.0e-2	0.243	0.103	0.299	0.210	0.503	22.7	7.05	67.2	171
V_{t4}+50%	-1.5e-5	0.88	-2.5	1.55	4.9e-3	9.9e-2	0.169	0.142	0.209	0.443	0.467	86.4	31.2	96.6	128
V_{t5}+50%	-2.8e-5	-2.2e-4	-2.45	2.45	6.4e-3	5.9e-2	0	0.084	0	0.404	0.212	15.0	18.0	90.2	158
V_{t6}+50%	-3.3e-5	-4.8e-4	-2.45	2.45	7.5e-3	6.3e-2	0	0.064	0.016	0.224	0.143	3.45	7.57	72.0	143
V_{t7}+50%	-5.5e-6	2.5e-4	-2.45	2.45	1.1e-3	3.8e-2	0.027	0.075	0.052	0.169	0.202	3.78	8.34	71.8	152
V_{t8}+50%	-6.7e-5	-1.0e-5	-2.45	2.4	9.9e-3	2.4e-2	0	0.047	0	0.246	0.158	2.47	2.54	58.1	134
V_{t1}-50%	-2.1e-5	-0.9	-1.55	2.5	2.4e-3	7.5e-2	0.271	0.110	0.437	0.175	0.575	3.64	7.13	60.1	143
V_{t2}-50%	-2.8e-5	0.9	-2.5	1.55	9.4e-3	8.9e-2	0.07	0.152	0.319	0.197	0.529	5.47	8.06	59.7	143
V_{t3}-50%	-1.5e-5	0.88	-2.5	1.55	4.9e-3	8.1e-2	0.098	0.141	0.165	0.444	0.457	86.2	31.3	96.4	127
V_{t4}-50%	-2.8e-5	-0.881	-1.6	2.5	3.4e-3	5.3e-2	0.188	0.094	0.471	0.226	0.596	22.5	68.6	67.2	171
V_{t5}-50%	-4.1e-5	2.8e-4	-2.45	2.45	9.3e-3	6.0e-2	0	0.059	0	0.190	0.238	2.68	2.28	57.9	135
V_{t6}-50%	-3.3e-5	4.5e-4	-2.45	2.45	7.6e-3	6.0e-2	0	0.067	0.027	0.245	0	3.46	7.41	72.0	143
V_{t7}-50%	-6.1e-5	-2.5e-4	-2.45	2.4	9.1e-3	1.6e-2	0	0.047	0	0.310	0.254	2.99	7.05	71.9	143
V_{t8}-50%	-6.1e-6	-3.3e-6	-2.45	2.45	1.3e-3	1.2e-2	0	0.082	0.050	0.230	0.144	9.21	11.4	88.6	161
L_1+50%	-3.2e-5	0.207	-2.5	2.25	9.4e-3	6.1e-2	0.031	0.082	0.073	0.255	0.151	6.88	9.54	86.0	143
L_2+50%	-1.1e-5	-0.207	-2.25	2.5	1.9e-3	5.3e-2	0.081	0.094	0.112	0.079	0.099	3.21	7.15	71.7	145
L_3+50%	-2.0e-5	-0.192	-2.3	2.5	3.4e-3	4.4e-2	0.079	0.026	0.063	0.097	0.238	3.17	1.76	67.6	148
L_4+50%	-1.6e-5	0.192	-2.5	2.25	4.1e-3	7.6e-2	0.073	0.081	0.040	0.291	0.123	3.86	7.44	74.7	143
L_5+50%	-3.1e-5	-9.4e-5	-2.45	2.45	7.1e-3	6.0e-2	0	0.066	0.014	0.275	0	4.18	9.32	78.9	148
L_6+50%	-3.1e-5	-1.2e-4	-2.45	2.4	5.3e-3	4.0e-2	0	0.064	0.016	0.329	0.205	3.39	8.77	72.0	151
L_7+50%	-2.2e-5	8.0e-5	-2.45	2.45	4.6e-3	5.0e-2	0	0.037	0.027	0.224	0.356	3.84	6.87	72.2	145
L_8+50%	-3.6e-5	-5.4e-6	-2.45	2.4	5.6e-3	1.6e-2	0.014	0.043	0	0.230	0.072	2.99	1.50	65.4	139
W_1+50%	-1.7e-5	-0.160	-2.3	2.5	2.8e-3	4.4e-2	0.060	0.064	0.078	0.081	0.063	4.57	5.72	77.3	152
W_2+50%	-3.1e-5	0.160	-2.5	2.3	9.0e-3	8.0e-2	0.053	0.083	0.041	0.223	0.110	3.97	3.80	70.9	145
W_3+50%	-1.9e-5	0.177	-2.5	2.25	8.7e-3	5.4e-2	0.064	0.098	0.113	0.308	0.163	3.85	7.40	74.6	143
W_4+50%	-1.9e-5	-0.177	-2.3	2.5	3.3e-3	4.7e-2	0.068	0.061	0.090	0.090	0.108	3.09	2.05	67.3	146
W_5+50%	-3.6e-5	1.0e-4	-2.45	2.45	8.3e-3	6.2e-2	0	0.063	0	0.212	0.238	3.03	1.23	63.8	140
W_6+50%	-2.2e-5	7.8e-5	-2.45	2.45	4.6e-3	5.2e-2	0	0.067	0.049	0.249	0.265	3.56	7.77	72.4	146
W_7+50%	-3.1e-5	-1.1e-4	-2.45	2.4	5.3e-3	1.5e-2	0.012	0.058	0	0.273	0.076	3.44	7.12	71.9	144
W_8+50%	-2.0e-5	-8.6e-6	-2.45	2.45	4.5e-3	5.0e-2	0	0.063	0.050	0.236	0.076	4.21	8.55	78.0	149
Average					5.6e-3	5.5e-2	0.063	7.9e-2	0.102	0.236	0.232	10.4	8.34	72.3	146

error is $A.E.=\sqrt{\Sigma\frac{(V_{o_sim}-V_{o_model})^2}{V_{o-sim}{}^2}}\times 100\%$, the phase

error is , $P.E.=\sqrt{\Sigma\left(\frac{t_d}{T}\right)^2}\times 360°$,

Σ is under the inputs of different amplitudes, V_{o_sim} is the magnitude of the simulation output, V_{o_model} is the magnitude evaluated by the offset model, t_d is the phase delay and T is the period of the input signals. In the table, it can be seen that the results obtained from the proposed behavior level fault simulation are very close to those obtained from the transistor level simulation for the DC and AC simulations up to a frequency of 100KHz. When the simulation frequency approached 1 MHz, which is close to the unit gain frequency of the benchmark OP, the P.E. became larger (8.34° in average), as did the A.E. (about 10.4% in average). This means that, for all parametric faults, if the signal frequency is far away from the OP's cutoff frequency, at which point the fault free OP starts to operate abnormally, the proposed behavior level offset fault model derived from the DC analysis can be applied to simulate the AC response of the closed loop faulty OP circuit with fairly good accuracy.

In the above, all the parameter faults do not affect the open loop frequency response of the OP very much; i.e., the faulty OP still exhibits dominant pole characteristics. As for catastrophic faults, if the faulty OP's dominant pole is less than the working frequency of the circuit, the errors will become large except in the frequency range below the faulty dominant pole. For some faults, such as M_{1_dg}, M_{1_gs}, M_{1_ds}, M_{2_dg}, M_{2_gs}, M_{2_ds}, M_{4_ds}, M_{5_dg}, M_{5_ds}, M_{6_dg}, and M_{6_ds} short faults which still maintain a dominant pole higher than the working frequency of the circuit, the A.E. and P.E. errors will still be small, similar to those of parametric faults.

Next, the fault model was applied to simulate a larger circuit, which was the benchmark biquad filter circuit [17] as shown in Fig. 9. A transistor level hard fault, M_{5_ds} short was injected. The offset fault, derived from the DC transistor level simulation, was F_{os} = 0. 00512 × (V_{in} + V_{LPO})+0.0277 × V_{BPO} − 0.0439. Fig. 10 shows the simulated waveforms at the output LPO of the circuit under two applied stimuli which were square pulses with the amplitude from −2.5V to +2.5V, which did not excite the fault (Fig. 10(a)), and from +2.5V to −2.5V, which did excite the fault (Fig. 10(b)) where a large voltage difference (about

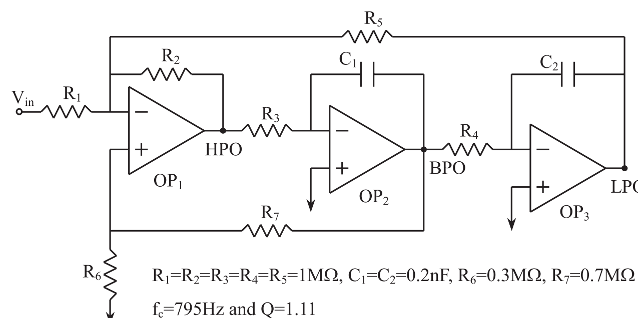

Fig. 9. The simulated benchmark biquad filter circuit [17] with the behavior level fault model.

Table 3. Analog fault simulation time for simulations at three different levels. The waveform length is 20us/1 point.

	100 points	200 points
Transistor Level	26.2 s	32.3 s
Macro Equivalent Circuit Level [15]	3.81 s	5.57 s
Behavior Level with our Proposed Offset Model	2.82 s	3.71 s

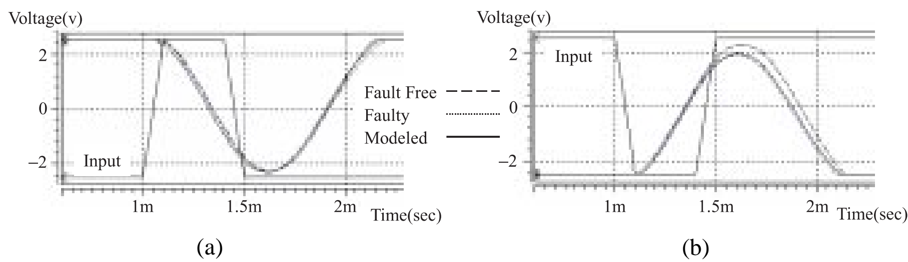

Fig. 10. Analog fault simulation result using the proposed fault model for an injected transistor M_{5_ds} short hard fault. The dotted curves were obtained from the transistor level simulation, and the solid curves were obtained from the module level simulation using the derived fault model. (a) The pattern did not excite the fault; (b) the pattern excited the fault.

250mV) between the fault free circuit and the faulty circuit existed, respectively. It can be seen that the output waveforms obtained from the transistor level simulations are the same as those obtained from the behavior level simulations using the fault model for both cases. Table 3 lists the computer time used in these two simulations as well as the macro equivalent circuit level [15] simulation for two different numbers of simulation points. The behavior level simulation used the least computation time.

6. DISTRIBUTIONS OF *m* AND *k* OF OFFSET FAULTS

To know how the values of *m* and *k* of the offsets would be fault distributed when random transistor level faults occurred. Hence, a Monte Carlo analysis was done by performing 1000 transistor level simulations by randomly injecting multiple parametric faults with 3(=10% on the variations of W, the width, L, the length and V_t, the threshold voltage of each transistor of the benchmark OP for three OP configurations. The obtained offset voltages with respect to the input voltage for three configurations are shown in Fig. 11 where each curve corresponds to a single (multiple) transistor level fault(s). The values of parameters, m and k, can then be extracted from curves of Fig. 11, and they are shown in Fig. 12 in terms of the number of the circuits simulated. These plots give the ranges on the values of offset faults if a behavior level fault simulation is to be performed for a large circuit for which the above three OP configurations are the basic building blocks without going into the transistor level fault simulation.

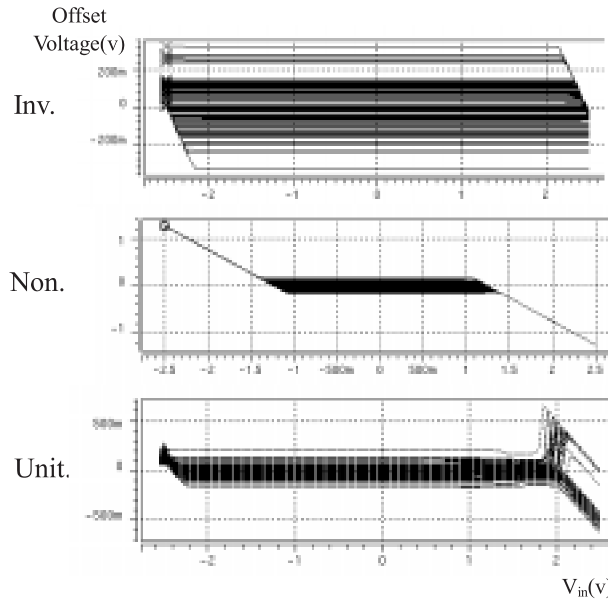

Fig. 11. The input-offset relationship of the Monte Carlo analysis.

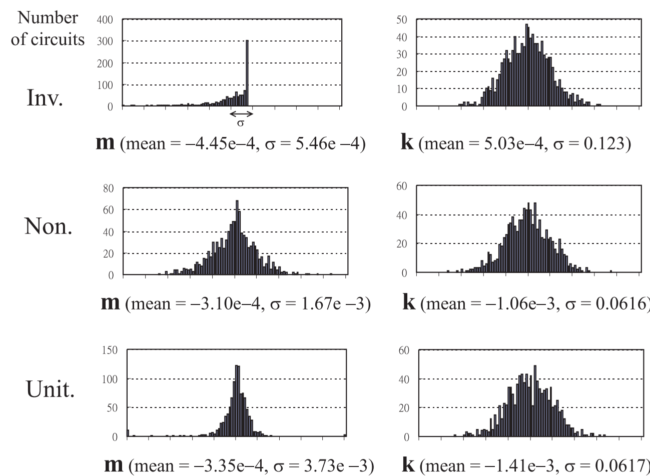

Fig. 12. The distributions of *m* and *k* under the Monte Carlo analysis.

7. CLOSED-FORM ANALYSIS WITH THE FAULT MODEL

Since the derived fault model is very simple, closed form analysis of the linear circuit with the faulty OP is possible. The 3-stage benchmark biquad is again used as an example to demonstrate the contribution of this model. The faulty OP is treated as an ideal OP but with an offset injected at the input of OP_1. By means of superposition of the feedback structure, the offset voltage, F_{os}, can be found to be $m_1V_{in} + m_2V_{HPO} + m_3V_{LOP} + k$, where m_1, m_2, m_3 and k are constants obtained from the transistor level simulation as described below.

Since OPs are treated as ideal at the behavior level,

$$V_{HPO} = -V_{in} - V_{LPO} + 0.9V_{BPO},$$
$$V_{BPO} = -\frac{1}{(2\times10^{-4})s}V_{HPO} \text{ and } V_{LPO} = -\frac{1}{(2\times10^{-4})s}V_{BPO}.$$

For the F_{os} injected at the positive input of OP_1,

$$V_{HPO} = (3m_1 - 1)V_{in} + (3m_2 - 1)V_{LPO} + (3m_3 + 0.9)V_{BPO} + 3k.$$

Solving with the latter two equations, we can obtain

$$\begin{aligned} V_{HPO}(s) &= \frac{(4\times10^{-8})s^2}{(4\times10^{-8})s^2 + (3m_3 + 0.9)(2\times10^{-4})s + (1-3m_2)} \times [(3m_1 - 1)V_{in}(s) + 3k] \\ &= H_{HP}(s)V_{in}(s) + K_{HP}(s), \end{aligned} \tag{3}$$

where $H_{HP}(s)$ is the transfer function and $K_{HP}(s)$ is the offset function. Equation (3) is the closed form of the high pass output of the filter under the faulty OP_1, which is caused by a transistor fault existing in it. For example, for the case where M_{5_ds} is short at OP_1, $m_1 = m_2 = 0.00512$, $m_3 = 0.0277$ and $k = -0.0439$, Eq.(3) is plotted in Fig. 13(a) (solid curve), where the transfer curve obtained from the transistor level simulation is also plotted (dotted curve). It can be seen that the two curves agree exactly with each other.

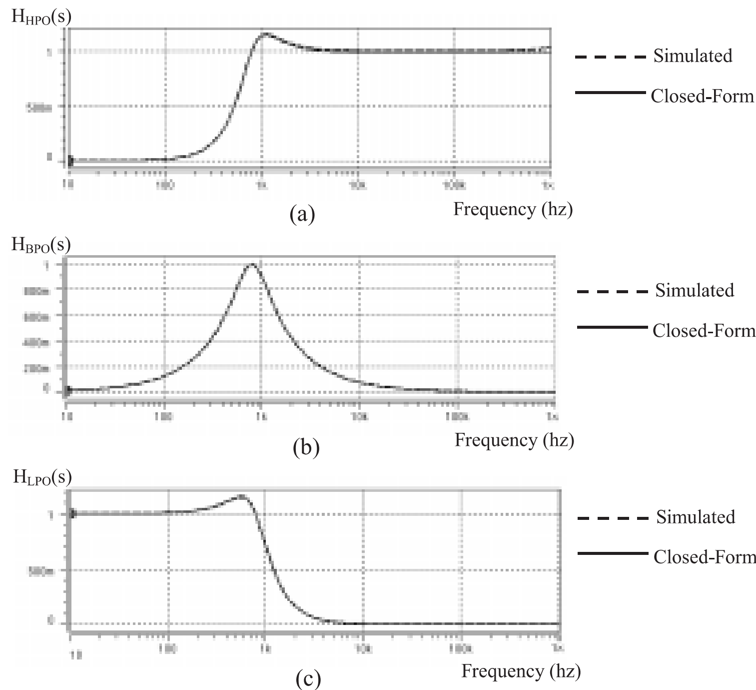

Fig. 13. Transfer functions of the closed-form analysis (solid curves) and transistor level simulation (dotted curves) for the M_{5_ds} short fault occurring at OP_1: (a) for the high pass output, (b) for the band pass output, (c) for the low pass filter.

In a similar way, we can obtain the transfer functions and the offset functions for the other two BPO and LPO outputs of the filter:

$$H_{BPO}(s) = \frac{(1.96928\times 10^{-4})s}{(4\times 10^{-8})s^2 + (1.9662\times 10^{-4})s + 0.98464},$$

$$K_{BPO}(s) = \frac{(2.634\times 10^{-5})s}{(4\times 10^{-8})s^2 + (1.9662\times 10^{-4})s + 0.98464},$$

$$H_{LPO}(s) = \frac{-0.98464}{(4\times 10^{-8})s^2 + (1.9662\times 10^{-4})s + 0.98464},$$

$$K_{LPO}(s) = \frac{-0.1317}{(4\times 10^{-8})s^2 + (1.9662\times 10^{-4})s + 0.98464}.$$

The curves obtained from the above equations are plotted in Figs. 13 (b) and (c) along with the simulation curves, respectively. They also agree with each other very well.

In the above offset functions, it is seen that the offset fault of OP_1 is more easily observed at the LPO output instead of at its own output since only $K_{LPO}(s)$ is nonzero when $s = 0$; i.e., only $K_{LPO}(s)$ can be measured by means of DC testing.

8. CONCLUSIONS

In this paper, a new behavior level fault model for the OP, operated under closed loop configurations, has been proposed to describe the faulty behavior of the circuit. This model consists of the offset fault and the limited-current fault. The offset fault lumps the fault effects of the transistor faults of the OP into an offset voltage in the input of the circuit, thus making the model extremely simple when used in fault simulation. It has been found that the offset voltage, in most cases, has a linear relationship with the input and is composed of two parts, i.e., $F_{os} = mV_{in} + k$ where m is the gain attenuation part and k is the input offset part. The values of m and k are independent of the input. The other fault, the limited-current fault, explains the piecewise linear form of the input-offset relationship and describes the fault effect of the slew rate for the OP. They have been verified for three closed-loop configurations, namely, the inverting configuration, the non-inverting configuration and the unit gain buffer configuration at the transistor level for all transistor faults. This model can well describe the DC behaviors of all the soft faults and 92.5% of the hard faults. Moreover, the DC behaviors can be applied to AC fault simulation when the faulty OP, caused by transistor faults, still exhibits a single dominant pole behavior and the frequency of the AC input does not exceed the cutoff frequency of the OP.

When this fault model is used in fault simulation, the closed-loop OP is treated as ideal and only the faulty offset voltage is added to the circuit. This significantly reduces the analog fault simulation time with accuracy and makes closed-form frequency response analysis of the faulty analog circuit feasible when the closed loop OP is used as a basic building block in the circuit. The fault model, when used in specification-driven testing, can identify transistor faults which drive the circuit out of its specification; when used in fault model-driven testing, it can tell what the output of the faulty circuit will be when a fault is injected.

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