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Temperature-dependent characteristics of pulse-laser-deposited (Pb, Sr)TiO_3 films at low temperatures

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ABSTRACT Pulsed laser deposition (PLD) of (Pb, Sr)TiO_3 (PSrT) film on $Pt/SiO_2/Si$ at low substrate temperatures (T_s), ranging from 300–450 °C, has been investigated. As T_s increases, the films reveal coarsening clusters, improved crystallization of the perovskite phase, distinct capacitance–electric field (C–E) hysteretic loops and a larger dielectric constant. The 350 °C-deposited film shows strong (100) preferred orientation and optimum dielectric properties with the dielectric constant of ~ 620. The current density increases as the measurement temperature and the electric field increase. Moreover, PSrT films exhibit a strong negative temperature coefficient of resistance (NTCR) behavior at temperatures ranging from 100 to 390 °C.

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1 Introduction

Ferroelectric semiconducting materials, with perovskite structure, have received much attention lately for their temperature coefficient of resistance (TCR) properties [1–8]. Of these materials, (Pb, Sr)TiO_3 (PSrT) have aroused considerable interest in the composite effect of negative and positive TCR (NTCR and PTCR), first found in 1988 [3]. In addition, PSrT has a relatively low sintering temperature compared to conventional barium titanate [4]. In past studies [3–8], PSrT ceramics are found to exhibit an NTCR behavior below the Curie temperature (T_c) and a PTCR effect above T_c). Moreover, PSrT solid-solution is constituted of $SrTiO_3$ (STO) and $PbTiO_3$ (PTO) and its T_c) can be linearly adjusted from −220 °C to 490 °C by varying the lead (Pb) content [9, 10]. The effect of Pb substituted by strontium (Sr) in the PTO film will decrease the crystallization temperature and offers a good control of the dielectric properties at room temperature [11, 12]. The TCR effect of PSrT bulk prepared by conventional ceramic solid state sintering processes has been reported [4–8]. However, there is a lack of sufficient studies on the TCR properties of PSrT films, which can be used as a thermistor sensor embedded into micro-electro-mechanical systems (MEMS). As a consequence, the subject needs further investigations into the film properties.

Mostly, ferroelectric thin films require low-temperature processes for integrated circuits (IC) and MEMS applications to prevent the formerly-fabricated structure from thermal damage. Nevertheless, depositions of ferroelectric lead-titanate films, such as PTO and Pb(Zr, Ti)O_3 (PZT), are usually conducted at high-temperatures (> 600 °C) to obtain the good crystallinity of a perovskite structure [13]. The high-temperature (> 450 °C) process will result in the volatilization of lead oxide (Pb-O compounds) in lead-titanate-based thin films [14, 15], which in turn degrades the microstructure and affects the film composition. Thus, a relatively low-temperature process (≤ 450 °C) is desirable for the deposition of PSrT thin films.

To deposit PSrT films, a pulsed-laser deposition (PLD) technique is conducted because of its simplicity, versatility, and capability of growing a wide variety of stoichiometric oxide films without subsequent high-temperature annealing [16]. The PLD process consists of three steps [16]: (i) vaporization of a target material by laser beam, (ii) transport and interaction of a vapor plume with a background ambient, and (iii) condensation of the ablated material onto a substrate where a thin film nucleates and grows. Therefore, the structural and the electrical characteristics of PLD ferroelectric films are strongly affected by the processing parameters, such as deposition temperature, laser energy, and oxygen ambience. Some previous works regarding the dielectric and ferroelectric properties of PLD PSrT films have been reported [17–21]. To our knowledge, much less is known about the TCR effect of PLD PSrT films. In this work, the temperature dependent properties and electrical characteristics of PLD PSrT films deposited at low-temperatures (≤ 450 °C) will be addressed.

2 Experimental procedures

Platinum (Pt) film, 100 nm thick, was sputtered onto SiO_2/p-type Si as a bottom electrode and was followed by annealing at 450 °C for 30 min. in an N_2 ambient to improve the adhesion between the Pt and SiO_2. Thin PSrT films

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(200 nm thick) were then deposited on the $Pt/SiO_2/Si$ substrate by a PLD system (Lambda Physik Excimer Laser LPX 210i, using KrF, $\lambda = 248$ nm). A set of optical lens was used to focus the laser beam over the $((Pb_{0.6}Sr_{0.4})TiO_3$ target in a vacuum chamber. The vacuum chamber was pumped down to a base pressure of 0.1 mTorr and then refilled with O_2 as the working gas. The PSrT target was prepared by conventional ceramic fabrication process [16]. During deposition, the target material was vaporized by the laser beam. The vaporized species transferred and deposited on the substrate heated by a thermal heater. The target to substrate distance was 4 cm. The deposition temperature (substrate temperature, T_s), which was calibrated at the wafer upper surface, varied from 300 °C to 450 °C. During the PLD process, the oxygen partial pressure was kept at 80 mTorr. The laser pulsed rate was 5 Hz, and the average laser power density (laser energy) was 1.55 J/cm^2 per pulse.

The film thickness and the surface morphology of PSrT films were examined by a field emission scanning electron microscopy (FESEM, S-4000, Hitachi). An X-ray diffractometer (D5000, Siemens, using Cu K_α, $\lambda \sim 0.154$ nm) was employed to analyze the crystallinity of the films. The Pt top electrodes, with a thickness of 100 nm and a diameter of 75 μm, were then deposited by sputtering and patterned by a shadow mask process to form a metal/ferroelectric/metal (MFM) capacitor structure. The noble metal Pt, with low resistivity, is considered as the best electrode for Pt/PSrT/Pt capacitors because of its small leakage current, low power consumption, low RC delay, and good thermal stability for lead-based perovskite materials [14].

An automatic measurement system that combines an IBM PC/AT, semiconductor parameter analyzer (4156C, Agilent Technologies) and a probe station with an embedded heater was used to measure the current–voltage (I–V) characteristics as a function of measurement temperature (T_m) ranging from 30 to 390 °C. The TCR values were evaluated from the temperature dependent leakage current data. A capacitance–voltage (C–V) analyzer (Package 82 system C–V 590, Keithley) was also applied to measure C–V curves at 100 kHz, and the dielectric constant was extracted from the C–V measurements.

3 Results and discussion

Figure 1a presents a cross-sectional SEM micrograph of PLD PSrT films deposited at $T_s = 400$ °C on $Pt/SiO_2/Si$, with the columnar-like structure. The growth of PSrT films is strongly influenced by the deposition temperatures (T_s). As exhibited in Fig. 1b, as the T_s increases, the clusters gradually coarsen and become more rounded. The surfaces of PSrT films are mostly dense without any cracks at T_s from 300 to 450 °C.

Figure 2 displays X-ray diffraction patterns of PSrT films deposited on $Pt/SiO_2/Si$ (100) wafers at various T_s. A mono phase of $(Pb_{1-x}Sr_x)TiO_3$ perovskite structure is obtained [9, 11, 12, 17]. There are two reasons for the crystallization of PSrT perovskite phase at low temperatures (≤ 450 °C): (i) the addition of Sr makes the crystallization temperature of PSrT lower than that of PZT [15], and (ii) the PLD technique could preserve the stoichiometric ratio of the

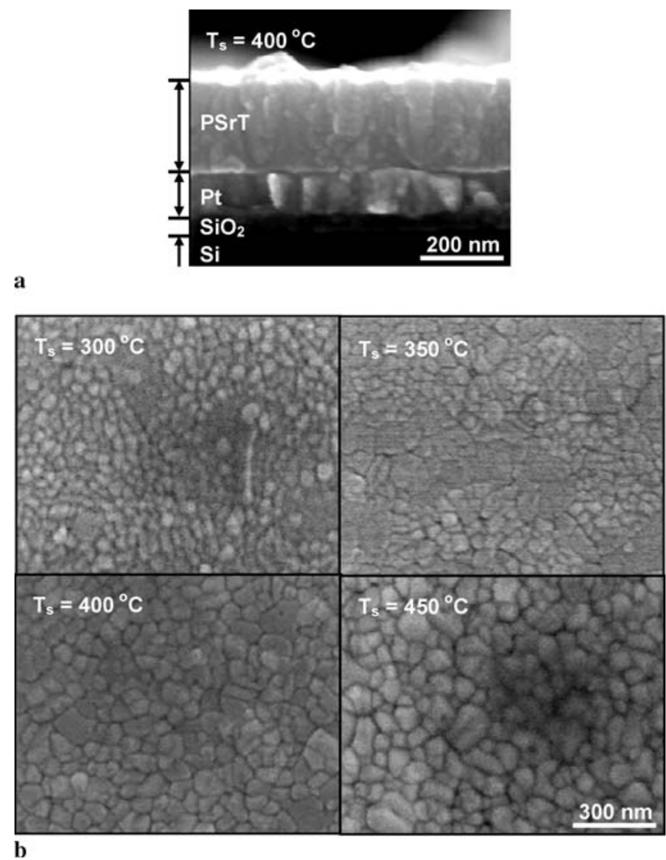

FIGURE 1 SEM (**a**) cross-sectional and (**b**) surface morphologies of PLD PSrT films deposited at various substrate temperatures (T_s) on $Pt/SiO_2/Si(100)$ wafers

target material [16]. The X-ray peak intensity at various deposition temperatures has been normalized by keeping the Pt(111) peak with the same height. The intensities of the (100) and (110) peaks increase significantly with the increase of T_s from 300 °C to 400 °C but decrease at $T_s = 450$ °C. The $(Pb_{1-x}Sr_x)TiO_3$ films had a tetragonal structure with a prominent (100) peak for $x < 0.5$ and a cubic structure with a strong (110) peak for $x \geq 0.5$, as reported in previous works [11, 12].

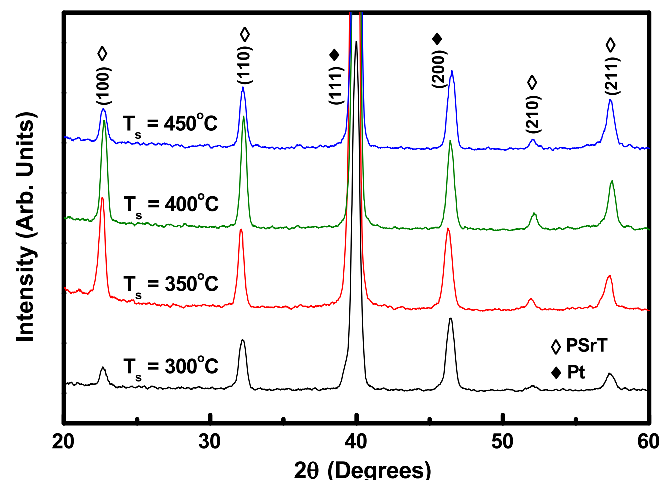

FIGURE 2 X-ray diffraction patterns of PSrT films deposited at various T_s on $Pt/SiO_2/Si(100)$ wafers

Kang et al. [11] also stated that the split (110) peaks near $31° < 2\theta < 33°$ tended to merge at $x > 0.5$, suggesting that the structure of PSrT films is tetragonal and the composition may be close to the stoichiometric composition of the $(Pb_{0.6}Sr_{0.4})TiO_3$ target.

Figure 3a gives the 100 kHz capacitance versus electric field (C–E) characteristics for PSrT films deposited at various T_s. The figure presents the typical C–E hysteretic characteristics of ferroelectric materials. The capacitance shows a maximum value at negative bias, according to the coercive field (E_c) of the hysteresis loop, when the applied field sweeps from +200 kV/cm to −200 kV/cm. However, the maximum capacitance appears at positive E_c when the applied field sweeps in the reverse direction. It is argued that the asymmetric C–E loops are possibly due to different configurations of the electrodes. The asymmetric C–E loop may be associated with the interfacial asymmetry induced by thermal processes (i.e. the top and bottom electrodes are subjected to different thermal processes) [22], and/or the different electrode areas (i.e. the area of the bottom electrode is larger than that of the top electrode, as defined by the shadow mask). The distinct C–E hysteresis loops suggest the existence of ferroelectricity for films deposited at 300–450 °C. Since the polarization of the lead-titanate-based crystal is maximal in the (100) direction, the polarization of the film with stronger (110) orientation is weaker than that with stronger (100) orientation [14, 23]. On the basis of Fig. 2, the diffraction intensity ratios, addressed as $I_{100}/(I_{100} + I_{110})$, are 31.4%, 65.4%, 55.8% and 49.3% at $T_s = 300$, 350, 400, and 450 °C, respectively. Hence, it suggests that the better ferroelectricity and more distinct C–E loops can be obtained for films prepared at $T_s = 350$–400 °C due to the strong (100) preferred orientation as shown in Fig. 2. The zero-field capacitance, in terms of the dielectric constant, depends considerably on the T_s. Figure 3b displays the effect of T_s on dielectric constant and $(\varepsilon_{T_s} - \varepsilon_{300})/\varepsilon_{300}$, where ε_{T_s} and ε_{300} are the dielectric constant for films deposited at T_s and 300 °C, respectively. The dielectric constant has a maximum value of ~ 620 for 350 °C deposited films. Besides, the dielectric properties of the films depend on the deposition temperatures, a 50 °C change in T_s results in 72% change in the dielectric constant. Furthermore, films with

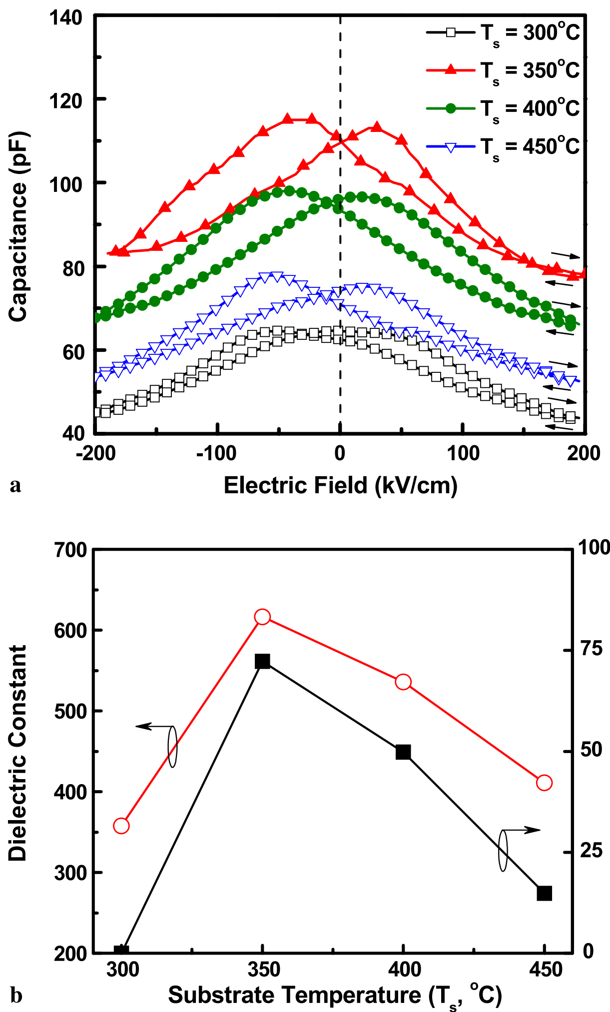

FIGURE 3 (**a**) Capacitance–electric field (C–E) hysteresis loops and (**b**) dielectric constant and $(\varepsilon_{Ts} - \varepsilon_{300})/\varepsilon_{300}$ of Pt/PSrT/Pt capacitors prepared at various T_s, where ε_{Ts} and ε_{300} are the dielectric constant for films deposited at T_s and 300 °C, respectively

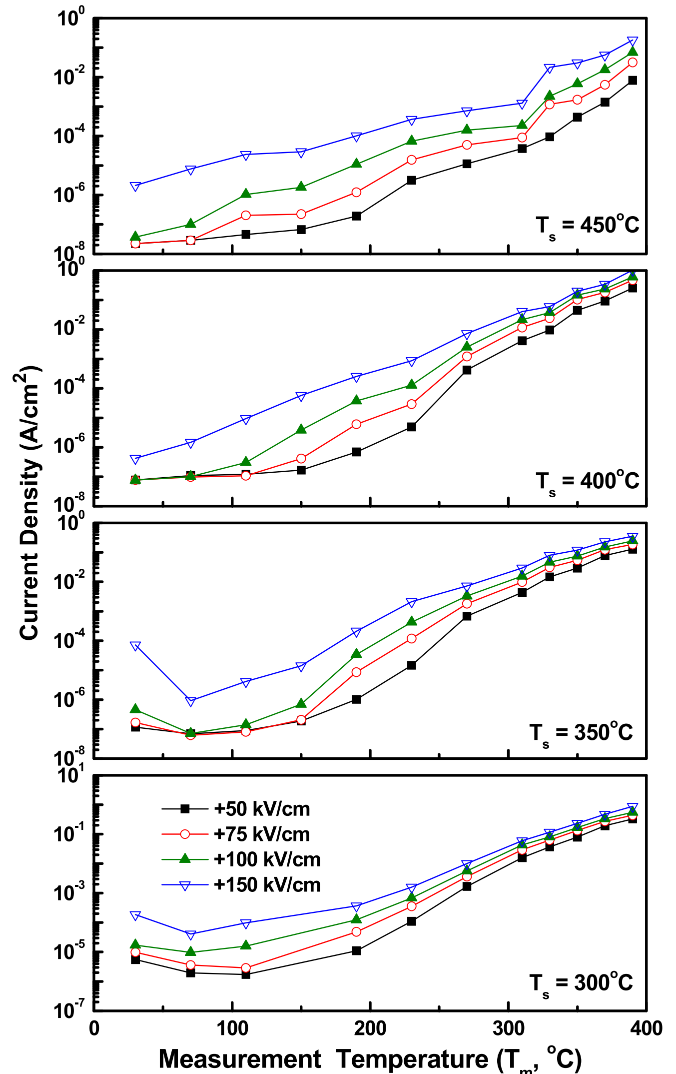

FIGURE 4 Current density versus measurement temperature characteristics of Pt/PSrT/Pt capacitors prepared at various temperatures (T_s) as a function of the biased field

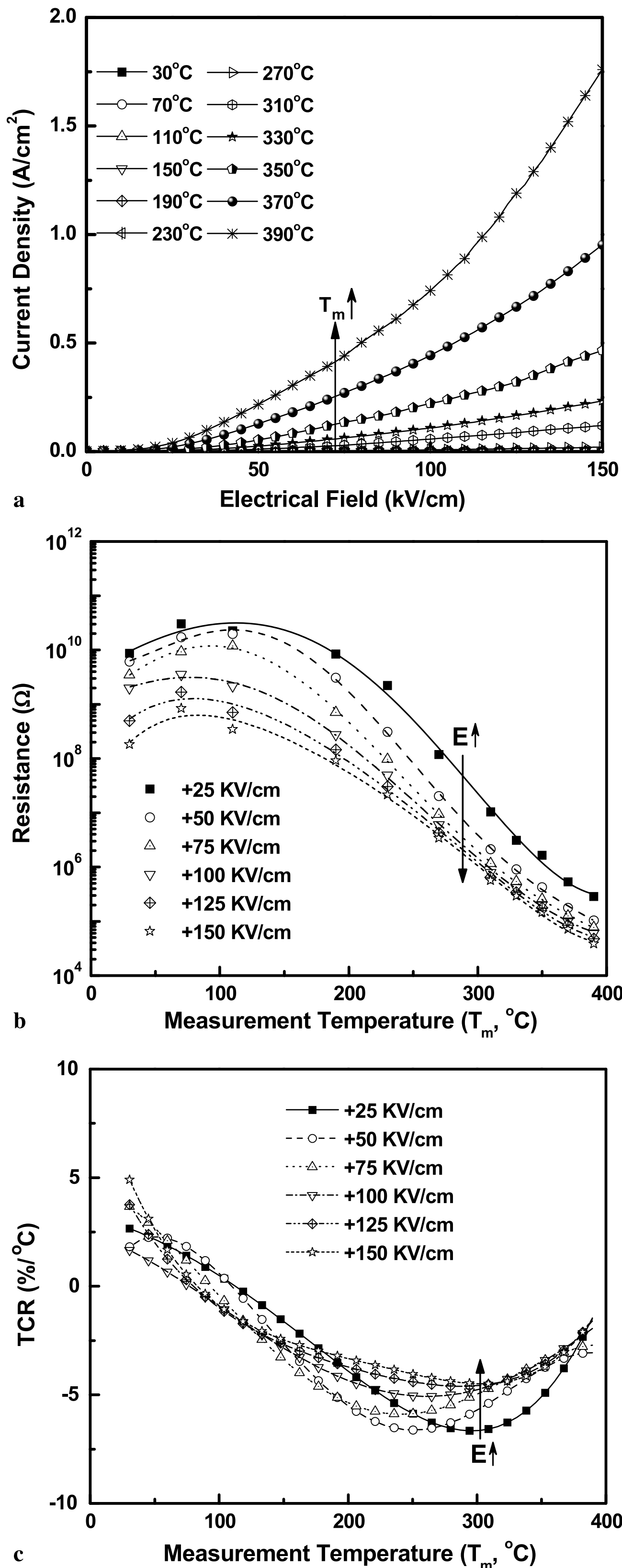

FIGURE 5 (**a**) Current density versus electric field (J–E) curves, (**b**) resistance-temperature (R–T_m) curves and (**c**) TCR plots for Pt/PSrT/Pt capacitors prepared at 300 °C

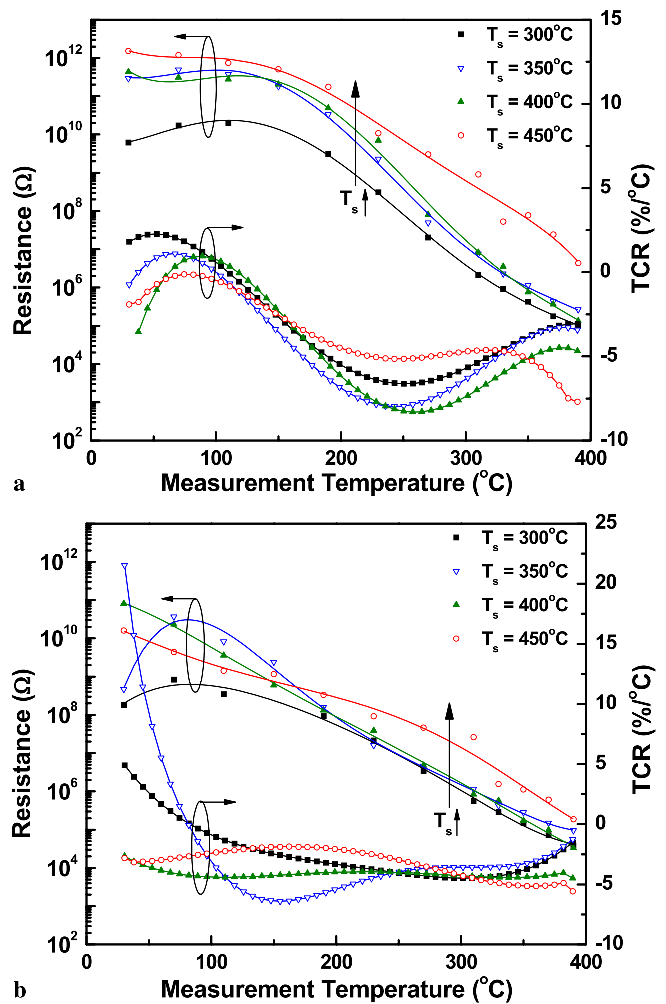

FIGURE 6 Resistance–temperature curves and TCR plots of Pt/PSrT/Pt capacitors prepared at various temperatures (T_s) biased at (**a**) +50 kV/cm and (**b**) +150 kV/cm

enhanced (100) texture exhibit larger dielectric constant, as suggested in Figs. 2 and 3.

Figure 4 reveals that the temperature dependence of the current density (J) versus the applied field for films deposited at various T_s. The current density increases as the temperature of measurement (T_m) and electric field increase. For J–T_m curves of the PSrT capacitor biased at +50 kV/cm in Fig. 4a, the current density (0.08 A/cm^2) at $T_m = 390\,°C$ is around 6 orders of magnitude higher than that (from 0.02 μ A/cm^2) at $T_m = 30\,°C$. However, when the PSrT capacitor is biased at +150 kV/cm (Fig. 4a), the current density (0.18 A/cm^2) at $T_m = 390\,°C$ is approximately 4 orders of magnitude larger than that (2.12 μA/cm^2) at $T_m = 30\,°C$. As a result, J is more sensitive to T_m when the films are biased at a low electric field. In addition, the substrate temperature (T_s) affects the film resistance while the J–T_m curves biased at different fields vary as T_s increases. Figure 5 shows the effects of temperature (T_m) and the biased field on the current density, dc resistance (R) and temperature coefficient of resistance (TCR) for Pt/PSrT/Pt capacitors prepared at 300 °C. The leakage current density increases with the increase of temperature (T_m) and biased fields (Fig. 5a), while the resistance also decreases with the increase of applied bias field (Fig. 5b), where the

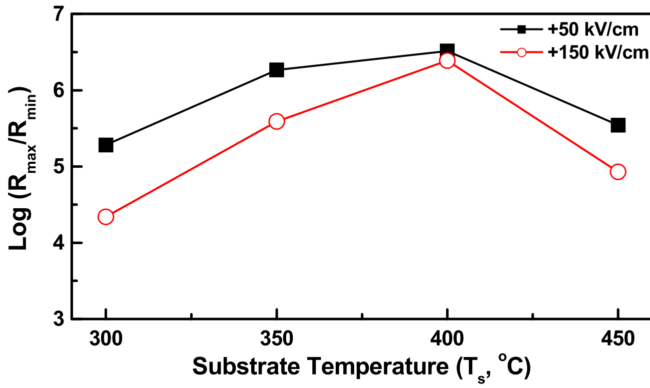

FIGURE 7 The log of the resistance ratio, (log (Rmax/Rmin)), of PSrT films deposited at various substrate temperatures (T_s), where R_{max} and R_{min} are the maximum and minimum of the film resistance measured from 30 to 390 °C

symbols at each applied field are extracted from J–E curves and the lines represent fitted results. The values of R increase slightly with increasing T_m from room temperature to ~ 100 °C (i.e. a positive TCR, PTCR) and then decrease with T_m (i.e. a negative TCR, NTCR), as exhibited in Fig. 5c. The phenomenon of strong NTCR, the values of resistance reduce with increasing T_m and biased fields, could be connected to the decrease of the resistance of semiconducting materials when the temperature increases. The TCR, as described by the following equation [1]

$$\mathrm{TCR} = \frac{1}{R}\left(\frac{\mathrm{d}R}{\mathrm{d}T_m}\right), \quad (1)$$

exhibits a minimum at $T_m \sim 250$ °C except for that at +25 kV/cm, possibly due to the unstable J–E measurement biased at such ultra-low electrical field. Thus, the J–E data at +50 and +150 kV/cm were selected to analyze the effect of deposition temperature (T_s) on the temperature dependence of R and the TCR properties (Fig. 6). Films deposited at lower temperatures (T_s) have smaller insulation resistances, larger TCR and are more sensitive to temperature change. The bias field effects the temperature dependence of the film resistance, especially at higher temperatures ($T_m > 100$ °C). As seen in Fig. 6, the TCRs of films biased at +50 kV/cm are larger than those at +150 kV/cm, and this is important for PSrT films utilized as thermistor components in MEMS applications. The PLD PSrT films exhibit an apparent NTCR behavior, which is different from the bulk PSrT ceramics where a NTCR-PTCR transition is observed in the temperature range of 100–390 °C [4–8]. It is possible that the PTCR effect of PLD PSrT films appear only at temperatures above 390 °C, as reported by Chou et al. in their work on PSrT bulk ceramics [8]. The evolution of the temperature-resistance of PSrT films, which can estimate the Curie temperature (T_c) of PSrT by electrical measurement, has been reported by Lu, and Tseng [6], and Zhao et al. [5]. It implies that the Curie temperature of PSrT films is higher than 390 °C and no phase transition of ferroelectric–paraelectric would occur at temperatures below 390 °C. In this study, due to the hardware limit, the maximum of the measurement temperature (T_m) is 390 °C, hence, no ferroelectric-paraelectric transition is observed. Thus, without the phase transition, the effects of deposition temperature (T_s) on resistance and TCR are attributed to films physical characteristics, originating from the changes of crystallinity, microstructure and composition (i.e. preferred orientations, grain boundaries and oxygen vacancies).

Figure 7 shows the resistance ratio, (R_{max}/R_{min}), as a function of T_s, where R_{max} and R_{min} are the maximum and minimum of film resistance, respectively, measured from 30 to 390 °C as given in Fig. 6. Larger (R_{max}/R_{min}) are obtained when films biased at +50 kV/cm than those at +150 kV/cm, which is consistent with what is observed in Fig. 4. Besides, films deposited at 400 °C show the maximal (R_{max}/R_{min}) value. Table 1 summarizes the Curie temperature, resistance ratio, and TCR of PLD PSrT films in this study and the PSrT bulk ceramics reported in the literature. It is noticed that

	This Work	[4]	[5]	[6]	[7]	[8]
Composition	PSrT	PSrT	PSrT	Y-doped PSrT	Y-SiO_2-doped PSrT	Y-SiO_2-doped PSrT
Film/ceramic bulk	Film	Ceramic bulk	Ceramic bulk	Ceramic bulk	Ceramic bulk	Ceramic bulk
Preparation method	PLD	CS **	CS **	CS **	CS **	CS or MS **
Electrode material	Pt	In-Ga alloy	In-Ga alloy	In-Ga alloy	NA *	In-Ga alloy
Process Temperature (°C)	300 – 450	1100	950	1250	1080 – 1180	1150 or 1220
Measurment Temperature (T_m, °C)	30 – 390	RT-400	RT-400	RT-500	RT-450	RT-700
Curie temperature (T_c, °C)	NA *	150 – 200	123 – 212	140 – 280	165	CS: 210, MS: 390 **
NTCR/PTCR Effect	Strong NTCR	NTCR-PTCR Composite	NTCR-PTCR Composite	NTCR-PTCR Composite	NTCR-PTCR Composite	NTCR-PTCR Composite
log (R_{max}/R_{min})	NTCR: 4.34 – 6.51	NTCR: 0.45 – 1.38 PTCR: 4.85 – 5.25	NTCR: 0.11 – 1.86 PTCR: 3.23 – 4.5	NTCR: 0.7 – 1.5 PTCR: 3.6 – 5	NTCR: 2.7 PTCR: 4.7	NTCR: 1 PTCR: 2.5
TCR (%/°C)	−8.3 – +21.5	NA *	NA *	NA *	−3.54 – +6.61	NA *

* NA: not available
** CS: conventionally sintered, MS: microwave sintered

TABLE 1 Curie temperature (T_c), the log of the resistance ratio (log R_{max}/R_{min}), and the TCR of PSrT films in this work and PSrT bulk ceramics reported in the literature

the low temperature prepared PLD PSrT films exhibit strong NTCR behavior with the larger values of (R_{max}/R_{min}) than the PSrT ceramics do [4–8]. This suggests that film-type PSrT is a better candidate for application to thermistor sensors due to its large resistance range in the temperature range of interest (30–390 °C).

4 Conclusions

Low-temperature PLD PSrT films, deposited at temperatures ranging from 300 to 450 °C, exhibit perovskite phases. The deposition temperature (substrate temperature, T_s) strongly affects the crystallinity, morphologies and electrical properties of PSrT films. As T_s increases, the films reveal coarsening clusters, preferred (100) orientation, distinct C–E hysteretic loops, and larger dielectric constants. The 350 °C-deposited film shows strong (100) diffraction intensity and optimum dielectric properties with the dielectric constant of ~ 620. The current density increases with temperature (T_m) and biased fields. The NTCR behavior is observed in the temperature range of 100–390 °C. Furthermore, PLD PSrT films exhibit strong NTCR behavior with a larger resistance range (log (R_{max}/R_{min}) values of 4.3 – 6.5) than the PSrT ceramics do. In addition, deposition temperature affects both the leakage current density and the temperature dependence of leakage current density of the films. As a result, the larger resistance range of the PLD PSrT films renders them a better candidate for application as thermistor sensors.

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