Reduction of Source/Drain Series Resistance and Its Impact on Device Performance for PMOS Transistors with Raised $Si_{1-x}Ge_x$ Source/Drain

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***Abstract*—P-channel MOS transistors with raised $Si_{1-x}Ge_x$ and Si source/drain (S/D) structure selectively grown by ultra high vacuum chemical vapor deposition (UHVCVD) were fabricated for the first time. The impacts of $Si_{1-x}Ge_x$ and Si epitaxial S/D layer on S/D series resistance and drain current of p-channel transistors were studied. Our result show that the new device with $Si_{1-x}Ge_x$ raised S/D layer depicts only half the value of the specific contact resistivity and S/D series resistance (R_{SD}), compared to the device with Si raised S/D layer. The improvement is even more dramatic, when comparing to the conventional device without any raised S/D layer, i.e., R_{SD} of the new device with $Si_{1-x}Ge_x$ raised S/D is only about one fourth the value of the conventional device. Moreover, the device with raised SiGe S/D structure produces a 29% improvement in transconductance (g_m) at an effective channel length of 0.16 μm. These performance improvements, together with several inherent advantages such as self-aligned selective epitaxial growth (SEG) nature and the resultant T-shaped gate structure, make the new device with raised $Si_{1-x}Ge_x$ S/D structure very attractive for future sub-0.1 μm p-channel MOS transistors.**

***Index Terms*—RSD MOSFET, selective epitaxial growth, source and drain series resistance ((R_{SD}), strained $Si_{1-x}Ge_x$, ultra high vacuum chemical vapor deposition.**

I. Introduction

As the device is scaled down to sub-0.1 μm region, the source/drain area needs to be scaled proportionally, while keeping a low specific contact resistivity (ρ_c) in order to maintain a high current drive on the scaled transistors [1]. However, it has become increasingly difficult to use conventional ion-implantation to form shallow junctions, due to channeling effects and the tradeoff between radiation damage annealing and low thermal budget [2]. Recently, out-diffusion from a doped layer has received renewed interest for ultra-shallow junction formation [3]. Shallow junctions obtained by out-diffusion from in-situ doped or ion-implanted p^+/n^+ SiGe layer have been reported [4]. $Si_{1-x}Ge_x$ is particularly suitable for such application, because it can be selectively deposited onto the exposed S/D areas. Besides, $Si_{1-x}Ge_x$ can be selectively etched with high selectivity to Si and SiO_2 [5]. Furthermore, $Si_{1-x}Ge_x$ has lower Schottky barrier height with respect to p^+ junctions because of the reduced band gap, which is beneficial for achieving low contact resistivity [6], [7]. However, to the best of our knowledge, there has been no literature report regarding the application of p^+-SiGe epitaxial layer to form p-channel transistors with raised S/D structure. Although Uchino *et al.*[8] has reported the use of n^+-SiGe epitaxial layer to form n-channel transistors with raised S/D, however, the raised S/D structure in their p-channel transistors were formed by p^+-Si material only. In this work, p-channel MOS transistors with raised $Si_{1-x}Ge_x$ S/D structure were fabricated, for the first time. The impacts of using $Si_{1-x}Ge_x$ S/D layer on contact resistance and device performance are reported.

II. Experiment

P-channel MOS transistors with raised source/drain structure were fabricated on 6-in (100) 10–15 Ω-cm wafers. Briefly, 550 nm LOCOS field oxide was used for device isolation. After V_T-adjust implant and anti-punchthrough implant, a 4-nm gate oxide and polysilicon gate were formed. The gate was defined by g-line lithography and further ashed down to 0.18 μm. Afterward, the source/drain extension implant was performed by BF_2 at 10 KeV with 1×10^{15} cm^{-2} dosage. An 800 °C, 20 min furnace anneal and RTA 1050°C, 10 s for activation of gate and S/D extension took place at this stage. The activation anneal must be processed before SiGe epitaxy because strained SiGe layer cannot tolerate large thermal budget. Next, a 150 nm sidewall spacer was formed by a conformal TEOS deposition and subsequent RIE-etch. Then, wafers were split to receive SiGe or Si selective epitaxial growth (SEG) on the exposed S/D regions by ANELVA SRE-612 cold-wall ultra-high vacuum chemical vapor deposition (UHVCVD) system. The standby base pressure was kept at 2×10^{-10} torr. For growing B-doped strained $Si_{1-x}Ge_x$ layers, Si_2H_6, GeH_4, and 1% B_2H_6 diluted in H_2 were introduced with a growth rate of 41 Å/minute for $Si_{0.91}Ge_{0.09}$ and 43 Å/minute for $Si_{0.86}Ge_{0.14}$ at 550 °C. The maximum available time for selective epitaxial growth of $Si_{0.91}Ge_{0.09}$ or $Si_{0.86}Ge_{0.14}$ layer (i.e., epitaxy on Si region but not on oxide region) at 550 °C is above 90 min. Samples with epitaxial thickness of 50 nm and 100 nm were processed in order to study the effect of the epitaxial layer thickness on the device performance. Afterward, p^+ S/D implant was

Manuscript received July 26, 1999; revised January 26, 2000. This work was supported in part by the National Science Council under Contract NSC88-2215-E009-048. The review of this letter was arranged by Editor C. Wann.

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Publisher Item Identifier S 0741-3106(00)07259-1.

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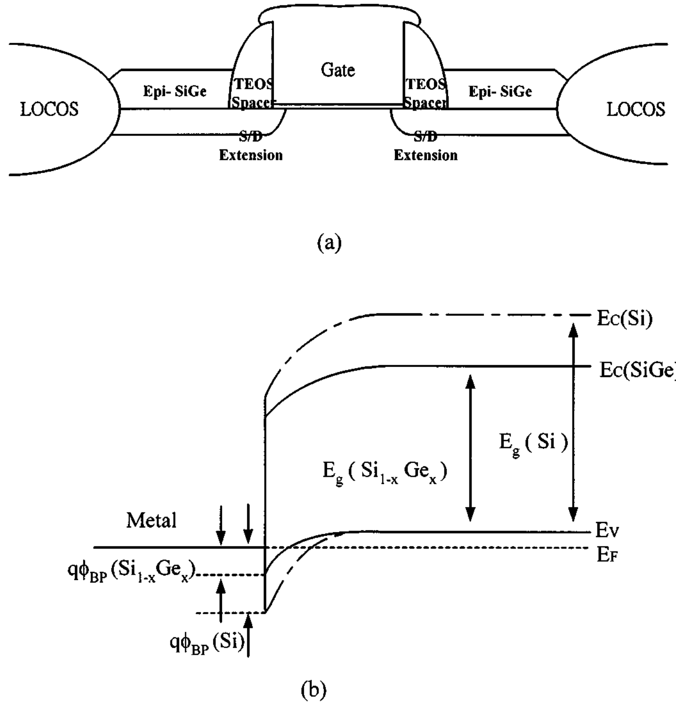

Fig. 1. (a) Schematic cross section of raised source/drain transistors and (b) energy band diagram of metal/$p^+Si_{1-x}Ge_x$ junction.

performed by BF_2 at 20 KeV with 5×10^{15} cm^{-2} dosage. This is followed by rapid thermal annealing (RTA) at 950 °C for 10 s. For comparison, conventional MOS transistors (i.e., without any raised S/D layer) were also fabricated in the same run. The schematic cross-section of the resultant raised source/drain MOS transistor (RSDMOSFET) is shown in Fig. 1(a). It is worthy to note that a T-shaped gate structure is formed simultaneously as a result of lateral overgrowth during S/D epitaxial growth. Finally, Ti/TiN/Al-Si-Cu/TiN was deposited and patterned to complete the contact metallization.

III. Results and Discussion

The barrier height ($q\phi_{\rm BP}$) formed at metal/semiconductor interface is known to be a critical factor in determining the contact resistivity. Fig. 1(b) shows the energy band diagram of a metal/$p^+Si_{1-x}Ge_x$ junction. The energy-band gap (Eg) of $Si_{1-x}Ge_x$ changes from 1.12 to 0.66 eV with increasing Ge mole fraction [9]. The conduction band edges are almost at the same level in metallurgical Si and SiGe junction. However, the potential difference of the valence band will cause the lowering of the Schottky barrier height (SBH) in metal/$p^+Si_{1-x}Ge_x$ junction [10]. For pseudomorphic p-$Si_{0.86}Ge_{0.14}$ layer, the SBH is expected to be lower than that of metal/p^+Si by 0.07 eV [10], thus effectively reduces the specific contact resistivity (ρ_C).

Measured S/D series resistance ($R_{\rm SD}$), specific contact resistivity (ρ_C), and sheet resistance ($\rho_{\rm SH}$) are summarized in Table I for samples with different process conditions. The specific contact resistivity was measured by transmission line method (TLM), while the S/D series resistances ($R_{\rm SD}$) were extracted by "shift and ratio" (S&R) method [11]. From Table I, it can be seen that $R_{\rm SD}$ is significantly improved for devices

TABLE I
MEASURED S/D SERIES RESISTANCE ($R_{\rm SD}$), SPECIFIC CONTACT RESISTIVITY (ρ_C), AND SHEET RESISTANCE ($\rho_{\rm SH}$)

PMOS Sample No.	Epi. Thickness (Å)	Ge mole Fraction x (%)	Spec. Contact Resistivity ρ_C (Ω-cm²)	Sheet Resistance ρ_{SH} (Ω/□)	S/D Series Resistance R_{SD} (Ω)
Control Sample	0	0	3.91×10^{-6}	130.68	93.25
1	500	0	3.20×10^{-6}	105.88	43.92
2	500	9	2.12×10^{-6}	111.22	31.45
3	1000	9	1.93×10^{-6}	84.46	19.23
4	500	14	1.62×10^{-6}	113.78	23.85
5	1000	14	1.81×10^{-6}	96.62	21.19

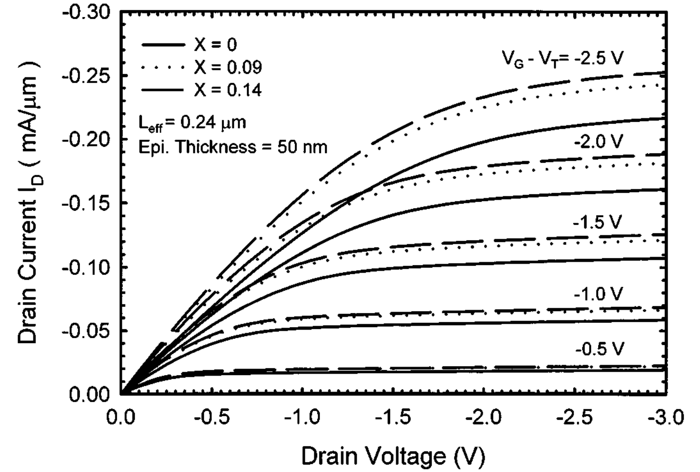

Fig. 2. Measured drain current I_D versus drain voltage V_D characteristics for RSD-MOSFET with different Ge mole fraction x. The effective channel length ($L_{\rm eff}$) is 0.24 μm, and the epitaxial thickness is 50 nm.

with SiGe RSD (~20 Ω), compared to devices with Si RSD (~44 Ω) and conventional MOSFET without RSD (~93 Ω). By comparing Samples 1 (50 nm Si), 2 (50 nm $Si_{1-x}Ge_x$ with $x = 9\%$), and 4 (50 nm $Si_{1-x}Ge_x$ with $x = 14\%$), it can be seen that for a given epitaxial thickness (e.g., 50 nm), ρ_C and $R_{\rm SD}$ decrease as Ge fraction (x) increases. It is believed that the decrease in ρ_C is the main reason for $R_{\rm SD}$ reduction. However, the sheet resistance ($\rho_{\rm SH}$) shows a slight increase with increasing x, which is probably due to incremental defects in pseudomorphic $p^+Si_{1-x}Ge_x$ layer. The value of ρ_C for Sample 2 (50 nm $Si_{1-x}Ge_x$ with $x = 9\%$) and Sample 3 (100 nm $Si_{1-x}Ge_x$ with $x = 9\%$) should be about the same. This is also true for Sample 4 (50 nm $Si_{1-x}Ge_x$ with $x = 14\%$) and Sample 5 (100 nm $Si_{1-x}Ge_x$ with $x = 14\%$), because ρ_C should be independent of the epitaxial thickness. The observed difference could be attributed to calculation errors, or defects during epitaxial process. On the other hand, by comparing Samples 2 (50 nm $Si_{1-x}Ge_x$ with $x = 9\%$) and 3 (100 nm $Si_{1-x}Ge_x$ with $x = 9\%$), there is about 24% improvement in $\rho_{\rm SH}$ as the epitaxial layer becomes twice as thicker, which also leads to a reduction of $R_{\rm SD}$.

Fig. 2 displays the I_D-V_D characteristics of RSDMOSFET's with the same epitaxial thickness (50 nm) but different Ge mole fraction x. The effective channel length was extracted by S&R method. It can be seen that the device with $Si_{0.86}Ge_{0.14}$ RSD produces a drive current (measured at $V_D = -2.5$ V and $V_G - V_T = -2.5$ V) of 246 μA/μm, which is 17%

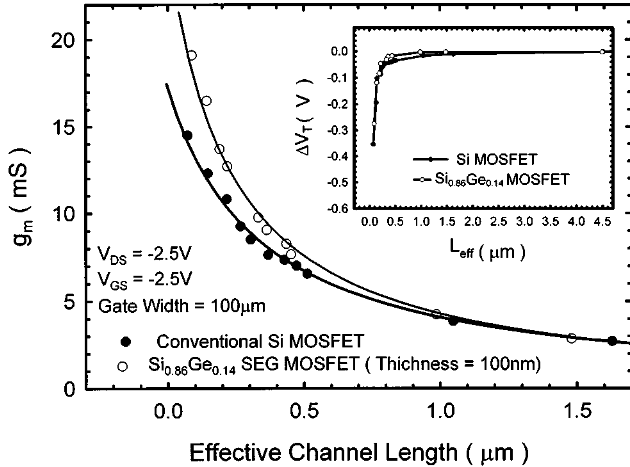

Fig. 3. Transconductance g_m as a function of effective channel length $(L_{\rm eff})$ for both RSD-MOSFET and conventional transistors. The insert figure shows the $\Delta V_{\rm TH}$ roll-off characteristics. The gate oxide thickness is 4 nm.

more than that of the device with Si RSD, both with the same effective channel length (e.g., 0.24 μm). The transconductance (g_m) as a function of effective channel length for both RSD $Si_{0.86}Ge_{0.14}$ MOSFET and the conventional Si MOSFET are plotted in Fig. 3. For $L_{\rm eff} = 0.5$ μm, $Si_{0.86}Ge_{0.14}$ MOSFET exhibits roughly 15% g_m improvement over the conventional Si MOSFET. However, as $L_{\rm eff}$ reduces to 0.16 μm, the g_m improvement of $Si_{0.86}Ge_{0.14}$ MOSFET's reaches 29% over that of the conventional counterparts. This illustrates the importance of maintaining a low series resistance as devices are scaled down, and makes the devices with $Si_{0.86}Ge_{0.14}$ RSD even more attractive for future sub-0.1 μm technologies. The short channel characteristics $(\Delta V_T = V_T\ (\text{long channel}) - V_T\ (\text{short channel}))$ are shown in the insert of Fig. 3, it can be seen that a slight improvement in threshold voltage lowering is also obtained on the devices with $Si_{0.86}Ge_{0.14}$ RSD.

IV. Conclusion

In this study, p-channel MOS transistors with raised $Si_{1-x}Ge_x$ source/drain were fabricated, for the first time, to study its impact on extrinsic resistance and device characteristics. Significant reduction of source/drain contact resistance by the epitaxial $Si_{1-x}Ge_x$ has been demonstrated. By employing a $Si_{1-x}Ge_x$ raised source/drain structure, the extrinsic component of the parasitic source-drain resistance can be reduced remarkably, resulting in improved drive current and transconductance for p-channel transistors. These performance improvements, together with several inherent advantages such as the self-aligned nature of selective epitaxial growth (SEG) and the resultant T-shaped gate structure, make it a very attractive device structure for future sub-0.1 μm salicided or nonsalicided p-channel MOS transistors.

Acknowledgment

The authors would like to thank Dr. H. C. Lin and Dr. T. S. Chao for their support and experimental assistance.

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