

# An Anomalous Crossover in $V_{th}$ Roll-Off for Indium-Doped nMOSFETs

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**Abstract**—The effects of indium channel implant energy on short-channel effect (SCE) and narrow channel effect (NCE) were studied on NMOS devices down to  $0.1 \mu\text{m}$  channel length. An anomalous crossover in  $V_{th}$  roll-off curves was observed, for the first time, on indium-implanted splits with different implant energies. This intriguing finding, together with the observed reduction in reverse narrow channel effect (RNCE) and effective channel length with reducing indium implant energy, can be consistently explained by the suppression of transient enhanced diffusion (TED) of channel impurity due to indium deactivation.

**Index Terms**—Indium, SSR.

## I. INTRODUCTION

AS MOSFET dimensions are scaled into subquarter-micrometer regime, an effective way to improve sub-threshold turn-off and to eliminate short channel effect (SCE) is to increase substrate doping. However, a uniform increase in substrate doping results in undesirable channel mobility reduction, junction capacitance increase, and high threshold voltage. To circumvent these problems, nonuniform channel implant has been proposed [1]–[3]. More recently, super-steep-retrograde (SSR)-channel has also been proposed as a viable scheme for transistors with channel length smaller than  $0.1 \mu\text{m}$ . By employing SSR, transistor enjoys a high driving current due to a low surface impurity scattering because of the lightly doped surface channel, while also maintaining a good  $V_{th}$ -roll-off behavior due to a higher substrate doping [4]. To achieve this goal, indium with a low diffusion coefficient at elevated temperature has been proposed as a suitable candidate to create SSR profiles for subquarter-micron nMOSFET.

In this letter, an anomalous crossover in  $V_{th}$  roll-off curves was observed, for the first time, on indium-implanted SSR devices. This intriguing finding, together with the observed reduction in reverse narrow channel effect (RNCE) and effective channel length with reduced indium implant energy, can be con-

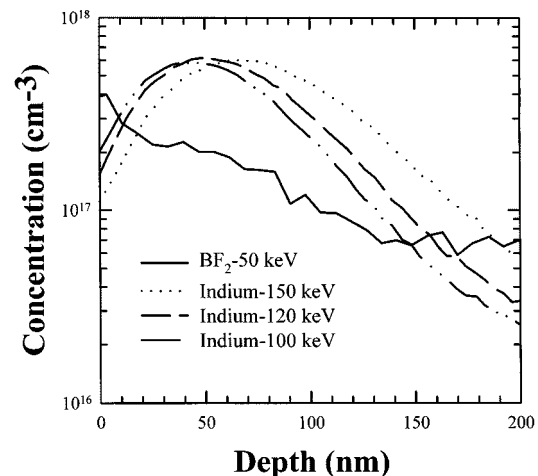


Fig. 1. SIMS profiles of indium and  $\text{BF}_2$  channel implantation.

sistently explained by the suppression of transient enhanced diffusion (TED) of channel impurity due to indium deactivation.

## II. EXPERIMENTAL

Devices with channel length down to  $0.1 \mu\text{m}$  were fabricated using shallow trench isolation (STI) and retrograde well. To form SSR channel, three different indium implantation energies, i.e., 100, 120 and 150 keV, with a dose of  $1 \times 10^{13} \text{ cm}^{-2}$  were conducted. Conventional devices with  $\text{BF}_2$  implant (at 50 keV,  $5 \times 10^{12} \text{ cm}^{-2}$ ) were also processed to serve as the control. Then, a 2.6-nm gate oxide was grown using rapid thermal oxidation (RTO), followed by the deposition of 200-nm gate polysilicon. After gate patterning, a 20-nm offset-space was used to reduce gate/drain capacitance. Ultrashallow extensions were formed by 4 keV As implant, followed by a boron pocket implant (20 keV,  $1 \times 10^{13} \text{ cm}^{-2}$ ). After the formation of  $0.1 \mu\text{m}$  thick sidewall spacer, a deep source/drain junction was formed by As ion implantation at 40 keV. Finally, wafers were annealed by a rapid thermal process (RTP) at  $1000 \text{ }^\circ\text{C}$  for 20 s, followed by  $\text{CoSi}_2$  salicidation process. Wafers were then processed through a standard backend flow to completion.

## III. RESULTS AND DISCUSSION

The resultant channel profiles by SIMS for In- and  $\text{BF}_2$ -implanted samples are shown in Fig. 1. The channel profiles are measured after all processing steps. Compared to  $\text{BF}_2$ -implanted control, In-implanted samples exhibit a lighter surface doping concentration and simultaneously a heavier doping

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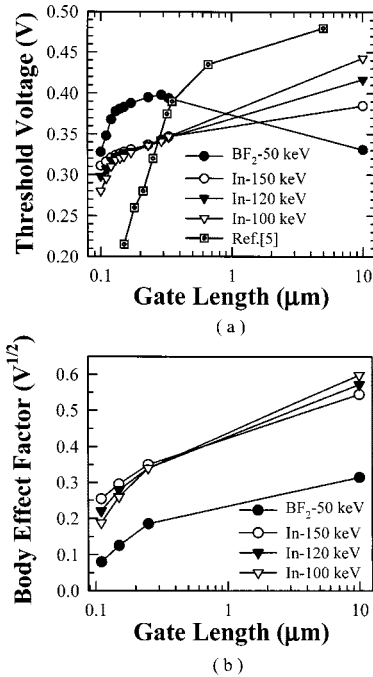


Fig. 2. (a)  $V_{th}$  roll-off characteristics as a function of gate length. (b) Body factor as a function of gate length.

concentration deeper in the channel. The threshold voltage, deduced from  $G_{m_{max}}$  method, versus channel length is plotted in Fig. 2(a). It can be seen that while the conventional BF<sub>2</sub>-implanted sample depicts a reverse SCE (RSCE), In-implanted samples all exhibit the normal  $V_{th}$  roll-off characteristics, i.e., threshold voltage decreases monotonically with decreasing channel length. A long distance roll-off, occurring on Indium-doped NMOSFET, has been observed [5], [6]. This indicates that transient enhanced diffusion (TED), which has been recognized as the cause for RSCE, is effectively suppressed in the In-implanted samples. More interestingly,  $V_{th}$  roll-off curves with different indium energies depict an unexpected "crossover." Specifically, In-implanted devices with the lowest implant energy of 100 keV depict the highest  $V_{th}$  among In-implanted splits for long channel devices, which is expected for their highest p-type surface concentration. However, contrary to the general concept that a high surface concentration should also result in less  $V_{th}$  roll-off, an unexpected trend is observed. As can be seen in Fig. 2(a), In (100 keV)-implanted devices actually depict the worst  $V_{th}$  roll-off among the In-implanted splits. As a result, an interesting "crossover" of the curves is observed for the In-implanted splits in the short channel regime. Fig. 2(b) shows the body factor versus channel length for these devices. Again, the body factors depict a crossover and are less severe for the short channel devices. Since the body effect depends only on the gate oxide thickness and channel doping distribution, it is evident that channel doping profile is modified as the channel length changes. We believe this intriguing phenomenon can be explained by indium deactivation reaction, i.e.,  $\text{In}^{(s)} + \text{Si}^{(i)} \leftrightarrow \text{In}^{(i)} + \text{Si}^{(s)}$  [7]. Since a large amount of Si interstitial ( $\text{Si}^{(i)}$ ) is generated by S/D extension implant, a higher surface indium dopant concentration can react with  $\text{Si}^{(i)}$  more efficiently, resulting in a more pronounced deactivation,

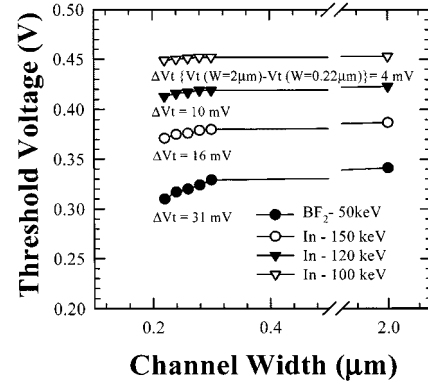


Fig. 3.  $V_{th}$  roll-off characteristics as a function of gate width.

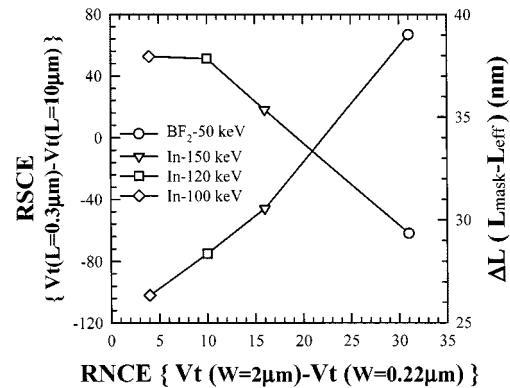


Fig. 4. Relationships among RSCE, RNCE, and gate to S/D overlap distance  $\Delta L$  ( $L_{mask} - L_{eff}$ ) for indium and BF<sub>2</sub> channel implantation.

causing an accelerated  $V_{th}$  roll-off for the short-channel devices. In addition, indium could become a donor-type when it is in the interstitial site ( $\text{In}^{(i)}$ ) [8], which further accelerates the effects of  $V_{th}$ -roll-off. Finally, it is also possible that indium may also act as a sink for silicon interstitial, and the reduced TED of boron may also contribute to the observed crossover.

The narrow channel effects are also studied. As shown in Fig. 3, BF<sub>2</sub>-implanted control shows the worst  $V_{th}$ -roll-off, while In (100 keV)-implanted split depicts only a minimal  $V_{th}$ -roll-off of only 4-mV. This is consistent with the proposed deactivated model that a significant amount of Si-interstitial is absorbed by the deactivated indium for the In (100 keV)-implanted split, so TED and therefore RNCE are reduced [9]. In fact,  $V_{th}$  shift due to RSCE is proportional to the  $V_{th}$  shift due to RNCE. As illustrated in Fig. 4, the difference between BF<sub>2</sub>- and In-implanted devices can be clearly seen. For the BF<sub>2</sub>-implanted control, TED dominates, resulting in a positive RSCE. For In-implanted devices, indium-deactivation dominates, which results in a negative RSCE and the corresponding reduction in RNCE. Finally, we have also estimated the dopant distribution under the gate edge by measuring the effective length. It has been shown that reduced TED leads to decreased effective channel length for a given poly-gate length [10], [11]. Therefore, it is expected that as the indium deactivation increases, the gate to S/D overlap distance  $\Delta L$  ( $L_{mask} - L_{eff}$ ) should increase. To confirm this, the  $\Delta L$  for the four samples are also plotted in Fig. 4. It can be seen clearly that as the indium deactivation increases,  $\Delta L$  also increases.

This is another evidence supporting our proposed model that TED is suppressed by indium deactivation effects.

#### IV. CONCLUSION

In this study, an anomalous crossover in  $V_{th}$  roll-off is reported for the first time on indium-implanted n-channel MOS transistors. We found that while devices with the lowest indium implant energy depict the highest threshold voltage at long channel length, they also depict the worst  $V_{th}$  roll-off and therefore the lowest threshold voltage at short-channel length. As a result, an interesting “crossover” is observed on the  $V_{th}$  roll-off curves among the indium-implanted splits with different implant energies. This interesting finding, together with the observed reduction in reverse narrow channel effect and effective channel length with reducing indium implant energy, can be consistently explained by the suppression of transient-enhanced diffusion due to indium deactivation.

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#### REFERENCES

- [1] Y. V. Ponomarev *et al.*, “Channel profile engineering of 0.1  $\mu\text{m}$ -Si MOSFET by through-the-gate implantation,” in *IEDM Tech. Dig.*, 1998, p. 635.
- [2] D. A. Antoniadis and J. E. Chung, “Physics and technology of ultra short channel MOSFET devices,” in *IEDM Tech. Dig.*, 1991, p. 21.
- [3] G. G. Shahidi *et al.*, “A high performance 0.15  $\mu\text{m}$  CMOS,” in *VLSI Tech. Dig.*, 1993, p. 93.
- [4] G. G. Shahidi *et al.*, “Indium channel implant for improved short-channel behavior of submicrometer NMOSFET’s,” *IEEE Electron Device Lett.*, vol. 9, p. 409, 1993.
- [5] P. Bouillon, R. Gwoziecki, and T. Skotnicki, “Anomalous short channel effects in Indium implanted nMOSFETs,” in *IEDM Tech. Dig.*, 1997, p. 231.
- [6] P. Bouillon *et al.*, “Re-examination of Indium implantation for a low power 0.1  $\mu\text{m}$  technology,” in *IEDM Tech. Dig.*, 1995, p. 897.
- [7] G. F. Cerofolini *et al.*, “Thermodynamic and kinetic properties of indium-implanted silicon,” *Thin Solid Films*, vol. 101, p. 263, 1983.
- [8] A. G. Milnes, *Deep Impurities in Semiconductors*. New York: Wiley, 1973.
- [9] A. Ono, R. Ueno, and I. Sakai, “TED control technology for suppression of reverse narrow channel effect in 0.1  $\mu\text{m}$  MOS devices,” in *IEDM Tech. Dig.*, 1997, p. 227.
- [10] S. K. Hong *et al.*, “The impact of Nitrogen implantation at (LDD) NIL on deep sub-micron CMOS devices,” in *Proc. SSDM*, 1999, p. 34.
- [11] Y. Okayama *et al.*, “Nitrogen concentration optimization for down-scaled CMOSFET with  $\text{N}_2\text{O}$ -based oxynitride process,” in *VLSI Tech. Dig.*, 1998, p. 220.