Wafer bonding by low-temperature soldering

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Abstract

Recently, wafer level packaging received lots of attention in microsystems because it shows the potential to reduce the packaging cost, while the yield of devices after dicing and packaging can be increased. However, there is a limitation of commercialized wafer bonding technology, i.e., the high process temperature, such as 1000°C of silicon fusion bonding, and 450°C of anodic bonding. A novel low-temperature wafer bonding with process temperature lower than 160°C is proposed, it applies the In–Sn alloy to form the interface of wafer bonding. The experiment results show helium leak test of 6×10^{-9} Torr l/s, and a tensile strength as high as 200 kg/cm^2. Reliability test after 1500 temperature cycles between −10°C and 80°C also shows no trace of degradation compared to the initial quality of the samples. This low-temperature soldering process demonstrates its promising potential at the wafer level packaging in industrial production. © 2000 Elsevier Science S.A. All rights reserved.

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1. Introduction

Silicon wafer bonding has been developed for more than a decade. Currently, commercial wafer bonders can offer 6 in. processes of silicon fusion bonding and anodic bonding [1]. Wafer bonding allows to form microstructures such as pressure sensor, accelerometer, and packaging of microsensors [2]. In most cases, the hermetic sealing and interface bonding strength are of major concern, while low-temperature processing is essential in the case of bonding a microelectronic wafer to a micromechanical wafer in order to facilitate integration and achieve an increase in device density. However, the commercialized wafer bonding technology cannot meet this demand well, since the process temperature is relatively high, such as silicon fusion bonding of 1000°C, and anodic bonding of 450°C [1]. The anodic bonding can be performed at 180°C by using high alkaline content glass [3], nevertheless, it is not a commercially available process and high alkaline content may cause degradation of ICs for monolithic IC

sensors. The intermediate bonding by using Au–Si eutectic bonding, i.e., adding an adhesive interlayer, has been proposed as another potential way to reduce bonding temperature. It involved a necessary process temperature of 500°C that is higher than the Au–Si eutectic temperature of 363°C [4]. On the other hand, an Au–Au$_4$Al–Si intermediate bonding at 350°C was reported for packaging infrared microsensors successfully [5]. The same group also used Au/Sn to Ni/Au solder bonding, and Sn/Pb to Ni/Au solder bonding for making a sealed cavity of capacitive pressure sensor, while the respective treatment temperatures were 300°C, and 250°C for fluxless soldering in a vacuum oven with infrared light [6]. Actually, all materials that provide enough bonding force to the adhesive can be used at the bonding interface. Epoxy and thermoplastic polymers have been applied to the wafer level packaging with heat treatment temperatures of 150°C and 280°C, respectively [7].

However, a lower bonding temperature is not only desirable for easier integration of circuits, but also for minimizing bonding-induced stress problem after cooling. Except for the above-mentioned hermetic sealing, interface bonding strength, and bonding temperature, the vacuum-sealed cavity is able to gain the design of pressure sensor of a wide dynamic range with high resolution [8]. Vacuum

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packaging is known to be necessary for thermal sensors and some resonant sensors due to the merit of increasing responsivity [9,10]. In this paper, we report a new low-temperature wafer bonding process based on using In–Sn alloy as the intermediate layer for bonding. The feasibility of forming a vacuum-sealed cavity by In–Sn wafer bonding is also studied.

2. Process development and experimental results

2.1. Basic preparation procedure of samples

In–Sn alloys have eutectic temperature near 120°C. This allows frequently used as the final treatment of step soldering. The In–Sn alloy shows fair wettability to most alloys. Its ductility and ability to withstand creep are compatible with Pb–Sn alloy. In the experiment, material of In–Sn (50/50) eutectic composition was vacuum-evaporated onto a lid wafer with film thickness of 2 to 12 μm, while another gold-coated wafer is used to imitate the sensor wafer. A 100 nm Au–Sn (80/20) thin layer was deposited subsequently on the In–Sn surface in order to avoid oxidation of indium when the In–Sn surfaces are exposed to atmosphere. A pair of matching patterns was delineated on both the films of individual wafers for the purpose of diffuse bonding. The two wafers were then taken for pattern alignment with a double-side aligner. They were then held in position with a fixture and transferred into a vacuum chamber for physical bonding. They were first subjected to vacuum evacuation and pressed, then gradually heated to a preset temperature for a defined soldering duration before cooling down. The integrated (bonded) wafers were than sawed into pieces of sample for subsequent testing.

2.2. Adhesive strength evaluation

In the case of real application, the contacting surface of sensor wafer may be bare silicon or SiO_2, so we designed six combinations of bonding interface to optimize, as shown in Table 1. The Au 2 μm/Ti 200 Å thin film has been deposited onto the base wafer B2 and B3, and lid wafer L2. Then In–Sn 12 μm and Au–Sn 100 nm films
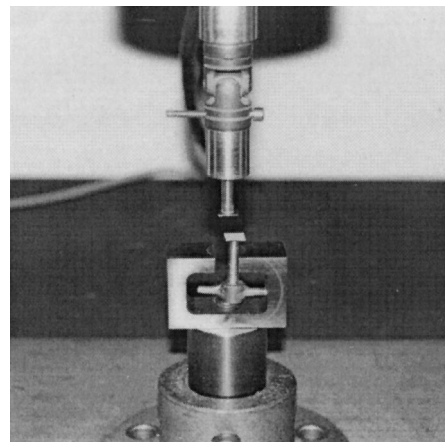

Fig. 1. Multi-axes pulling tester for characterizing the interface strength.

have been subsequently deposited onto the lid wafer L1 and L2. All of the depositions were done at the 3×10^{-6} Torr by thermal coating. The specimens were diced into 8×8 mm^2 samples for later on bonding experiments. A pair of samples were put inside a vacuum chamber, and the soldering condition is 160°C, 5×10^{-5} Torr, with an axial loading of 3 kg/cm^2 for 1.5 h.

Pulling test via a force perpendicular to the substrate can derive the interface bonding strength. The pulling tester is shown in Fig. 1. From Table 1, L1/B1 and L1/B2 pairs have failed, while the L1/B3, L2/B1 and L2/B2 show fairly high interface strength. It points out that the adhesion between Si and In–Sn is comparatively weak. Additionally, the $SiO_2//Ti//Au$ interface is weaker than $Si//Ti//Au$ interface. The pair of L2/B3 shows the best result of interface strength 207 kg/cm^2. We characterized the fracture surface of separated, broken, samples of L2/B3 pair. From Fig. 2, it can be observed as a ductile fracture surface from the fracture surface morphology. There is no evidence that cracks initiated from void defects and propagated during the pulling test, then fracture of the bonding interface may be induced by these

Table 1
Interface strength for various pairs of substrates

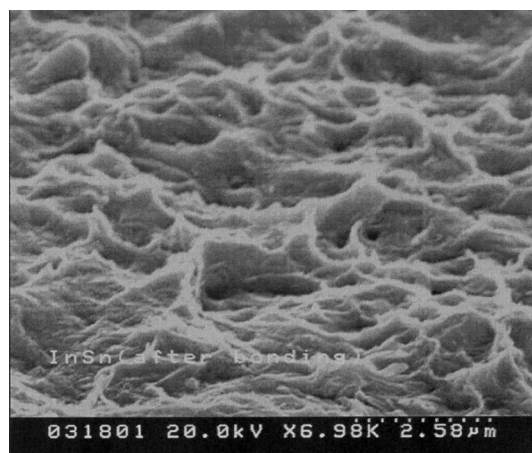| Base wafer	Lid wafer	
	(L1) Si// InSn// AuSn	(L2) Si//Ti// Au//InSn// AuSn (kg/cm^2)
(B1) Si (with native oxide)	Failed	52
(B2) Si/SiO$_2$ //Ti//Au	Failed	150
(B3) Si//Ti//Au	82 kg/cm^2	207

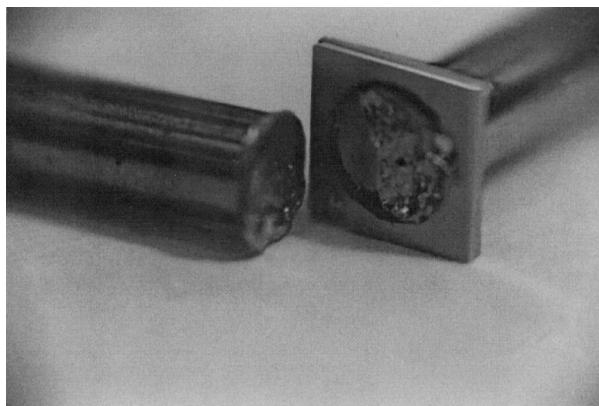Fig. 2. SEM photo of the fracture surface of bonding interface.

Fig. 3. Photo of the fracture surface of bonded sample pair.

cracks. Additionally, the fracture interface of some samples was even observed in the broken silicon substrate instead of the soldering interface, as shown in Fig. 3. We prepared the L2/B3 pair at the same condition but various temperatures as well. It is found from the experiment that an interface strength can be as high as 210 kg/cm^2 for the case of 160°C heat treatment (Fig. 4). The strength of 120°C sample drops from 125 kg/cm^2 down to 50 kg/cm^2 of 100°C sample. It means the soldering process could not proceed well at a temperature below the eutectic temperature of In–Sn alloy.

2.3. Sealing evaluation

After the bonding strength evaluation, helium leak rate tests were used to check the quality of the interface. Anisotropic Si wet etching was applied to make a hole through the wafer of one B3 sample. Another plain L2 sample was also prepared. They were bonded together at the same condition as in the previous bonding experiments but of various temperatures. We used the silver paste to fix the sample on an adapter, which was connected to a pumping tube of the leak rate tester. Then helium gas is sprayed onto the bonding interface. From Fig. 5, we find that the leakage rate decreases quickly when the bonding temperature increases, and a helium leakage rate as low as 6×10^{-9} Torr l/s can be obtained for temperatures higher
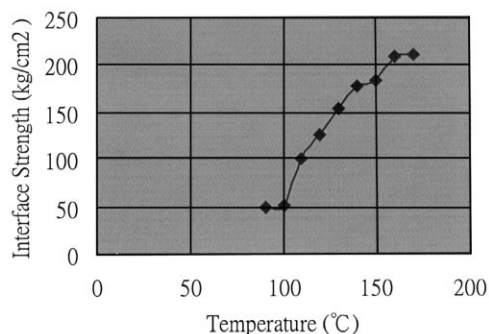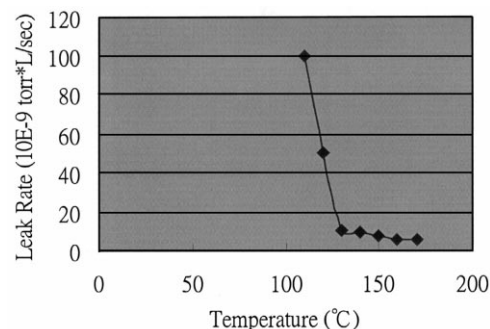

Fig. 5. Helium leak test data of different soldering temperatures.

than 150°C. This value is superior to that reported by others [11]. A fair value is obtained for 130°C, while the leakage rate becomes higher than 1×10^{-7} Torr l/s for bonding temperatures less than 110°C. Interface inspection by scanning acoustic microscopy (SAM) shows that the bonding interface is pore-free for the L2/B3-bonded samples (Fig. 6). This SAM has a resolution of about 100 μm and some small reflective steps will occur in Fig. 6, if there are some cracks or pores.

2.4. Materials characterization

Fig. 7 shows the surface morphology of the as-deposited In–Sn film, the roughness of 2–4 μm can be observed. We also found that lid wafers with a thickness of In–Sn less than 6 μm were hard to be bonded in the bonding experiment. This fact reflects that a minimum solder film thickness is necessary to overcome the influence of surface roughness. As a result, we applied 12 μm thick In–Sn solder film in the bonding experiment to avoid surface roughness effect. The Auger surface spectrum and depth profile analyses were applied to characterize the oxygen element content of a surface of Au–Sn with 100 nm thickness. It showed very low oxygen content. This

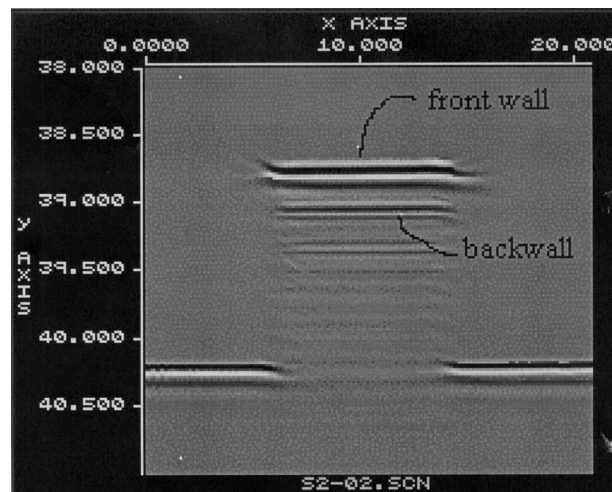Fig. 4. Interface strength vs. different soldering temperatures.

Fig. 6. Interface inspection of the bonding quality by SAM.

Fig. 7. SEM photo of the surface morphology of as-deposited In–Sn solder film.

fact helps us to believe that the Au–Sn thin film acts as a passivation layer to prevent oxidization beneath the In–Sn film, since the indium is a strong reduction precursor.

The raw materials for preparing In–Sn solder film have been characterized by X-ray diffraction (XRD) analysis. The major phase of In_3Sn (β) and minor phase of $InSn_4$ (γ) can be observed in the XRD pattern of In–Sn (50/50) solder preform, i.e., the raw materials. On the other hand, the XRD pattern of evaporated solder film shows major γ phase and minor β phase. Checking the eutectic point of the In–Sn phase diagram, the eutectic composition of In–Sn (51/49) at 120°C can be observed. However, in the case of In–Sn (50/50), the melting point becomes about 125°C [12]. In the soldering process of the bonding experiment, some grains of β-Sn (high-temperature phase with melting point of 232°C) will nucleate and grow from the $InSn_4$ matrix, while some $InSn_4$ and In_3Sn will start melting. A good melting state should be reached above 125°C, but some remaining β-Sn particles inside the molten solder need time and higher temperatures to consume themselves and transfer into the liquid through solid/liquid interface diffusion. This can explain that only the samples
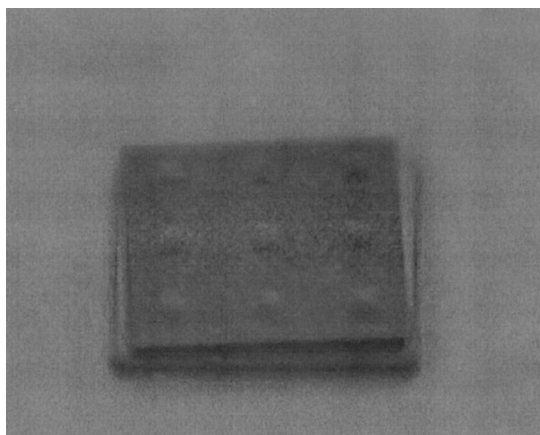

Fig. 8. Photo of concavity array of B3 surface due to pressure difference.

Table 2
The simulated displacement of center point for concave diaphragm vs. inside pressure

P_{inside} (Torr)	760	400	100	30	20	10	0.01	0.001
Displacement (μm)	0	2.06	3.72	4.1	4.15	4.2	4.26	4.26

treated above 130°C show good leak rate test results in Fig. 5. We also know indium is a material showing cold welding behavior. It means that some In-rich areas may start melting at a temperature a little bit below 125°C when a force loading is applied to the samples. This is the reason why L2/B3 samples still exhibit 50 kg/cm² bonding strength, even if this value is poor.

2.5. Characterization on vacuum degree and reliability

In order to identify the pressure inside the packaged cavity of L2/B3 samples, the wet-etched B3 wafer with a 15-μm thick diaphragm was bonded with the L2 wafer at 160°C. Then the bonded wafer were diced into 8×8 mm² pieces. Because the inside pressure is lower than the atmosphere, a concavity of the B3 surface can be observed by human eyes as shown in Fig. 8, and measured as 4-μm depth in the center. We built a FEM model to analyze and simulate the relationship between displacement of center point and inside pressure. Displacement will become saturated when the inside pressure is less than 0.01 Torr from Table 2. The measured displacement is about 4.1 ± 0.1 μm for various samples. As a result, we believe the inside pressure should be lower than 50 Torr. Packaging a microbolometer inside the cavity for directly measuring the vacuum degree may be a good method for more precise evaluation, since a microbolometer has been applied as a micro-pirani gauge for measuring the vacuum down to 0.001 Torr [13]. Moreover, a vacuum-sealed capacitance type pressure sensor has been reported as an alternative way for measurement [14].

The temperature cycles of 10 min duration at -10°C and 80°C with 2 min switch time were used to characterize the L2/B3 samples. Cycles of 100, 200, 400, 800, and 1500 was performed, and samples after 1500 thermal cycling still showed bonding strength of 200 kg/cm², a leakage rate of 6×10^{-9} Torr l/s, and a measured center displacement of about 4 μm. It exhibits no trace of degradation compared to the initial quality of the bonded samples.

3. Conclusion

A novel low-temperature wafer bonding with a process temperature lower than 160°C is proposed. It applies In–Sn

alloys to form the interface of wafer bonding. The experimental results show helium leakage rate of 6×10^{-9} Torr l/s, and a tensile strength of the bonding interface as high as 200 kg/cm^2. Reliability test after 1500 temperature cycles between $-10°C$ and $80°C$ also shows no trace of degradation compared to the initial quality of the samples. It is concluded that the In–Sn (50/50) eutectic solder is an ideal low-temperature interlayer for the bonding process of vacuum-sealed package applications of microsensors.

Acknowledgements

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Biographies

Chengkuo Lee received a MS degree in Materials Science and Engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1991. He also received a MS degree in Industrial and System Engineering from Rutgers University, New Brunswick, NJ, USA in 1993. He received the PhD degree in Precision Machinery Engineering from the University of Tokyo, Tokyo, Japan, on January 1996. He had worked in Mechanical Engineering Lab., AIST, MITI of Japan as a national post-doctoral fellow for a year. Thereafter, he was a senior research staff of Microsystems Lab., Industrial Technology Research Institute, Hsinchu, Taiwan. Since September 1997, he has joined the Metrodyne Microsystem, Hsinchu, Taiwan, and established the MEMS device division and micromachining fab. Currently, he is the general manager of MEMS device division. He has been the adjunct assistant professor in Electro-Physics Department of National Chiao Tung University in 1998.
His doctoral research involved an investigation of piezoelectric microcantilevers for sensing, actuation, and imaging application of atomic force microscopy. After graduation, his research interests are micromirrors, wafer bonding and packaging, and micro-flow sensors. Currently he is engaging in the development of microsensors based on CMOS processes and reliability issue of microsensors. He is a member of IEEE, MRS, AVS, and IEE Japan. He received the IUMRS graduate student award for the research on "the sol–gel derived PZT force sensor for scanning force microscopy" in 1994.

Wei-Feng Huang received his BS degree from Electro-Physics Department, and MS degree from Institute of Electro-Optical Engineering of National Chiao Tung University, Hsinchu, Taiwan, in 1996 and 1998, respectively. His major research interest is in packaging of microsensors.

Jin-Shown Shie earned his B.S.E.E. degree from National Cheng Kung University in 1965 and M.S.E.E. degree from National Chiao Tung University in 1968, both in Taiwan. In 1972 he received his PhD degree in Materials Sciences from SUNY at Stony Brook, USA. Since then he has joined the National Chiao Tung University and is currently the emeritus professor at the Institute of Electro-Optical Engineering. He has authored or co-authored about 40 journal articles and conference presentations and refereed papers.